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ELECTRONIC PROPERTIES OF SILICON INTERFACES PREPARED BY DIRECT BONDING

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Abstract - The influence of interface charges on the properties of Si-Si and Si-SiO₂ interfaces prepared by direct bonding has been investigated. Surface potentials of N-N and P-P interfaces and recombination currents in P-N junctions depend on surface and heat treatments. In both cases lower magnitudes were measured in samples pre-treated in HF compared to samples pre-treated in HNO₃. Bonded Si-SiO₂ interfaces with interface state densities of about 10¹¹ cm⁻² eV⁻¹ and low flatband voltages have been achieved.

1 - INTRODUCTION

The technique of directly bonding surfaces of materials together included in the silicon technology [1,2] has given rise to new possibilities for device geometries. Interfaces obtained by this kind of preparation have been included in novel insulating structures [2,3,4] and in discrete power devices [5,6]. In the works performed up to this date, the main efforts have been to demonstrate the mechanical properties of these interfaces, while the electronic behavior has been investigated only to limited extent. An interesting question, therefore, is whether this technique can be used in cases where device data critically depend on the electronic interface properties. The presence of interface charges accompanied by potential barriers and charge carrier recombination is the main factor limiting this possibility. In this work we have investigated the electronic properties of interfaces prepared by direct bonding of silicon wafer surfaces of both N- and P-type including materials with different bulk resistivities. Interfaces of the combinations N-N, P-P and P-N have been studied together with the bonded interface of the important combination SiO₂-Si.

2 - SAMPLE PREPARATION

Polished silicon wafers with flatness and warp similar to that of wafers used in integrated circuit production were cleaned by standard procedure in hot H₂O₂-NH₃ and H₂O₂-HCl solutions. This was followed by a treatment in HNO₃ or 2% HF:H₂O, water rinse and drying. The polished surfaces of wafer pairs were brought together using vacuum in a specially designed fixture. After releasing from the fixture, the wafers held together by adhesion forces, were loaded into an annealing furnace at room temperature. The furnace temperature was slowly ramped to the region 1000 - 1100 °C, where the samples were annealed for 1-2 hours, in an atmosphere of oxygen or nitrogen.

3 - EXPERIMENTAL RESULTS

Impurities and crystalline defects present at the bonded interface are expected to create charges and potential barriers. A charge Q at an interface between two semiconductors with a shallow doping concentration N creates an interface potential $V \sim Q^2 / N$. This means that the sensitivity to interface charges is less pronounced at higher doping levels. For resistivities higher than about 1 Ωcm, interface charge densities higher than about 10¹¹ cm⁻² are expected to cause considerable energy barriers (S. Bengtsson and O. Engström, unpublished). Further, small lateral variations in interface charge may cause considerable lateral variations in potential.

3.1 N-N AND P-P INTERFACES

Using spreading resistance measurements across an N-N interface lapped to a small angle for 10 Ωcm silicon an interface potential barrier was found. The result, shown in fig. 1, exhibit a clear peak in spreading resistance due to the interface potential barrier.

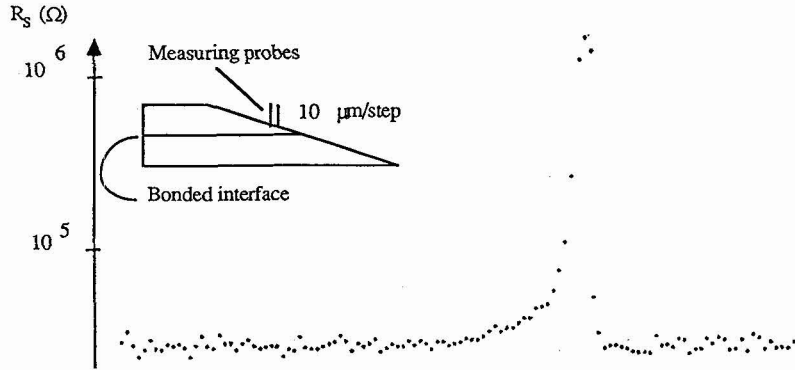


Fig. 1 - Spreading resistance measured across a bonded N-N-interface prepared of two 10 Ωcm silicon wafers and with HNO₃ used as prebond treatment.

The lateral distribution of the interface potential was investigated by scanning the wafer surface with a He-Ne laser beam and the photocurrent at the interface was measured as a function of the position of the laser spot [7]. No bias was applied during the measurement. The variation in photocurrent, displayed in fig. 2 demonstrates the lateral variations in interface potential. The influence of surface effects was negligible, as found from measurements after repeated surface treatments. This variation in interface potential gives current-voltage characteristics with a much smaller curvature than expected from a structure with a simple energy barrier.

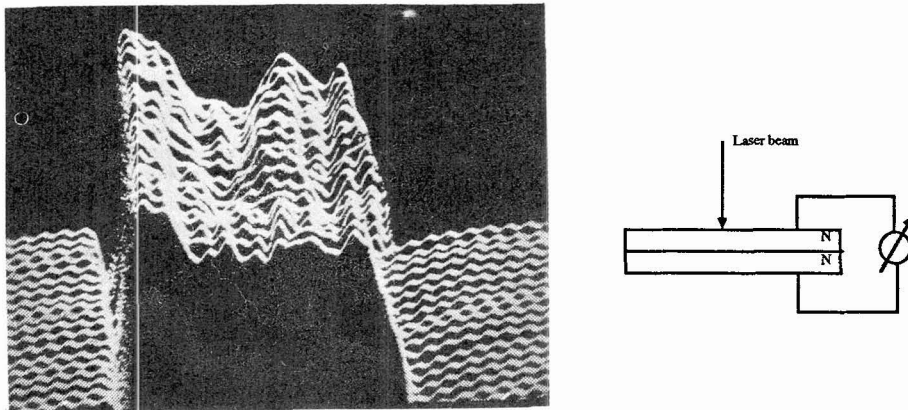


Fig. 2 - The lateral variation of photocurrent of a bonded N-N-interface.

The differential resistance at low voltage was used to estimate the influence of different surface and heat treatments on the interface charge. Fig. 3 displays the differential resistances before and after a post-bonding anneal at 1000 °C during about 90 minutes for two different pre-bond treatments and for different silicon resistivities. For samples with low resistivities, a considerable decrease in differential resistance after the heat

treatment indicates a decreasing interface charge for the samples pre-treated in HNO_3 . The samples pre-treated in HF exhibit a considerably smaller potential barrier, already after the wafer bonding procedure, and it was not necessary to give these samples a post-bonding anneal. These results show that the native oxide layer present on silicon surfaces after treatment in HNO_3 is important in the generation of defects influencing the interface resistance.

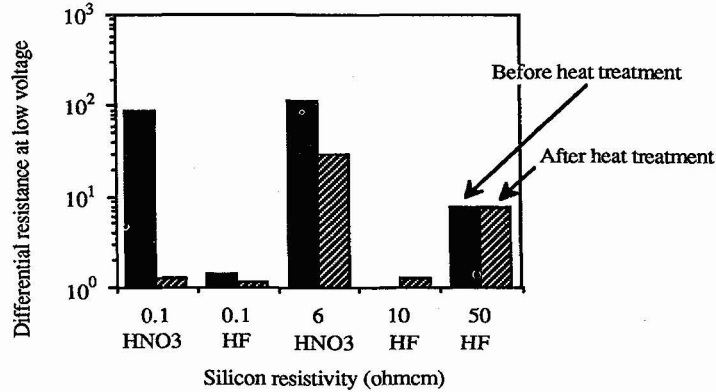


Fig. 3 - Differential resistance at low voltage for some samples with bonded N-N-interface as a function of silicon resistivity for different surface and heat treatments.

3.2 P-N INTERFACES

PN-junctions were prepared by bonding low ohmic P^+ -type wafers of resistivities $< 0,1 \Omega\text{cm}$ to N-type wafers of $1-5 \Omega\text{cm}$ resistivity. Current voltage characteristics in the forward direction are shown in fig. 4 for two samples with surface treatment before bonding using HF and HNO_3 respectively. The n-factors in the expression $I = I_0 \exp(qV/nkT)$ were found to be in the region of 1,5 - 7, with the lowest values for samples treated in HF. This reflects a higher recombination current in samples treated in HNO_3 , again indicating that surface treatment in HF before bonding of two silicon surfaces gives a lower density of electron states at the bonded interface than does a corresponding treatment in HNO_3 . Breakdown voltages in the reverse direction of about 75 V were found for bonded P^+N -interfaces using 2-3 Ωcm N-type wafers.

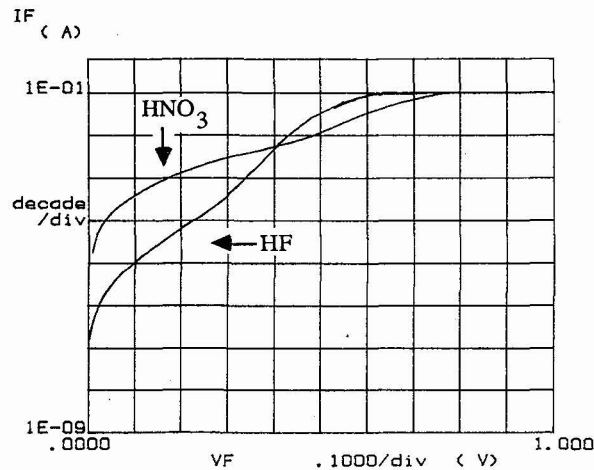


Fig. 4 - Current voltage characteristics of two bonded P^+N -junctions treated in HF and HNO_3 , respectively, before wafer bonding.

3.3 MOS-STRUCTURES

MOS-structures were prepared by bonding a thermally oxidized silicon wafer to a bare silicon wafer. After this, the bulk silicon of the oxidized wafer was etched off using a selective silicon etch, leaving a

silicondioxide-silicon structure with a bonded interface. Aluminium contacts were evaporated onto both sides of the structure to make MOS-capacitors and the interface properties were characterised using CV-technique. Usually low flatband voltages and low midgap interface state densities at and above $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ were found. Fig. 5 shows measured CV-curves and calculated interface state density for a MOS-capacitor with bonded interface. Reference capacitors with thermally grown interfaces oxidized in the same furnace as the wafers used in the bonding procedure, had interface state densities in the range 10^{10} to $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

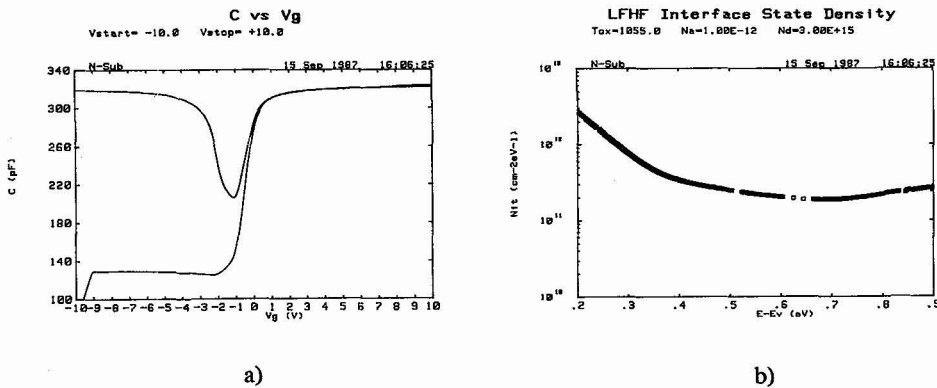


Fig. 5 - a) HF and LF CV-curves for a MOS-capacitor with bonded SiO_2 -Si interface.
b) Interface state density obtained from the curves in a).

4 - DISCUSSION

For N-N and P-P interfaces the interface charges were reduced by heat treatment or by using HF as surface treatment before wafer bonding. In fact, the lower differential resistances obtained after these treatments were of the same magnitudes as the contact resistances of the samples. Estimations of the interface charges based on these results give concentrations in the region below 10^{11} cm^{-2} . In a recently published work [1], low interface potential barriers were found for bonded P-P interfaces of samples with bulk resistivities of 0,004 Ωcm . However, for such low resistivities only interface charges of about 10^{13} cm^{-2} are expected to give a measurable interface barrier. It was also possible to obtain P⁺N-junctions with low recombination currents. For P⁺N-junctions prepared by direct bonding technique, the P⁺-region may be expected to diffuse into the N-region, creating a P⁺N-junction at a certain distance from the mechanical interface. As seen from fig. 4, this interface still has a certain influence on the properties of the PN-junction, but can be controlled by the chemical surface treatment before bonding. Finally, we have shown that SiO_2 -Si interfaces can be prepared with low interface state densities and low flatband voltages. This demonstrates that silicon interfaces obtained by direct bonding can be utilized in cases where the electronic properties are crucial for the behaviour of a device.

5 - ACKNOWLEDGEMENTS

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