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André Touboul, J. Lopez, G. Lecoy. HOT CARRIERS IN REDUCED GEOMETRY SURFACE-CHANNEL CHARGE-COUPLED DEVICES. *Journal de Physique Colloques*, 1981, 42 (C7), pp.C7-183-C7-192. 10.1051/jphyscol:1981721 . jpa-00221658

**HAL Id: jpa-00221658**

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Submitted on 4 Feb 2008

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## HOT CARRIERS IN REDUCED GEOMETRY SURFACE-CHANNEL CHARGE-COUPLED DEVICES

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**Résumé :** Pour un C.C.D. à canal en surface, les champs électriques à l'interface ont été calculés par une méthode numérique (différences finies). Le champ normal supérieur au champ critique peut donner lieu à de l'ionisation par impact sous le milieu des grilles mais pas dans les espaces interelectrodes. Néanmoins, le rôle de ce champ a peu de conséquences sur le fonctionnement en registre à décalage de ces dispositifs. Le champ longitudinal, défini comme la somme de deux composantes n'est supérieur au champ critique que pour une très faible partie du stade initial du transfert. Tous ces résultats ont été retrouvés sur une structure théorique ayant une longueur de grille de 1.5  $\mu\text{m}$ . Néanmoins, cet effet de chauffage des porteurs est la cause principale de la limitation de la fréquence maximum des transferts.

**Abstract :** In a surface-channel C.C.D., electric fields have been computed with the help of a finite-difference method. The normal field, higher than the critical value, can create impact ionization under the gates but not in the gaps. Nevertheless this field is not crucial for the C.C.D. operation as a shift register. The longitudinal field, defined as the sum of two components, is higher than the critical field but at the very beginning of the transfer. All those results have been found again for a theoretical device with 1.5  $\mu\text{m}$  gate length.

Nevertheless this heating of the carriers is found to be the major limitation to the maximum transfer frequency.

## I. INTRODUCTION

Reducing the dimensions of surface-channel Charge-Coupled Devices has two main purposes : increasing the density of integration and operating the devices at higher transfer rates.

As the charge transfer is controlled by the interface electric fields, we may expect hot carriers which will consequently affect the transfer and/or the storage behaviour of the device. This work has been focused on the transfer of free carriers in a surface p-channel C.C.D. presenting a very simple electrode structure : one level of metallic (Al) gates with interelectrode gaps. The values of the electric fields under the gates and in the gaps could be such that impact ionization mechanisms, hot carriers injection into  $\text{SiO}_2$  or mobility saturation (and then velocity saturation) might take place and reduce the transfer speed. An actual sequence of transfer used for C.C.D.'s operation is described. The clock pulses  $V_{G1}$  and  $V_{G2}$  applied

to two adjacent gates are represented in Fig. 1.

The following sequences will be considered :

i) the carriers are stored under the gate  $G_1$ ; the  $V_{G1}$  and  $V_{G2}$  signals are respectively equal to  $V_{st}$  and  $V_r$ .

ii) the  $V_{G2}$  signal swings from  $V_r$  to  $V_{st}$ : the charge transfer starts.

iii)  $V_{G1}$  and  $V_{G2}$  are equal during the clock pulses overlap.

iv) the transfer is finishing:  $V_{G1}$  goes to  $V_r$ .

For most of clock frequencies, these two clock signals present this overlap, and a rise time  $\tau_r$  much smaller than the fall time  $\tau_f$  (see fig. 1).

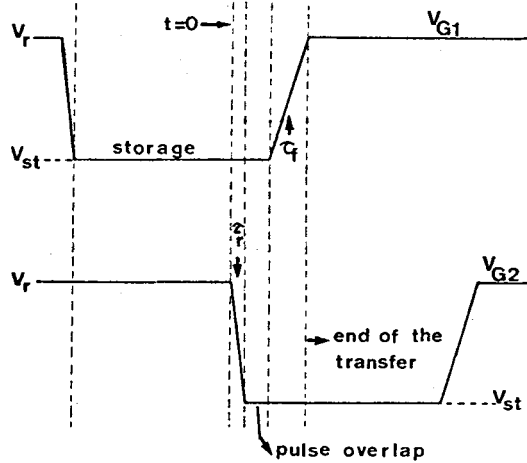


Fig. 1 : Clock pulses diagram for a complete sequence of transfer (3-phase C.C.D.).

In order to evaluate the electric fields, we have developed a simulation of the elementary transfer process between two gates. This 2-D model of the device operation includes the effect of the interelectrode gap and takes into account the field-dependent mobility.

A 1-D model of the M.O.S. structure has given results supporting a "sheet-model" for the inversion channel where the free carriers are located.

## 2. CHARACTERIZATION AND CALCULATION OF THE ELECTRIC FIELDS

Normal components  $E_N$  of the field will be distinguished from longitudinal ones  $E_L$  (in the transfer direction:  $\vec{ox}$  axis).

To calculate the strength of the fields, we need a physical model of the structure defined by the following assumptions :

- i) the oxide layer (thickness :  $d_{ox}$ ) is ideal
- ii) the Si-SiO<sub>2</sub> interface is free of traps
- iii) we have neglected the quantum effects associated with the inversion layer population [ 1 ]
- iv) for the considered intervals of time which control the transfer sequences, thermal generation of carriers is not taken into account.
- v) the majority carrier current is negligible.

This set of equations is used for a n-type silicon substrate (p-channel)

$$\Delta V = 0 \quad (1)$$

for  $0 < y < d_{ox}$

$$\Delta V = - \frac{q}{\epsilon_{Si}} \cdot [N_D + p(x,y,t) - n(x,y,t)] = - \frac{q \cdot \rho(x,y,t)}{\epsilon_{Si}} \quad (2)$$

for  $y > d_{ox}$

$$\vec{J}_p = q \mu_p \left[ \vec{E}(x,y,t) \cdot p(x,y,t) - \frac{D_p}{\mu_p} \text{grad } p(x,y,t) \right] \quad (3)$$

$$q \frac{\partial p(x,y,t)}{\partial t} = - \text{div } \vec{J}_p \quad (4)$$

The boundary conditions are :

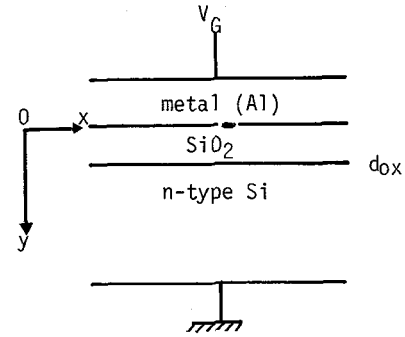
$$V(x,y) \rightarrow 0 \quad \text{for } y \rightarrow \infty$$

$$E(x,y) \rightarrow 0 \quad \text{for } y \rightarrow \infty \quad (5)$$

$$\rho(x,y) \rightarrow 0 \quad \text{for } y \rightarrow \infty$$

$$V(x,y=0) = V_G \quad (6)$$

$$\frac{\epsilon_{ox}}{\epsilon_{Si}} E(x, y=d_{ox}^-) = E(x, y=d_{ox}^+) \quad (7)$$



The resolution of these equations by means of a finite differences method under one gate leads to the normal field  $E_N$  after the onset of the deep depletion regime and an ideal injection of minority carriers (the signal) representing the inversion layer population. The results of this calculations imply a 1-D model for the transversal field : 99 % of the signal carriers are located in about 120 Å under the oxide layer for a voltage swing of 10 V on the gate. For a doping density of  $N_D = 10^{15}/\text{cm}^3$ , the normal field  $E_N$  and the signal charges  $Q_S$  distribution are plotted in Fig. 2.

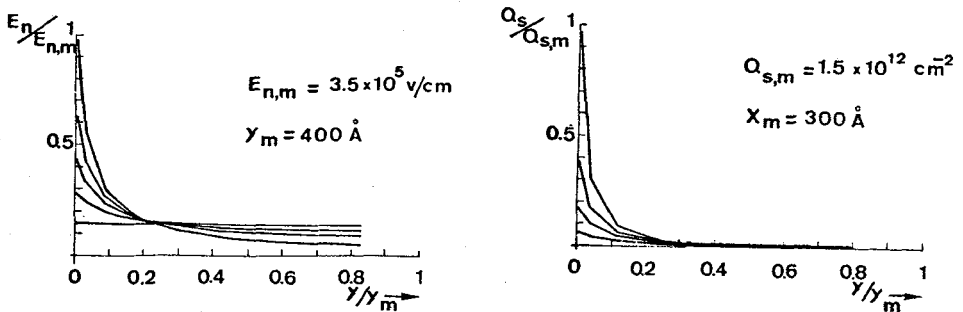


Fig. 2 : Normal field  $E_n$  and carrier density  $Q_s$  at the interface.

Eqs. (1) to (4) become easier to solve and the longitudinal fields can be calculated anywhere along the interface when considering a "sheet-model" for the charges and an infinite depleted region. The structure under test is represented in Fig. 3 : it is periodic. Different gate lengths ( $L : 1.2 \rightarrow 4 \mu\text{m}$ ) and gaps ( $2 \rightarrow 0.4 \mu\text{m}$ ) have been considered. A theoretical structure ( $L = 1.5 \mu\text{m}$  and  $g = 0.1 \mu\text{m}$ ) has also been investigated to point out specific gate shortening effects.

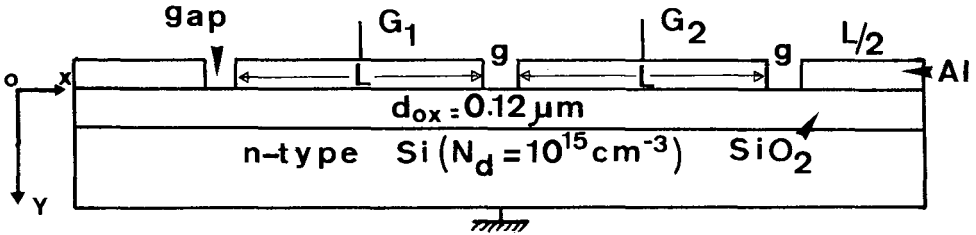


Figure 3 : Longitudinal view of the structure used for the transfer model.

The charge transfer in the x-direction is expressed by (3) and (4) which give :

$$J_p(x,t) = q \mu_p \left\{ E_L(x,t) p(x,t) - \frac{D_p}{\mu_p} \frac{\partial p(x,t)}{\partial x} \right\} \quad (8)$$

$$\vec{E}_L(x,t) = \vec{E}_e(x,t) + \vec{E}_i(x,t) \quad (9)$$

$$q \frac{\partial p(x,t)}{\partial t} = - \frac{\partial J_p(x,t)}{\partial x} \quad (10)$$

The electric field  $E_L(x,t)$  is the sum of an external component  $E_e(x,t)$  due to the neighbouring gate voltages [2] and of an internal component  $E_i(x,t)$  induced by the charges [3];  $E_i(x,t)$  is evaluated from the analytic expression derived by Carnes [3] on the basis of the surface potential [4] :

$$E_i(x,t) = - \alpha \frac{\partial p(x,t)}{\partial x} \quad (11)$$

The knowledge of  $V_{G1}$  and  $V_{G2}$  corresponding to the different transfer sequences applied to eqs (1) and (2) leads to  $E_e$ .

Then (8), (9) and (10) can be solved everywhere to give the carrier density  $p(x,t)$ . The numerical methods used for all the differential equations are based on a finite difference scheme [5, 6].

In the interelectrode gaps, we have derived an analytic expression of the potential which is a function of the two adjacent gate voltages, the oxide thickness, and the depletion layer depth.

### 3. EFFECT OF THE NORMAL FIELD $E_N$

For the devices described in section 2), we have calculated this field at the interface. When there is no carrier in the surface well, the value of  $E_N$  under the middle of a gate is  $5.0 \times 10^4$  v/cm for  $|V_G| = 10$  V. The presence of minority carriers increases strongly this field and it reaches  $3.5 \times 10^5$  v/cm for a carrier density of  $1.5 \times 10^{12}/\text{cm}^2$ . This situation is reported in figure 2.

In the gaps between two gates, a potential barrier takes place. When the two gates are biased at the same potential  $|V_{G1}| = |V_{G2}| = 10$  V, this barrier  $\Delta V_s$  is a strong function of the gate length  $L$  and of the gap width  $g$ . The different values of  $\Delta V_s$  and  $E_N$  in the gaps are given in table 1.

$V_G$ (V)	- 10	- 10	- 10	- 5
$L$ ( $\mu\text{m}$ )	12	12	4	1.5
$g$ ( $\mu\text{m}$ )	2	0.4	0.4	0.1
$\Delta V_s$ (V)	2.39	0.41	0.36	0.013
$E_N$ (V/cm)	$2.35 \times 10^4$	$3.6 \times 10^4$	$3.71 \times 10^4$	$3.06 \times 10^4$

Table 1 : Values of the potential barrier and  $E_N$  in the gaps.

The effect of the gate field has been extensively studied in M.O.S. structures [7, 8, 9]. We shall point out its specific effects on C.C.D.'s operations.

i) For these typical values of the gate voltages ( $|V_{st} - V_r| = 10$  V), the doping density ( $N_D = 10^{15}/\text{cm}^3$ ) and of the oxide thickness, the normal field is always less than the oxide breakdown field, nevertheless it is stronger than the critical field  $E_e$  which is  $1.8 \times 10^4$  v/cm for holes [10] and can even produce impact ionization [11] under the gates but not in the gaps. This effect could occur but for more doped substrates. Nevertheless, the resulting change in carrier density would not be of a great importance (less than  $10^{-5}$ ) on the first-order operation of C.C.D.'s.

ii) Another consequence of this normal field could be the injection of hot carriers into  $\text{SiO}_2$ . As the C.C.D.'s under study are implemented on n-type substrate, the free carriers are holes. The energy barrier at the interface is of the order of 3.8 eV [8] and reduces the emission probability. This injection could arise from "Channel Hot Carriers" when the carriers are transferring along the device or from "Substrate Hot Carriers" for some thermally generated carriers.

Anyway, the shift  $\Delta V_T$  of the threshold voltage does not constitute a very crucial limitation because the device working as a delay line is always biased in the deep depletion regime for times smaller than those ruling the thermal generation. A simplified calculation of this shift  $\Delta V_T$  for the above-mentioned data gives

values less than  $10^{-2}$  V.

#### 4. ANALYSIS OF THE LONGITUDINAL FIELD $E_L$ DURING THE TRANSFER

The variation of the mobility with the electric field  $\vec{E}_L(x)$  is introduced by the relation :

$$\mu_p = \mu_0 / \left\{ 1 + [E_L(x)/E_c]^\beta \right\}^{1/\beta} \quad (12)$$

where  $\mu_0$  is the "low field" interface mobility taken equal to half the bulk value,  $E_c$  is the critical field and  $\beta$  a parameter equal to 2 as reported in [10], [12].

In this section, we shall comment the results of the field calculation for the different stages of the transfer.

##### i) storage under the gate $G_1$ :

The transfer simulation is initiated with an arbitrary distribution of carriers under the emitting gate  $G_1$  under which their density is set constant.

The values of the external field  $E_e$  at the middle of the gaps are very dependent on the gap width  $g$  :  $E_e = 2.2 \rightarrow 9.43 \times 10^4$  V/cm when  $g$  is reduced from 2 to  $0.4 \mu\text{m}$  (gate voltage : - 10 V). At the edges of the gates, this component  $E_e$  increases also when  $g$  decreases ( $E_e$  :  $2.62 \rightarrow 7.91 \times 10^4$  V/cm) whereas it is nearly insensitive to variations of the gate length  $L$  from 12 to  $4 \mu\text{m}$ . For a theoretical device ( $L = 1.5 \mu\text{m}$  and  $g = 0.1 \mu\text{m}$ ), the calculation gives for a gate voltage of - 5 V:

$$\begin{cases} E_e = 7.61 \times 10^4 \text{ V/cm in the mid-gap} \\ E_e = 6.4 \times 10^4 \text{ V/cm at the gate edges} \end{cases}$$

These values of  $E_e$  allow us to expect fields higher than  $10^5$  V/cm for gate voltages greater than - 5 V.

It should be noticed that all the values of  $E_e$  are higher than the critical field  $E_c$ .

The internal field  $E_i$  has a very similar magnitude but its sign is always opposite to the one of  $E_e$ . Under the same bias conditions and at the same locations, the computed values are :

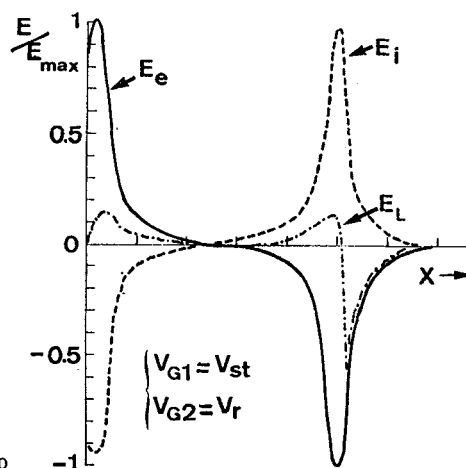
$$\begin{cases} E_i = 5.42 \rightarrow 9.2 \times 10^4 \text{ V/cm in the mid-gap} \\ E_i = 1.81 \rightarrow 5.4 \times 10^4 \text{ V/cm at the gate edges for } g \text{ varying from 2 to } 0.4 \mu\text{m}. \end{cases}$$

For the  $1.5 \mu\text{m}$  device,  $E_i$  compensates exactly  $E_e$  in the gaps.

The resulting field  $E_L$  (eq. 9) is smaller than any of the two components but still higher than  $E_c$  at the gate edges. This field  $E_L$  will play an important role during the next two stages. In figure 4, the resulting field  $E_L$  and the two components  $E_e$ ,  $E_i$  are plotted for a  $4 \mu\text{m}$  gate length device.

Fig. 4 : The longitudinal field  $E_L$  and the two components  $E_i$ ,  $E_e$  at the beginning of the transfer.

$$\begin{aligned} E_{L,max} &= 2 \times 10^3 \text{ V/cm}; \\ E_{e,max} &= 9.43 \times 10^4 \text{ V/cm}; \\ E_{i,max} &= 9.23 \times 10^4 \text{ V/cm}. \end{aligned}$$



ii) Rise time of  $V_{G2}$  and clock pulses overlap

When  $V_{G2}$  is equal to  $V_{st}$ ,  $E_L$  is still higher than  $E_C$ ; then, the first part of the transferred carriers will reach the saturation velocity only in the gaps. This will last from 1 to  $10^{-2}$  nsec according to the electrode dimensions which impose the clock frequency. At the beginning of the pulses overlap, the values of  $E_L$  are equal to  $1.8 \times 10^4$  V/cm at the gate edges for the  $4 \mu\text{m}$  device.

For the  $1.5 \mu\text{m}$  device, this field is more important (even for  $V_G = -5$  V) :

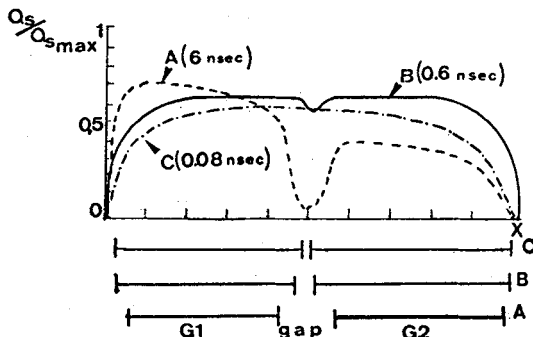
$$\begin{cases} E_L = 2.75 \times 10^4 \text{ V/cm in the gap} \\ E_L = 3.12 \times 10^4 \text{ V/cm at the } G_2 \text{ gate edge} \end{cases}$$

The external field  $E_e$  decreases to lower values in the gaps and its direction changes at the exact mid-gap. The transfer is controlled exclusively by  $E_i$ .

The resulting field  $E_L$  at the end of the overlap has typical values of 3 to  $6 \times 10^3$  V/cm for any device. An equilibrium is reached for the carriers distribution under the two gates (see Fig. 5). An extremum is obtained in the midgap :

Fig. 5 : Distribution of the carriers at the end of the pulse overlap stage (the indicated time gives the duration of the overlap)

$$\begin{aligned} \text{A : } L &= 12 \mu\text{m} ; g = 2 \mu\text{m} \\ \text{B : } L &= 4 \mu\text{m} ; g = 0.4 \mu\text{m} \\ \text{C : } L &= 1.5 \mu\text{m} ; g = 0.1 \mu\text{m} \end{aligned}$$



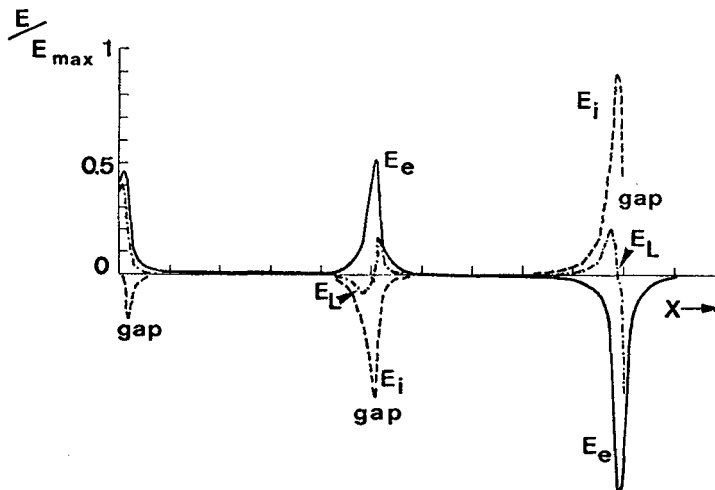


consequently  $E_i$  will be null and change its direction for gaps larger than  $0.1 \mu\text{m}$ . This illustrates the effect of the potential barrier  $\Delta V_s$  in the gaps reported in table 1, of section 3.

iii) Fall time of  $V_{G1}$  : final stage of the transfer

During this stage, in spite of the importance of the external field  $E_e$ ,  $E_L$  is less than  $E_c$  for any device because of the values of  $E_i$ . These 3 fields are reported in Fig. 6 for  $V_{G1} = V_{G2}/2$ .

Fig. 6 : Variation of the resulting field  $E_L$ ,  $E_e$  and  $E_i$  for  $V_{G1} = V_{G2}/2 = -5 \text{ V}$  (at half the fall time of  $V_{G1}$ ).



The calculation gives very high values for  $E_L$  at the right edge of  $G_2$  but as no transfer is possible, these fields have no effect on the carriers.

## 5. CONCLUDING REMARKS

We have shown that the effects of  $E_L$  are more important than the ones of the normal field  $E_N$  when considering the carriers transfer.

i) The calculation of the two components  $E_e$  and  $E_i$  of  $E_L$  have given in most of the cases values higher than  $E_c$  (except at the end of the overlap). Meanwhile, an effective heating of the carriers was found possible only during a very little fraction of the transfer sequence because of the simultaneous action of these two opposite fields.

This illustrates the obligation of considering both influences of the charge distribution and of the external field as was suggested in [13].

ii) To point out the effect of the field-dependent mobility (eq. 12), we have compared the computed carrier density when assuming a constant mobility with the previously described results. We have selected the rise time of  $V_{G2}$  and the pulse overlap stages during which we could show that the heating of the carriers happened. At the end of the  $V_{G2}$  rise time, the carrier density under the center of  $G_2$  is only

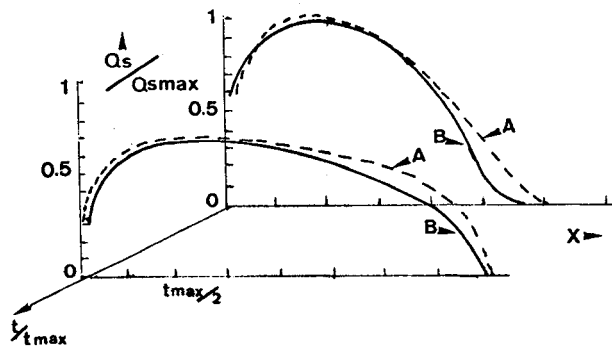
$1.2 \times 10^8 \text{ cm}^{-2}$  whereas the calculation, on the basis of the constant mobility, gives  $7.3 \times 10^9 \text{ cm}^{-2}$ . At the right edge of  $G_2$  where no carrier is found, the same calculation gives  $8.8 \times 10^4 \text{ cm}^{-2}$ .

At the middle of the overlap stage, the carrier distributions are very similar at the left edge and under the center of  $G_2$  whereas the density is three times higher at its right edge. This acceleration of the transfer is clearly related to the use of a constant mobility.

Furthermore, the equilibrium is reached in 60 psec instead of 80 psec under the two gates  $G_1$  and  $G_2$  equally biased at  $V_{st}$ .

These carrier distributions have been plotted in Fig. 7 for the two values of the mobility.

Fig. 7 : Comparison of the carrier distribution under  $G_1$  and  $G_2$  after the rise time of  $V_{G2}$  and at the overlap for different mobility laws :  
 A : constant mobility  $\mu_p = \mu_0$   
 B : field-dependent mobility  $\mu_p = \mu_p(E)$



According to an actual 3-phase clock pulse diagram (see Fig. 1), the  $4 \mu\text{m}$  device might be operated at clock frequencies of the order of 35 MHz. In that case, the time interval during which carriers are heated represents only 1.1 % of the clock period. For the  $1.5 \mu\text{m}$  device, the theoretical clock frequency is 258 MHz and the time when carrier heating should occur is 0.8 % of the clock period which is of the same order of the preceding one. This result is rather surprising because associated with the reduction of the dimensions were expected more effects of the mobility saturation. The reduction of the clock frequency due to that effect is only of 1.5 %.

iii) For this non-overlapping gate structure under test, the geometrical parameter which controls the electric fields is the gap width. Its influence on  $E_L$  has been found to be more preponderant than the reduction of the gate length (even for  $L$  as small as  $1.5 \mu\text{m}$ ).

Furthermore, this "theoretical"  $1.5 \mu\text{m}$  device has presented a behaviour which is mainly similar to the one of more conventional devices.

REFERENCES

- [ 1 ] F. STERN, C.R.C. Critical Review in Sol. Stat. Sciences, p. 499, (1974)
- [ 2 ] J.E. CARNES, W.F. KOSONOCKY et al., IEEE J. Sol. St. Circ. SC-6, p.322 (1971)
- [ 3 ] J.E. CARNES, W.F. KOSONOCKY et al., IEEE Trans. El. Dev. ED-19,p.798, (1972)
- [ 4 ] C.K. KIM, M. LENZLINGER, J.A.P. 42, p. 3586, (1971)
- [ 5 ] R.S. VARGA, "Matrice iterative analysis", Prentice-Hall, Englewood Cliffs N.J. (1962)
- [ 6 ] C.H. CHAN, S.G.C. CHAMBERLAIN, S.S.E. 17,p. 491 (1974)
- [ 7 ] S.A. ABBAS, R.C. DOCKERTY, A.P.L. 27, p. 147 (1975)
- [ 8 ] T.H. NING, P.W. COOK et al., IEEE Trans. El. Dev. ED-26, p. 346 (1979)
- [ 9 ] P.E. COTTRELL, R.R. TROUTMAN, T.H. NING, IEEE Trans. El. Dev. ED-26, p. 520 (1979)
- [ 10 ] C. JACOBONI, C. CANALI et al., S.S.E. 20, p. 77 (1977)
- [ 11 ] K. HESS, C.T. SAH, S.S.E. 22, p. 1025 (1979)
- [ 12 ] K. HESS, C.T. SAH, IEEE Trans. El. Dev. ED-25,p. 1399 (1978)
- [ 13 ] M.H. ELSAID, S.G. CHAMBERLAIN, L.A.K. WATT, S.S.E. 20, p. 61 (1977)