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# Innovative Design and Validation of a Zero-Cost Medium-Voltage Transistor for IoT Applications

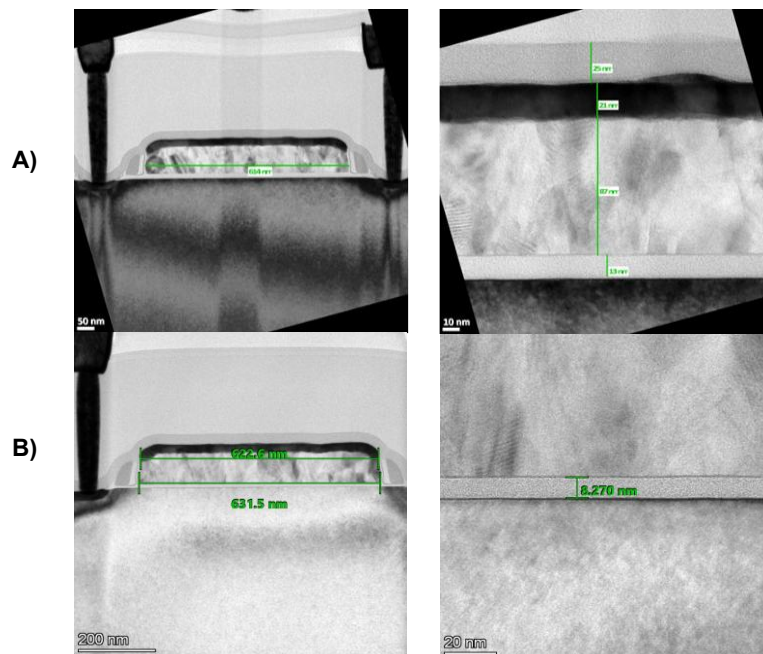
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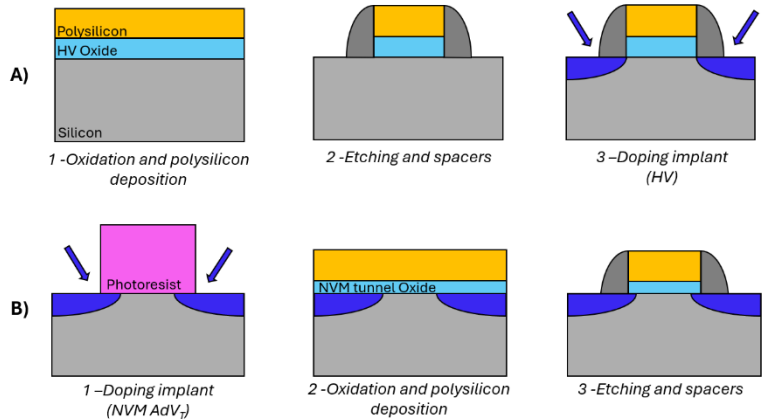
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The growing demands of the Internet of Things (IoT) industry require the development of efficient and cost-effective manufacturing technologies [1, 2]. In this context, this paper presents a fabrication process flow, physical and electrical simulations (based on Technology Computer Aided Design or TCAD tools) and electrical and reliability experimental results related to a new zero-cost transistor manufactured in a 40 nm embedded Non-Volatile Memory (eNVM) technology. This transistor is designed to provide the same electrical characteristics as a Medium Voltage (MV) MOS transistor. The proposed transistor, which does not require any additional fabrication step or new photolithographic mask, reuses most of the manufacturing steps from the High Voltage (HV) transistor and from the eNVM transistors. Indeed, the new MV MOS uses the spacers and the polysilicon gate inherited from the HV MOS. Its gate oxide is derived from the tunnel oxide of the eNVM cell, while its LDD (Lightly-Doped Drain) implant is implemented using the  $V_T$  adjustment implant ( $AdV_T$ ) from the same eNVM cell. Since the tunnel oxide of the eNVM is 40% thinner than the HV oxide, it allows the use of lower voltages. Moreover, the  $AdV_T$  implant, which is performed earlier in the process flow before HV MOS gate etching is independent of the gate and spacer dimensions. This enables precise control of the LDD doping area beneath the gate. Figure 1 shows the morphology of the new MV transistor versus the HV transistor through two TEM (Transmission Electron Microscopy) cross-section.



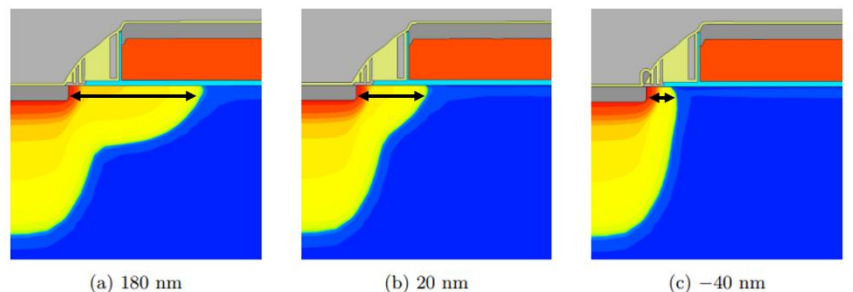
**Fig. 1:** TEM cross section: morphology of the HV MOS (A) versus the new MV transistor (B).

As the AdV<sub>T</sub> implant is performed before the HV MOS gate, preventing the use of the self-aligned gate technique during the implantation step, a photoresist is employed to mask the future gate location and to determine L<sub>DD</sub> implantation areas. The AdV<sub>T</sub>-associated mask, commonly open for eNVM areas and closed elsewhere on the chip, receives two openings adjacent to the future gate location. Figure 2 shows the main fabrication steps for the traditional (A) and proposed (B) L<sub>DD</sub> implantation techniques.



**Fig. 2:** Main process steps for the two LDD implantation techniques: A) Usual technique for LDDs self-aligned on the gate (example of HV MOS); B) LDD implanted before the gate using a photoresist.

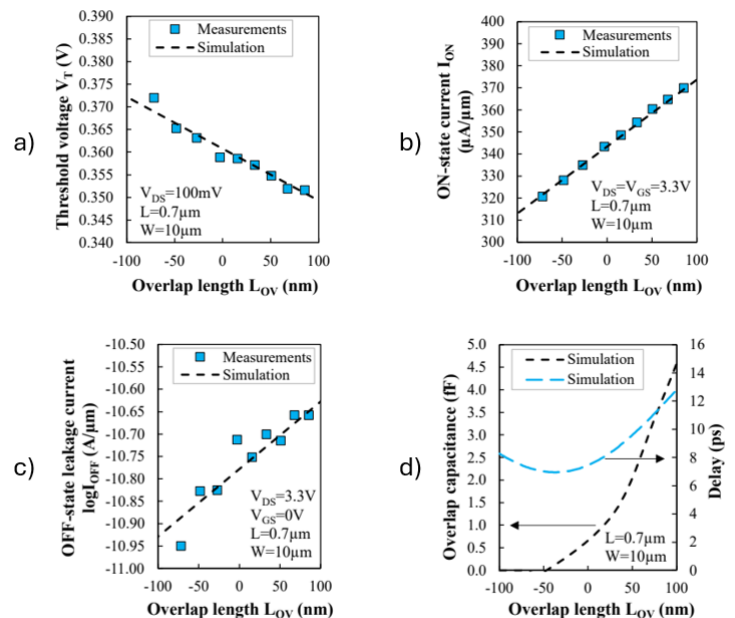
The technique's key advantage lies in the flexibility of the L<sub>DD</sub> definition through the resin, enabling independent size variation of the gate overlap length (L<sub>OV</sub>) without altering the polysilicon gate length L. This technique offers a convenient method to modify the effective channel length (L<sub>eff</sub>), since  $L = L_{eff} + 2 * L_{OV}$ .



**Fig. 3:** TCAD simulation of the transistor morphology for different lengths of gate overlap on source drain.

Figure 3 displays the TCAD simulation results of the new MV transistor for different gate overlap lengths.

Trade-offs in electrical performance can be found between a transistor with low L<sub>OV</sub> overlaps and one with large L<sub>DD</sub> regions prone to Short Channel Effects (SCE). Indeed, with the increase in overlap, the threshold voltage (V<sub>T</sub>) decreases (See Fig.4.a), leading to an increase in both the ON current (I<sub>ON</sub>) (Fig.4.b) and the OFF current (I<sub>OFF</sub>) (Fig.4.c).

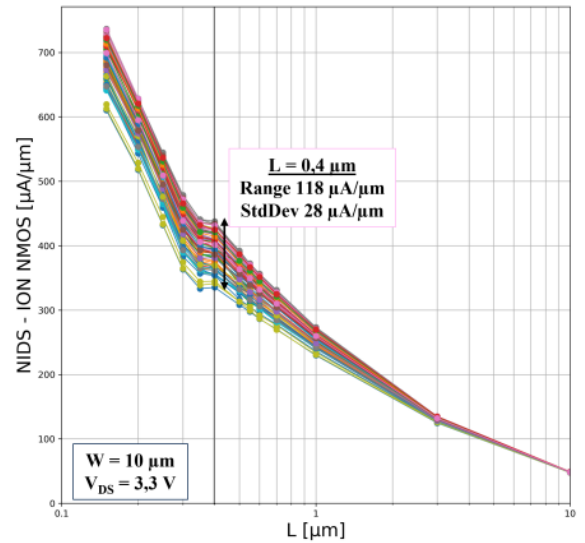


**Fig. 4:** Results of the study of the effects of gate-to-drain-source overlap on transistor performances: V<sub>T</sub> (a), I<sub>ON</sub> (b), I<sub>OFF</sub> (c), C<sub>OV</sub> (d).

However, this technique presents some challenges: the LDD implantation is no longer self-aligned on the gate, and instead relies on the alignment of its mask with the gate patterning mask. This deviation from the initial manufacturing process may lead to significant inter-wafer and intra-wafer electrical parameter dispersion [3]. To evaluate the dispersion, a misalignment of the two masks (overlay) was forced across a range of values (-30 nm; +30 nm).

Fig. 5 shows saturation current  $I_{ON}$  as versus the gate length  $L$  for several overlay values. The targeted size and electrical characteristics for this new transistor are: a gate length ( $L$ ) of 0.4  $\mu\text{m}$  and a width ( $W$ ) of 10  $\mu\text{m}$  and a  $V_T$  greater than 250mV along with a tight control of the SCE effect.

Investigation have been made at the circuit levels using Ring Oscillator (RO). Figure 4.d depicts the propagation delay of a three-stage RO versus the overlap length. The simulation integrates overlap capacitances values extracted from TCAD simulation and  $I_{ON}$  current measurements. The RO's minimum propagation delay occurs with a negative overlap length of -40 nm, with longer overlaps, we observe an increasing delay due to higher capacitances. Conversely, shorter overlaps reduce electrostatic gate control, lowering  $I_{ON}$  for the same bias.



**Fig. 5:** Measurement of saturation current  $I_{ON}$  as a function of gate length  $L$  for several values of LDD mask overlay and gate etching, from -30nm to +30nm.

In summary, this study presents the development of a novel zero-cost transistor designed for low-cost IoT applications. Its manufacturing process offers remarkable adaptability and flexibility in its characteristics. However, a potential concern lies in the risk of misalignment between the LDD implant and the gate, which may impact its performance. Ongoing research and optimization efforts aim to address this alignment issue and fully leverage the potential of this cost-effective transistor for IoT applications.

[1] D. Bol et al., "Can we connect trillions of IoT sensors in a sustainable way? A technology circuit perspective", IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, pp. 5-7, 2015.

[2] D.Chien et al, "Platform choices and design demands for IoT platforms: cost, power, and performance tradeoffs," IET Cyber-Physical Systems: Theory & Applications, pp. 70 – 77, 2016.

[3] "Influence of manufacturing variations in  $I_{DDQ}$  measurements: a new test criterion" Juan M. Díez and Juan C. López, [10.1109/DATE.2000.840854](https://doi.org/10.1109/DATE.2000.840854)