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Abstract

Wide bandgap (WBG) power semiconductors such as SiC and GaN devices allow for very fast switching speed, thus improving the overall efficiency and power density of power converters. Among the factors now limiting the switching speed, there is the parasitic inductance of the switching cell induced by power interconnections at packaging level, especially leadframe along with DBC layout and bonding wires. While important, optimizing power connexions reach some limits as long as the switching cell is closed with an external decoupling capacitor. A complementary approach is to integrate a RC snubber circuit directly inside the power module (PM) to shorten at most the switching cell inductive loop. This paper investigates the opportunity to integrate silicon monolithic RC snubber dies (SiRC), fully compatible with existing power modules assembly processes and operation. In this paper, several PM integrating different numbers of SiRC snubber are assembled and tested to assess the advantages on voltage overshoot and oscillations damping. A 3D modelling of the power module's inductive loop is also done to give comprehensive explanations of the remaining voltages overshoots and oscillations, and comment on the added value of such snubbers depending on the RC values.

Introduction

SiC power devices drastically improve power modules (PM) performances in terms of efficiency and power density, allowing much faster switching speed compared to Si semiconductors. These very fast voltage and current transitions come at the cost of an increase in the impact of parasitic impedances, especially the switching cell inductance causing voltage overshoot and ringing, thus being one of the most limiting factors for switching speed. Limiting this parasitic inductance has been the target of many researches focusing on novel packaging techniques and DBC layout optimization [1], due to the fact that the decoupling DC-link capacitors generally sit outside of the PM. A complementary approach discussed in this paper is to directly integrate a SiRC snubber inside the power module, as it is expected to reduce both power transistors turn OFF voltage overshoot and ringing. Such dies have been used in various papers such as [2], [3] or [4] showing great results for voltage overshoots reduction and oscillations damping. The possibility to switch faster to decrease switching losses was notably explored. However, existing prototypes were only designed with two variants: a reference power module without snubber and the same power module integrating one or several snubbers, giving a single point of comparison. In this paper, 4 different configurations of snubbers in addition to a reference module with no snubber are characterized to give a better understanding of the effect of the SiRC on the switching behaviour in both time and frequency domains, which will support snubber design guidelines.

This paper presents the SiRC technology considered in this work and its main characteristics in the next section. Then, the design of a power module prototype integrating one or several SiRC snubbers is described. The resulting gains in voltage overshoot and ringing are characterized experimentally for various parallel configurations of SiRC. The following section introduces a 3D modelling of the power module prototypes in order to analyse, in the frequency domain, the various high frequency interactions among components and parasitics in the power modules. A last section is dedicated to discuss the benefits and perspectives of the SiRC integration in Power Modules.

1 SiRC snubber

Power modules switching cell inductive loop minimization is limited by the closest decoupling capacitor connected to the power device. An easy way to limit the stray inductance is thus to have a decoupling capacitor placed as close as possible to the switching devices. To date, this approach remains difficult to implement directly inside power modules. Power modules operate at temperatures that are critical for high voltage ceramic capacitors with standard dielectric, significantly derating their lifetime and performances [5]. Thus, the integration of discrete capacitors could end up lowering the lifetime of PM. Also, integration and interconnects of traditional discrete capacitors such as ceramics adds manufacturing processes and costs. For these reasons, decoupling capacitors have mainly remained outside of power modules as a DC-link capacitor bank.
Silicon based RC snubbers address these issues by being fully compatible with power modules manufacturing processes and operation. These snubbers come in the form of a monolithic die that is soldered on the power module's

DBC and connected with bonding wires, as shown on Fig1. Its material composition is highly compatible with thermal stressors.
This paper will use SiRC dies from Murata shown in the zoom Fig1. These dies integrate a monolithic 1nF 5Ω series snubber network, with a DC breakdown voltage of 1,5kV. As for a SiC chip, the electrical terminals are located on each side of the die: the metallisation of the top side is in aluminium for the wire bonding process and the bottom side metallisation is adapted to soldering. The component shows very good thermal stability with at max 5mΩ/°C for the resistive part and a maximum of 2% total capacitance drift, up to 175°C. Some lower voltage components have been qualified at 250°C, which leaves good hope that future generations will be compatible with extended PM temperature ranges (220°C). The die size is 3.5x3.5mm² and the capacitance density is 0.18nF/mm². Next generations of component are expected to have significantly higher capacitance density, which will allow for components with higher capacitance value.

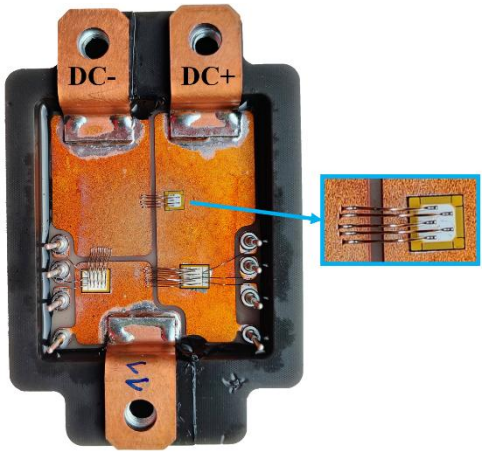

Figure 1: *Picture of a power module prototype integrating a SiRC monolithic device from Murata. Right: zoom on the SiRC device interconnects.*

2 Power module prototypes

To study and characterize the benefits of SiRC snubbers with respect to the values of Cs and Rs (series capacitance and resistance), several power modules prototypes integrating SiC MOSFETs were designed. Integrated power switches are made of a single 1200V 16mΩ SiC MOSFET die from ST. Freewheeling operation inside the switching cell is carried out by the body diode of the MOSFETs. Power module prototypes can integrate none or several of the previously described SiRC dies, up to 8. These PM designs allow us to assess the added value of the SiRC dies with respect to a reference PM without SiRC die, for several values of Cs and Rs.
The SiRC dies are directly soldered on the DC+ plane, and connected to the DC- plane with bonding wires. This makes decoupling close to the switching device possible, as illustrated in Fig 2.
Since the SiRC dies from Murata are only available for one Rs-Cs couple of values, being integrated in parallel in the PM, it only allows for certain equivalent values of snubber resistance-capacitance (Rse-Cse), as listed in Table 1.

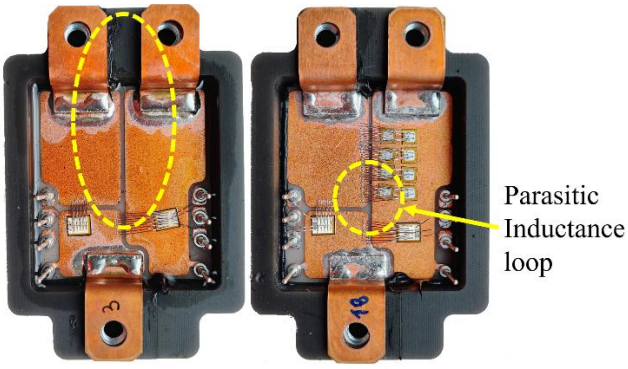

Figure 2: *Qualitative representation of the switching cell's inductive loop in a PM with no SiRC snubbers (left) and a PM with 8 SiRC snubbers (right)*

The power module prototypes used in this work are not specifically optimized with respect to interconnects with external components such as gate drivers and decoupling capacitors. Nevertheless, they are representative of state of the art of PM, although more optimized PM can be found. Our purpose here is not to propose a record-breaking PM but more to underline with a traditional but representative set up what can be expected from the integration of a SiRC snubber circuit.

Table 1: *Equivalent values of capacitance and resistance for a given number of parallel snubbers.*

Number of integrated SiRC	Equivalent resistance Rse (Ω)	Equivalent capacitance Cse (nF)
1	5	1
2	2.5	2
4	1.2	4
8	0.6	8

3 Double pulse test

The power modules prototypes switching performances are evaluated using the double pulse test. This test allows characterizing easily the switching behaviour of a switching cell configuration under various operating points, without the need for a source and load rated for high power, or the associated cooling system. In order to carry out a representative switching characterization, the driver and DC link PCBs are carefully designed.
The SiC MOSFETs are driven using UCC5390SC from Texas Instruments, with 10Ω of gate resistance for both sink and source currents. This comes in addition to the internal 1.1Ω gate resistance of the SiC MOSFETs. The drivers are supplied with +15V / -5V to enable a clean and fast switching. With this configuration, a switching speed of 30V/ns is obtained.
The driver board seen in Fig 3 is designed to keep the gate and measurement traces as low inductive as possible. A central cavity allows to see the dies during operation.
Some of the PM prototypes do not have any silicone gel, which make it possible to measure the switching voltage directly across the die when the measurement traces

impedance becomes too important, typically if the switching speed is increased. The probe is a TPP0850 800MHz probe from Tektronix (1.8pF input capacitance).
The DC-link capacitor bank is made of two 27uF foil capacitors, each with 4 terminals. The total ESL (equivalent series inductance) of the DC-link board is characterized to 21nH.

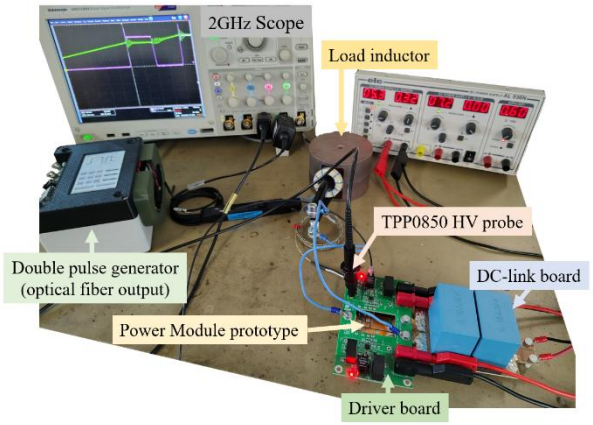

Figure 3: *Double pulse test measurement set up (high voltage power supply not shown)*

The drain-source voltage of the active MOSFET is measured during a turn OFF event with a 600V bus. The load inductor is charged to 80A before the switching event. A schematic of the test set up is shown in Fig 4.

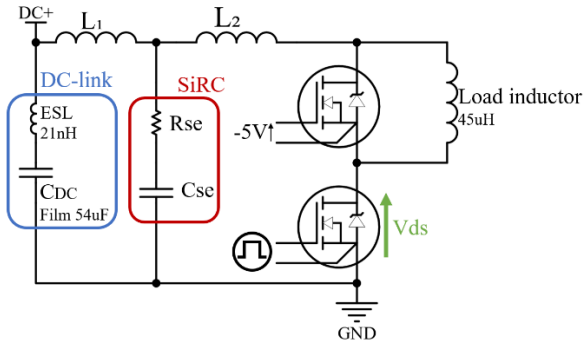

Figure 4: *Schematic of the double pulse test set up including switching cell's parasitic inductances L1 and L2*

The turn OFF voltage waveforms across the low-side MOSFET for the different snubber configurations are shown in Fig 5.
The addition of the snubber shows 3 effects on the turn OFF voltage waveforms: a reduction of the transient overvoltage, a damping of the oscillations and a decrease in the oscillation frequency. Despite these positive effects on the turn OFF switching behaviour, there remains a significant overvoltage, and noticeable oscillations.
The reasons for these overvoltages will be discussed in section 5. In particular, one can read in table 2 the values for voltage overshoot, damping ratio and oscillation frequency for each SiRC configuration. Unsurprisingly, more capacitance helps mitigating the voltage overshoot, while the decrease in resistance leads to less damping.

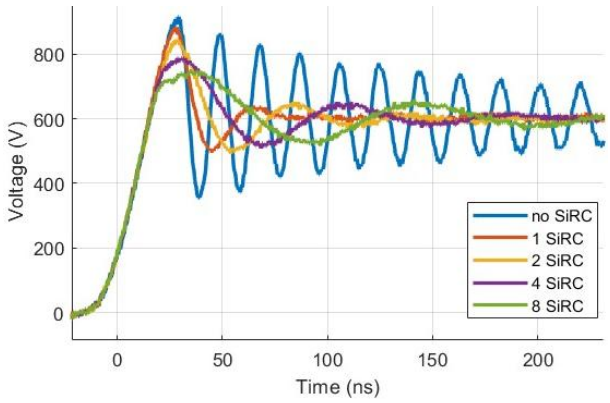

Figure 5: *Turn OFF drain-source voltage waveforms at 600V and 80A for different configurations of SiRC*

Table 2: *Voltage overshoots and oscillations damping for different snubbers configurations, double pulse test measurements (the damping ratio is calculated using the logarithmic decrement of the oscillations).*

Number of SiRC	Voltage overshoot	Damping ratio (ξ)	Oscillation frequency
0	316 V	0,02	52 MHz
1	284 V (-14%)	0,26	25 MHz
2	244 V (-21%)	0,15	18 MHz
4	188 V (-38%)	0,13	12 MHz
8	148 V (-50%)	0,10	9,2 MHz

4 3D modeling of the power module's inductive loop

A 3D meshed model of the power module prototype was done under Altair Simlab, using the PEEC solver. This model is used to derive the values of the parasitic inductances and resistances that appear between components and interconnects. Thus, it only models the DBC traces, power leads and wirebonds as geometric blocks of copper. The model is used as a transfer function. It includes different terminals as illustrated in Fig 7: there are 6 terminals for the drain, source and gate of each SiC MOSFETs, 8 for the + and – terminals of 4 SiRC dies and 2 for the DC+ and DC– power leads connection, where the DC link capacitor bank is connected. The transfer function can then be used in different simulation softwares, in which external components models can be connected to the terminals.
Terminals are modelled as equipotential surface regions, that are then connected to an external component model, as illustrated in Fig 6 for a SiRC chip.

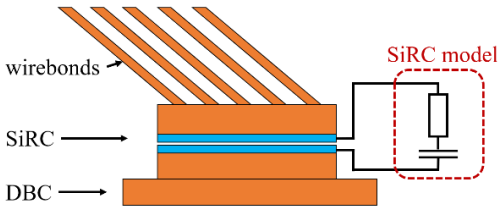

Figure 6: *Schematic view of the 3D modeling of a component, with meshed regions made of copper (orange), equipotential regions (blue) and the component's model added externally.*

It is then possible to run AC sweep or time domain simulations. Notably, by shorting the high side SiC MOSFET, and applying a current source through the drain-source of the low side one, the drain-source voltage of the low side MOSFET is the image of the power module's impedance seen by the active MOSFET. This simulation can be run for various SiRC configurations and DC link ESL over a wide range of frequencies. A schematic illustration describes the interactions between the models used for this simulation.

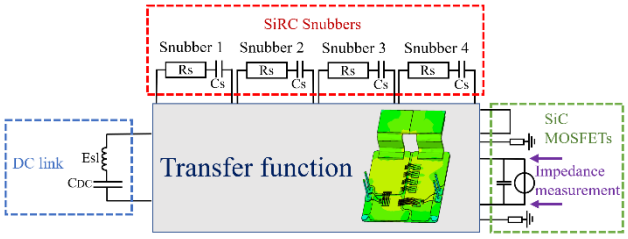

Figure 7: *Representation of the utilization of the 3D meshed model to obtain the power module prototype's impedance. The capacitor across the MOSFET terminal models Coss.*

To simulate the absence of a snubber chip, a large resistance value is placed across the corresponding terminals. Fig 8 shows that there are 4 spots to choose from to simulate a SiRC snubber. In order to correspond at best to our PM prototypes (see Fig 1), the variants integrating one or two snubbers used the spots located in the center of the power module's DBC trace.
The modeling results of the power module impedance will be shown and exploited in the next section.
When the simulation is run directly in Simlab, it is also possible to visualize the current densities in the power module prototype. Fig 8 shows how higher frequency currents harmonics will pass through the snubbers rather than the DC link, for two different frequencies.

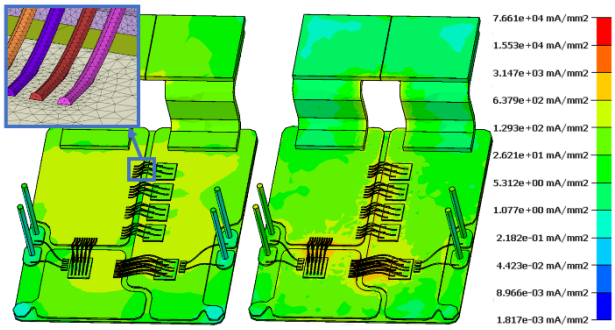

Figure 8: *Simulated current densities for a 1A sinewave at 1kHz (left) and 100MHz (right). Including a visualization of the meshing around a bonding wire (top left zoom).*

5 Frequency analysis and extraction of parasitic inductances

5.1 Power module prototype's impedance correlation with time response

The 3D model described in section 4 is used to obtain the power module prototype's impedance for different snubber configurations. The frequency representation of these impedance modeling are displayed in Fig 9. It can be seen that compared to the PM with no snubber (blue curve), the snubber introduces a new resonant frequency, noted 1 in Fig 9. This resonance implies the snubber capacitance Cse and the parasitic inductance formed by ESL+ L_1. Thus, L_1 is the parasitic inductance formed by a portion of the DBC traces and the power leads.
The other effect of the snubbers is the rise in frequency and damping of the resonance implying Coss. For the power module with no integrated snubber, the resonance noted 2 on Fig 9 occurs at 52MHz and has very low damping. For the power modules integrating one or several SiRC, this resonance noted 3 on Fig 9 occurs at about 180MHz, with a much greater damping.

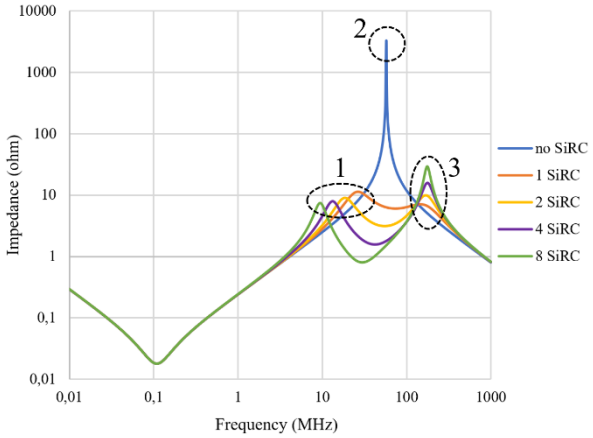

Figure 9: *Frequency domain power module prototype's impedance seen from the active MOSFET for different SiRC configurations.*

The reason for this frequency drift is the fact that in the case of the resonance noted 2 on Fig 9, Coss oscillates with ESL+L_1+L_2 while in the case of the resonance noted 3 on Fig 9, Coss only oscillates with L_2. Thus, L_2 is formed by the other portion of the DBC traces, bonding wires and the conducting MOSFET. It means that this resonance will be much harder to excite compared to the PM without snubber. And if oscillations do occur, they will be significantly more damped thanks to Rse as well as a higher Coss/L ratio, as seen from the relation between the damping ratio and RLC values (1).

$$\xi = \frac{R}{2} \cdot \sqrt{\frac{C}{L}} \qquad (1)$$

It is also possible to visualize the effect of the snubber Cse and Rse values on the PM impedance: Cse pulls the resonance frequencies lower as it rises, while Rse simply damps the resonance peaks.
To understand what causes the remaining voltage overshoots and oscillations seen Fig 5, it is important to identify which parasitic elements and components are resonating. It is seen in Fig 5 that the remaining oscillation frequencies vary with the value of Cse, meaning that the voltage overshoot and oscillations in PM integrating snubbers are caused by the resonance between L_1+ESL and Cse, as already pointed out in [6].
To extract the equivalent discrete parasitic inductances L_1 and L_2, the measured and simulated resonance frequencies are used.

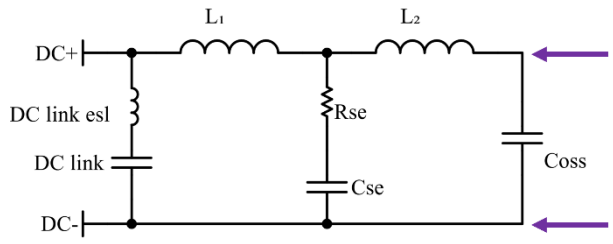

Figure 10: *Discrete modeling of the PM. The arrows represent the spot of measurement of the PM impedance as in Fig 7, which also corresponds to the spot of drain-source voltage measurement.*

Using the resonance frequencies measured during the double pulse test and the known values the equivalent capacitance of the snubber Cse, (2) is used to deduce L_1 (ESL is subtracted). The same calculation is done using the resonance frequencies obtained through the PM impedance simulation.

$$L_1 = \frac{\sqrt{1-\xi^2}}{(2\pi \cdot f_{resonance})^2 \cdot Cse} \qquad (2)$$

Table 3: *Calculated parasitic inductance L_1 from measured and simulated resonance frequencies.*

Cse	Measured parasitic inductance L_1	Simulated parasitic inductance L_1
1nF	15nH	14nH
2nF	13nH	14nH
4nF	16nH	14nH
8nF	13nH	12nH

The placement of the SiRC die on the DBC traces varies from one PM prototype variant to the other. Thus, while L_1+L_2 remains constant, the individual values of L_1 and L_2 vary.
A measurement of L_1+L_2 is also done by connecting a known capacitance (low ESL ceramic) to the DC- and DC+ power leads of the PM and letting it oscillate with L_1, L_2 and its own ESL (with both SiC MOSFETs turned on). This measurement gave a result of 23nH. Thus, L_2 can be estimated to be 7 to 10nH depending on the PM variant. L_2 could also have been measured using its resonance with Coss, but the high variability of Coss to bias voltage would make such a measurement unreliable (with voltage swings from 400 to 900V, Coss is expected to vary from 180pF to 250pF).
While useful, the approach of discretising the parasitics contains inherent approximation, such as neglecting the mutual inductances or the skin effect.

5.2 Real time simulation using a discrete parasitics model

The downside to the 3D modeling of the PM prototype described in section 4 is that the 3D and meshing work would have to be redone for every PM design that one could want to evaluate. Thus, a time domain simulation is developed using the discrete modeling seen in Fig 10. This will allow to run simulations for PM with different parasitics characteristics and to have more general conclusions.

The simulation consists in a double pulse test simulation, using the spice model of the SiC MOSFETs. The values for L_1 and L_2 obtained in the previous section are used as a starting point, and are then tuned to match at best the measured oscillations frequencies. The time domain simulation results can be seen in Fig 11 where experimental turn OFF voltage waveforms are compared with simulation turn OFF voltage waveforms, after tuning the parasitic elements.

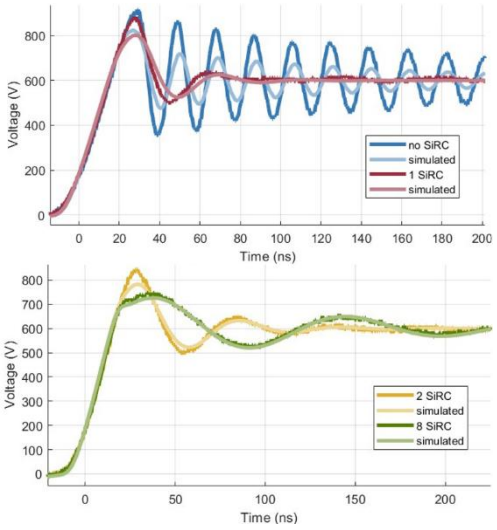

Figure 11: *Measured and simulated turn OFF voltage waveforms at 600V 80A. Parasitic inductances are tuned to L_1=13nH, L_2=6nH and ESL=21nH*

Great correlations on the oscillation frequency and damping comforts the utility of a discrete modeling approach of the switching cell.
The spice simulation reaches some limits when it comes to precisely predicting the voltage overshoot, which heavily depends on the current commutation speed that cannot be adjusted externally. However, it still provides an accurate prediction of the reduction of voltage overshoots, relative to the scenario where no snubber is integrated. Thus, this simulation can be used to test more scenarios of snubber Rse Cse values as well as PM parasitic inductances.

6 Discussion on the benefits of integrating SiRC snubbers in a power module

6.1 Optimization of the SiRC Cse-Rse values

From the previous section, it can be seen that while the SiRC snubber circuit can successfully mitigate the oscillations caused by Coss and its closest parasitic inductance (L_2), the oscillation between the snubber capacitor and L_1+ESL can still be responsible for significant voltage overshoots and ringing. Thus, while the snubber can provide significant improvements (-50% in voltage overshoot for our PM prototype integrating 8 SiRC), it remains necessary to make both the power modules interconnections and film DC-link capacitor bank as low inductive as possible to enable the best switching performances. Moreover, having a higher snubber capacitance value Cse will allow

both a better reduction of overvoltages, and a better damping of the oscillations. This also allows to use a lower value for the resistance. Regarding the resistance value, there is a sweet spot to hit: if the resistance is too low, it will let Cse and L_1+ESL having important voltage swings and thus voltage overshoots. It also implies that the oscillations are highly underdamped, which can cause EMI issues. If the resistance is too high, the currents charging Cse will induce a significant voltage across Rse, that adds to the voltage swings across Cse. The value of Rse also affects the phase of the oscillations to the voltage rise. [7] describes these effects and shows that the lowest voltage overshoot is obtained for a damping ratio of 0,25 which corresponds to equation (3).

$$Rse_{optimal} = \frac{1}{2} \cdot \sqrt{\frac{L_1}{Cse}} \qquad (3)$$

Fig 12 compares the PM prototype's 8 SiRC configuration to the same PM with Rse calculated for the lowest voltage overshoot.

It should be pointed out that this way of selecting Rse and Cse can only be valid if the resonant pole between Coss and L_2, that still exists, can be neglected. This implies that L_2 should be kept as low as possible, and the switching speed may have to be limited to avoid exciting the pole between Coss and L_2. Overwise, this resonance may cause overvoltages greater than the ones caused by Cse and L_1+ESL. This effect can be seen Fig 12 where the switching speed increases enough to cause oscillations between Coss and L_2.

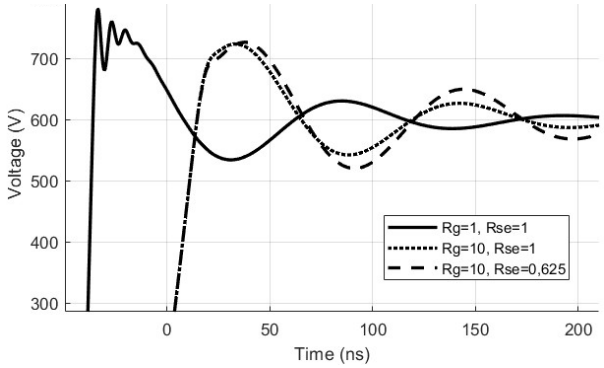

Figure 12: *Simulated turn OFF voltage waveforms at 600V 80A for different values of Rg, Rse (in Ω) and Cse=8nF*

Future generations of components will enable higher capacitance value per surface area, which will overall make the integration of SiRC snubbers more benefitable in term of voltage overshoots, as seen in table 4 with a hypothetic 20nF snubber. While in the case of our PM prototype the voltage overshoot was successfully reduced by a factor of 50%, the 8 snubbers in parallel populate an important part of the surface area on the DBC traces. If the power module had been designed without this constraint, it is very likely that the switching cell inductance could have been significantly reduced.

6.2 SiRC positive impact dependence on the power module parasitics

Finally, because the PM prototype and DC-link board were overall not optimized regarding the switching cell inductance, it is important to confirm the interest of the SiRC snubbers in the situation of a PM and DC link board optimized for low parasitic inductances. A PM with the following parasitics is simulated: ESL=8nH, L_1=10nH and L_2=3nH. It is then compared to the PM prototype. The resistance of the snubber is calculated in each case using (3). Table 4 summarizes the relative gains obtained on voltage overshoot. Since Rse is calculated for the optimal voltage overshoot, the damping ratio for these cases is always 0.25. The optimized PM still benefits from the snubber in comparable amount to the PM prototype. Thus, a power module that aims at achieving the best switching performances possible will benefit from a clever, low inductive layout, interconnect and DC-link as well as from the integration of SiRC snubbers.

Cse	PM prototype voltage overshoot (ESL=21nH, L_1=13nH and L_2=6nH)	Low parasitics PM voltage overshoot (ESL=8nH, L_1=10nH and L_2=3nH)
0nF	225V	134V
8nF	123V (-45%)	82V (-39%)
20nF	83V (-63%)	58V (-57%)

Table 4: *Simulated turn OFF voltage overshoots at 600V 80A for the PM prototype and a power module with optimized parasitic inductances for different snubber values.*

The improvements observed in voltage overshoot and ringing could lead to extra gains in switching speed, and reduce the commutation losses as shown in [2] and [3]. Another option could be to reduce the active device voltage ratings. Overall, a reduction of the stressors on the devices could show positive impacts on the device's lifespan.

Conclusion

In this paper, the effects of the integration of a Silicon RC (SiRC) monolithic snubber chip on voltage overshoots and ringing was studied. Because of the materials used, these chips are compatible with power modules existing manufacturing processes and operation, as they can be soldered on the DBC traces and connected with bonding wires, and show very good thermal stability. Thus, the SiRC chips can be integrated close to the switching elements and provide a low inductive path for high frequency currents. Several power modules prototypes were manufactured, integrating different amounts of SiRC snubbers in parallel, up to 8. These power modules prototypes were characterized through double pulse test measurements. The power module integrating 8 snubbers showed a reduction of 50% of the voltage overshoot, and every power module integrating a snubber provided a very efficient damping of the oscillations. A 3D meshed model of the power module prototype was done to obtain the simulated impedance of the power module prototype. These impedance curves supported a frequency analysis that allowed to find the intrinsic parasitic inductances of the power module prototype, and propose a model using discrete components to model a

switching event and explore different scenarios of snubbers and power modules parasitics. Finally, the advantages of the integration of SiRC inside a power module were discussed to provide a comprehensive summary of their interest. Notably, it was pointed out that SiRC heavily benefit from low parasitic inductances. Thus, there is no contradiction between integrating SiRC and optimizing PM DBC traces, interconnects and DC-link board ESL. The parasitic inductance should not be neglected because of the integration of SiRC snubber. The next generations of components will allow a better mitigation of overvoltages for a diminished surface area thanks to their higher capacitance density.

Acknowledgement

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