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# Characterization of a Fault-Tolerant RISC-V SoC in an SRAM-based FPGA under Proton Irradiation

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**Abstract**

Radiation-induced faults pose significant challenges for safety-critical systems operating in harsh environments such as space and avionics. Among these effects, Single-Event Upsets (SEUs) can impact both the logic and configuration memories of SRAM-based FPGAs, potentially compromising system functionality and reliability. The Hardened RISC-V System-on-Chip (HARV-SoC) incorporates a fault-tolerant soft-core processor designed with in-circuit hardening techniques such as Triple Modular Redundancy (TMR) and Hamming Error-Correcting Code (ECC), combined with structured fault-observability mechanisms to enhance system resilience under radiation. This work presents a characterization of proton irradiation for the HARV-SoC implemented on an Xilinx Artix-7 FPGA, aiming to investigate the susceptibility of both the processor architecture and the FPGA configuration memory to radiation-induced faults. The experiments were conducted using proton beams at different energies to assess the impact of radiation on functional correctness and recovery behavior, providing insights into the reliability of SRAM-based FPGA platforms for space-grade and mission-critical applications.

**Index Terms**

Systems-on-Chip, Fault Tolerance, Single-Event Effects, RISC-V.

## I. Introduction

Safety-critical systems deployed in domains such as space and avionics must maintain dependable operation despite radiation-induced faults. Exposure to energetic particles, including neutrons, protons, and heavy ions, can trigger Single-Event Effects (SEEs) that affect both combinational and sequential logic, potentially compromising system stability. Among these effects, Single-Event Upsets (SEUs) are particularly relevant, as they induce bit flips in memory structures or configuration storage, silently corrupting data or altering circuit behavior [1], [2]. As embedded systems increasingly use programmable logic devices, assessing their radiation sensitivity and quantifying mitigation techniques have become essential.

FPGAs play a prominent role in these applications due to their design flexibility and reuse. However, SRAM-based FPGAs are especially susceptible to configuration memory upsets, as their logic and routing resources rely on volatile SRAM cells that are highly sensitive to particle strikes [3], [4]. Upsets in this memory can modify the implemented circuit, degrade functionality, or even cause persistent system hangs if not mitigated by mechanisms such as scrubbing and built-in Error-Correcting Codes (ECC). Consequently, systems deployed on SRAM-based platforms require architectural hardening, protected memory structures, and system-level monitoring to maintain dependable operation in radiation environments.

The Hardened RISC-V System-on-Chip (HARV-SoC) addresses these challenges by combining a fault-tolerant RISC-V core with structured error reporting and redundancy mechanisms. The HARV core implements Single-Error Correction, Double-Error Detection (SECDED) in key memory elements, while Triple Modular Redundancy (TMR) is applied to critical datapath and control components. In addition to hardening, HARV-SoC provides detailed observability through custom RISC-V exceptions and memory-mapped registers that capture radiation-induced events. Previous evaluations of HARV-SoC implemented on Flash-based FPGAs, whose configuration memory is intrinsically more resilient, have demonstrated the robustness of this architecture under irradiation [2], [5], [6].

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Several works have investigated the fault behavior of RISC-V soft processors under radiation. Studies have evaluated the effectiveness of mitigation techniques such as ECC, TMR, and scrubbing when applied to processors like NOEL-V, VexRiscv, NEORV32, and RI5CY, primarily on SRAM-based FPGAs and under neutron or single-energy proton irradiation [7]–[11]. These contributions have advanced the understanding of fault tolerance in soft-core systems and provided insights into processor-level and system-level mitigation, but typically focus on a fixed radiation condition.

In this work, we extend the characterization of HARV-SoC by evaluating its implementation in an SRAM-based FPGA under proton irradiation. We analyze its behavior under different proton energies and assess the impact of radiation-induced faults in the programmable logic and the configuration memory. Experimental results include a detailed evaluation of observed events across processor-level and configuration memory, enabling comparative analysis of fault susceptibility and the effectiveness of the implemented mitigation strategies.

The paper is organized as follows. Section II describes the HARV-SoC architecture and its fault-tolerance mechanisms. Section III presents the proton irradiation experiment, detailing the irradiation facility, the system implementation, and the physical board setup. Section IV reports the experimental results and discusses the observed radiation-induced events. Finally, Section V concludes the paper.

## II. HARV-SoC

The HARV-SoC is a fault-tolerant RISC-V System-on-Chip (SoC) designed for reliable operation in radiation-prone environments. It integrates the HARV processor with communication interfaces, memory controllers, and monitoring modules interconnected via an AXI4-Lite bus. The architecture prioritizes balanced reliability and flexibility, enabling implementations across multiple FPGA families and technologies.

At its core, the HARV processor implements a multi-cycle RV32I architecture [12], supporting standard Control and Status Registers (CSRs), compressed instructions, multiplication, and vector extensions. Fault tolerance is achieved through the combined use of ECC and TMR. The register file, program counter, and instruction register are protected with SECDED ECC. In contrast, the control unit, ALU, and critical CSRs, including mtvec, mie, and mstatus, are protected using TMR with self-correction [13].

In addition to hardening techniques, the processor provides detailed fault awareness via a structured error-reporting mechanism. Radiation-induced faults generate custom RISC-V exceptions, and the associated memory-mapped registers expose contextual information, including event identifiers, error type, corrupted data, and application state at the time of the fault. This observability mechanism helps the software layer differentiate correctable from uncorrectable events and implement recovery policies accordingly.

Beyond core-level protection, HARV-SoC incorporates system-level reliability features, including ECC-protected data memory interfaces, peripheral access timeouts, a reset controller, and a watchdog timer to recover from processor hangs. Error reports originating from memory controllers or external peripherals are forwarded to the HARV processor via an external event interface, ensuring that system-level anomalies are also detectable at the architectural level.

The SoC was also designed to support different FPGA technologies. While Flash-based FPGAs offer greater robustness in configuration memory, SRAM-based FPGAs require additional monitoring due to their greater susceptibility to configuration memory upsets. For this reason, HARV-SoC integrates vendor-specific scrubbing and configuration-memory reporting structures whenever available. In Xilinx SRAM-based devices, the integration of the scrubbing enables real-time detection of correctable and uncorrectable configuration-memory errors, CRC mismatches, and frame-level parity events, which allow system-level analysis and response [14].

Overall, the combination of architectural hardening, system-level event monitoring, and configuration-memory protection makes HARV-SoC a suitable platform for reliability studies. In this work, we extend its evaluation by integrating the SoC into a tailored design implemented on a Xilinx Artix-7 SRAM-based FPGA, enabling investigation of previously unexplored radiation-induced effects induced by protons. By exposing the system to proton irradiation at different energies, we assess the susceptibility of both the processor and the configuration memory, providing complementary insights into the architecture's behavior when deployed on a technology with higher intrinsic sensitivity.

## III. Radiation Experiment

This section presents the experimental setup used to evaluate the HARV-SoC under proton irradiation. We describe the irradiation facility, the system implementation tailored for this test, followed by details on the physical board setup and the benchmark executed.

### *A. Irradiation Facility*

We performed the proton irradiation experiment at the Proton Irradiation Facility (PIF) of the Paul Scherrer Institute (PSI) in Switzerland. This facility is used to test spacecraft components and to generate representative proton spectra similar to those encountered in space. According to the energy range suggested in [15], we selected the following

proton energies for testing: 50, 100, 150, and 200 MeV. The primary proton energy (200 MeV) was degraded using copper plates introduced in the beam path to generate the other required energies. We used an average proton flux of approximately $4.8 \times 10^6$ p/cm$^2$/s for the main test runs.

### *B. System Design*

Fig. 1 presents the architecture implemented on the Xilinx Artix-7 FPGA for the proton irradiation experiment. The design integrates the HARV-SoC with the necessary peripheral and monitoring components to support program execution, error detection, and system observability during irradiation.

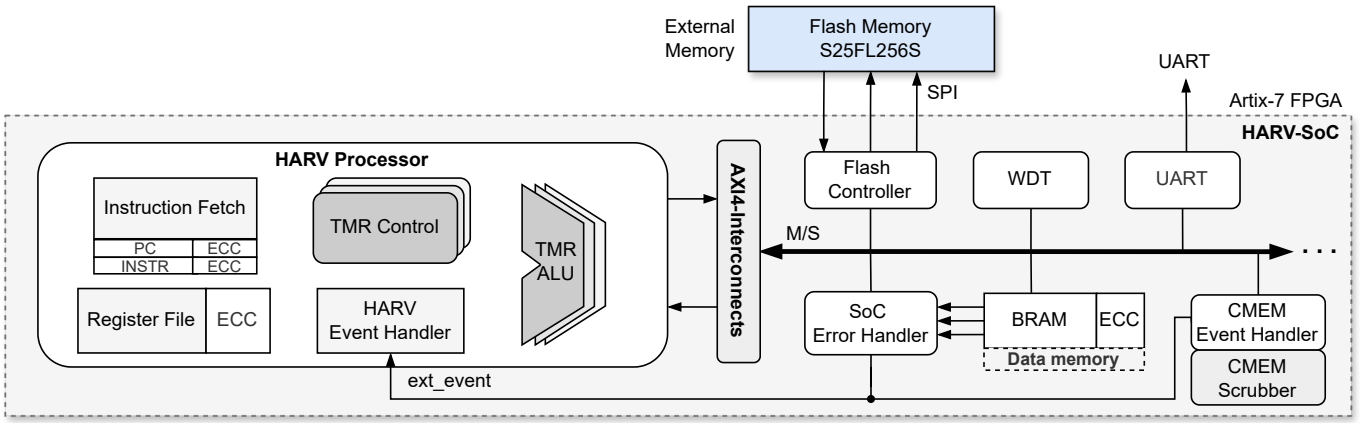


Fig. 1. System design for the experiment using HARV-SoC.

In this implementation, the HARV-SoC communicates with its internal modules via an AXI4-Lite interconnect, providing a lightweight, deterministic interface between the processor, memory blocks, and peripheral components. We used an external 32 MByte Flash memory device (S25FL256S) to store both the FPGA bitstream and the executable program for the HARV processor. We manage the access to this device by a standard SPI Flash Controller, which performs the required transactions to fetch instructions and data from the Flash when needed. The on-chip BRAMs of the FPGA serve as the HARV data memory. These memories are protected using Hamming SECDED ECC, allowing correction of single-bit flips and detection of double-bit upsets. This protection is essential for mitigating radiation-induced faults in programmable logic and preventing their propagation to the processor state.

Since the Artix-7 relies on SRAM configuration memory, which is highly sensitive to radiation-induced faults, the system integrates the AMD Xilinx FRAME_ECCE2 scrubbing primitive. In this work, we instantiate the component as the CMEM Scrubber, which monitors configuration frames at runtime. This block provides real-time information about correctable and uncorrectable configuration memory upsets, including single-bit upsets (SBU), double-bit upsets (DBU), CRC mismatches, and frame-level parity errors. To make these reports accessible, we implemented a dedicated CMEM Event Handler. This module captures the scrubber outputs and forwards them to the HARV processor using the exact event-signaling mechanism as the SoC Error Handler.

Alongside configuration memory monitoring, the system also integrates additional system-level fault reporting. The SoC Error Handler generates exceptions for internal BRAM events (single- and double-bit upsets) and for bus-access timeouts from peripherals. All these event sources are propagated to the processor via its existing external event interface, allowing the application to distinguish between processor, memory, and configuration-memory errors and report them.

Together, the CMEM Event Handler, SoC Error Handler, and the HARV Event Handler provide comprehensive observability of radiation-induced faults within the design. This level of visibility is essential for evaluating how user logic and configuration memory behave under irradiation, enabling the characterization presented in the following sections.

### *C. Board setup*

Fig. 2 shows the physical setup used during the irradiation campaign. The system is implemented on the Trenz TE0725 System-on-Module (SoM), which integrates the Xilinx Artix-7 XC7A35T FPGA along with the necessary power and I/O infrastructure. The external 32-MByte SPI Flash memory (S25FL256S), used to store the FPGA bitstream and the program executed by the HARV processor, is also visible on the module and is located in proximity to the FPGA package.

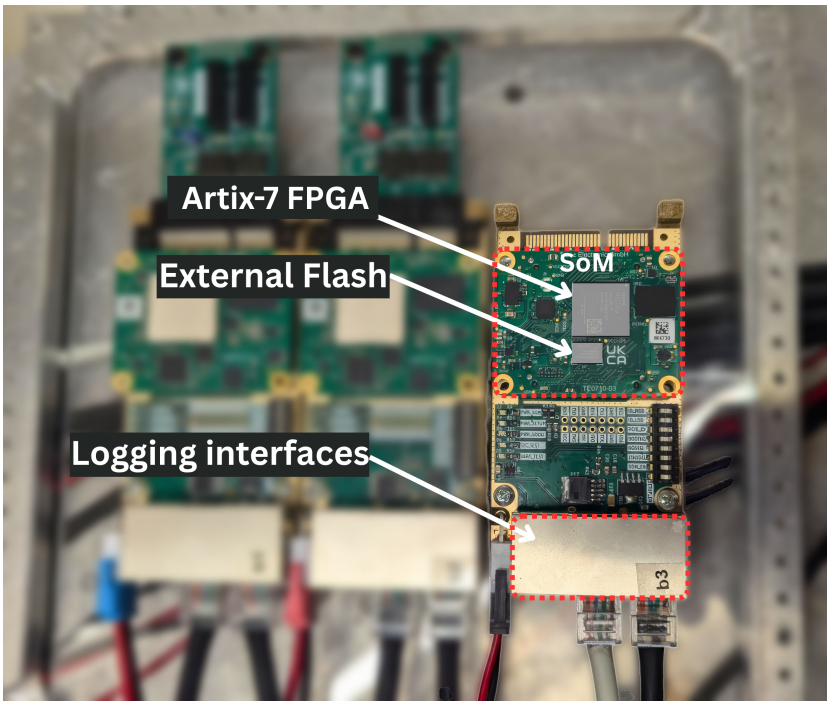


Fig. 2. Board setup for irradiation with the Artix-7 SoM.

Although the FPGA and the external Flash memory are located close to each other on the board, only the FPGA was intentionally exposed to the proton beam. We adjusted the irradiation area so that the beam covered only the FPGA die, ensuring that the programmable logic and configuration memory, our primary focus, were irradiated. This setup prevented external components, including the Flash memory and supporting circuitry, from being directly exposed, thereby avoiding secondary effects and ensuring that all observed events originated exclusively from faults in the FPGA.

To sensitize the system during irradiation, we executed the CoreMark benchmark, which combines representative embedded workloads such as list processing, matrix operations, state-machine transitions, and CRC computations [16]. The benchmark was configured to run continuously so that any radiation-induced event could be monitored throughout execution. Due to limited beam time and the facility's experiment scheduling, we tested a single board in this campaign.

## IV. Experiment Results

This section presents the results of the proton irradiation experiment, covering the resource utilization of the design, the reliability analysis based on the observed radiation-induced events, and a brief discussion of the main findings.

### *A. Synthesis results*

We implemented the system using the AMD Vivado 2024.2 tool, and Table I summarizes the resulting resource utilization for the Artix-7 XC7A35T device. The complete design occupies a modest portion of the FPGA, demonstrating the feasibility of deploying the HARV-SoC with its integrated hardening and monitoring mechanisms on a low-end SRAM-based FPGA. Logic and memory usage remain well within device limits, even with added components for event handling and configuration monitoring.

From the resource usage presented, approximately 71% of all Look-Up Tables (LUTs) and Flip-Flops (FFs) used in the design correspond to the HARV processor itself, reflecting the cost of the hardening applied to its datapath, control logic, and ECC-protected registers. The remaining resources are distributed across the SoC components, including peripheral interfaces, the AXI-Lite interconnect, data memory, the SoC Error Handler, and the CMEM Event Handler. These modules support communication, memory access, and fault awareness, and they occupy a small portion of the total area. This distribution highlights that the processor core is the dominant contributor to logic utilization, while other mechanisms add relatively modest overhead.

TABLE I
Synthesis results for the implemented system

| Component | Slice LUTs | Slice Reg. | BRAMs | LUTRAMs |
|---|---|---|---|---|
| HARV-SoC | 6,111 | 5,085 | 18 | 6 |
| **Available** | **20,800** | **41,600** | **50** | **9600** |
| Utilization | 29.38% | 12.22% | 36% | 0.06% |

In this configuration, the maximum operating frequency for the hardened design on the Artix-7 device was 51 MHz, accounting for all timing constraints introduced by the ECC-protected memories, TMR logic blocks, and system-level monitoring modules. The power analysis reported by the synthesis tool indicates a total dissipation of 241 mW, including both static and dynamic power components.

### *B. Irradiation Results*

During the experiment, several faults were observed, specifically in the configuration memory. For each proton energy, the total accumulated fluence with effective testing was calculated to $5\times10^9$ p/cm$^2$. We report the observed events for both the HARV-SoC and the configuration memory, along with the corresponding cross-section (XS) metrics calculated from events at each energy. Table II summarizes the radiation-induced events observed in the configuration memory.

The event count represents the total number of configuration-memory upsets accumulated over the irradiation campaign, combining results from all tested energies (50, 100, 150, 200 MeV). The observed events were corrected or not, depending on the type of error and the scrubber's operational status.

TABLE II
CMEM Events classification for the Artix-7 design under proton irradiation

| CMEM Component | Events | XS [cm$^2$/device] | | | |
|---|---|---|---|---|---|
| | | **50 MeV** | **100 MeV** | **150 MeV** | **200 MeV** |
| cram_sbu_ev | 745 | $4.5\times10^{-8}$ | $3.6\times10^{-8}$ | $3.1\times10^{-8}$ | $3.6\times10^{-8}$ |
| cram_dbu_ev | 48 | $1.6\times10^{-9}$ | $2.6\times10^{-9}$ | $3.0\times10^{-9}$ | $2.4\times10^{-9}$ |
| cram_crc_ev | 0 | - | - | - | - |
| cram_par_ev | 0 | - | - | - | - |
| **Run parameters** | | | | | |
| Flux [p/cm$^2$/s] | | $4.8\times10^6$ | $5.1\times10^6$ | $4.8\times10^6$ | $4.4\times10^6$ |
| Fluence [p/cm$^2$] | | $5.0\times10^9$ | $5.0\times10^9$ | $5.0\times10^9$ | $5.0\times10^9$ |
| Dose [rad] | | $7.9\times10^2$ | $4.7\times10^2$ | $3.5\times10^2$ | $2.9\times10^2$ |

The results in Table II show that the majority of configuration memory events (745) are single-bit upsets (cram_sbu_ev), which are detected and corrected by the FRAME_ECCE2 component, allowing the application to continue execution without interruption. In addition, the scrubber reports other types of correctable faults, including CRC mismatches (cram_crc_ev) and parity bit errors (cram_par_ev). In this experiment, no events were observed in these components. For the (cram_sbu_ev) events, the cross sections between different energies do not change significantly, presenting an average cross section of $3.7\times10^{-8}$ cm$^2$/device.

Additionally, the CMEM Event Handler captured uncorrectable double-bit upsets (cram_dbu_ev) and forwarded them to the processor to enable fault awareness. Since they are not correctable, these errors compromise the integrity of the configuration memory, leading to incorrect circuit behavior. Upon detection, HARV triggered a reprogramming process via Xilinx's Internal Configuration Access Port (ICAP), restoring the FPGA's original configuration. Since these 48 faults forced a reconfiguration cycle, each instance represents an application error for this system. Table II shows the XS for each energy.

Table III summarizes the faults detected directly in the HARV-SoC logic during the irradiation campaign. These events correspond to errors reported by the processor's fault-awareness mechanisms, including those originating from the ALU, the register file, and the external memory interface. As shown in the table, not all proton energies produced observable faults in the processor, and the events that did occur were limited to only a few of the monitored components. Several other blocks of the HARV-SoC provide observability for radiation-induced faults, yet no errors were recorded in those structures throughout the experiment.

TABLE III
HARV events classification for the Artix-7 design under proton irradiation

| HARV-SoC Component | Events | XS [cm$^2$/device] | | | |
|---|---|---|---|---|---|
| | | **50 MeV** | **100 MeV** | **150 MeV** | **200 MeV** |
| alu event | 4 | $2.0\times10^{-10}$ | $4.0\times10^{-10}$ | $2.0\times10^{-10}$ | - |
| ext. memory | 4 | $2.0\times10^{-9}$ | - | $6.0\times10^{-10}$ | - |
| register file | 2 | - | $2.0\times10^{-10}$ | - | $2.0\times10^{-10}$ |
| **Run parameters** | | | | | |
| Flux [p/cm$^2$/s] | | $4.8\times10^{6}$ | $5.1\times10^{6}$ | $4.8\times10^{6}$ | $4.4\times10^{6}$ |
| Fluence [p/cm$^2$] | | $5.0\times10^{9}$ | $5.0\times10^{9}$ | $5.0\times10^{9}$ | $5.0\times10^{9}$ |
| Dose [rad] | | $7.9\times10^{2}$ | $4.7\times10^{2}$ | $3.5\times10^{2}$ | $2.9\times10^{2}$ |

When comparing Tables II and III, most radiation-induced faults occurred in the configuration memory rather than in the programmable logic of the HARV-SoC. Even though single-bit upsets were corrected in both domains, their high frequency reinforces the need for protection mechanisms to avoid accumulation or undetected propagation. Additionally, double-bit upsets were significantly more frequent in the configuration memory and directly triggered system reprogramming, highlighting their critical role in overall system reliability.

In addition to monitoring radiation-induced events in the processor and configuration memory, the experiment included a mechanism to detect system-level failures. The HARV-SoC was continuously monitored to verify if it would regularly produce output data; thus, a lack of activity for more than 6 minutes was considered as an indicator of a processor hang. In such a case, a manual power cycle would be required to restore regular operation. Throughout the proton irradiation campaign, no system-level failures of this type were observed, and the processor remained responsive across all tested energies.

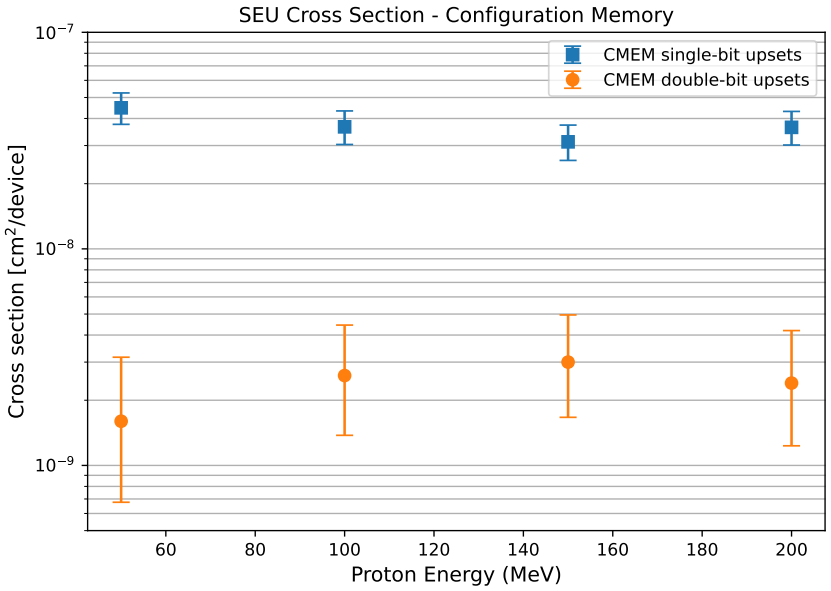


Fig. 3. SEU cross sections for the configuration memory proton irradiation tests. The error bars represent a 95% confidence interval with a 10% uncertainty in beam fluence.

Fig. 3 illustrates the XS obtained for the configuration memory events, complementing the data presented in Table II. The plot shows SEU cross-sections for both single-bit and double-bit upsets across the tested proton energies (50, 100, 150, and 200 MeV). The error bars represent the 95% confidence interval, incorporating a 10% uncertainty in the beam fluence. This graphical view highlights the relative stability of the SBU cross-section with energy, as well as the lower occurrence and higher variability of DBU events.

An additional observation from the configuration-memory results is that the XS remain relatively stable across the tested proton energies, with no strong energy dependence within the 50–200 MeV range. A slight tendency toward higher XS values at lower energies is evident, though the variations are subtle and insufficient to indicate a clear

trend. An assessment at lower energies would require dedicated characterization, as device technology and the balance between direct and indirect proton ionization can significantly influence SEU rates [17], [18]. It is worth noting that using copper degraders to obtain intermediate energies may broaden the proton energy spectrum, especially at lower settings, thereby increasing energy straggling. This dispersion can enhance the contribution of direct ionization mechanisms and may partially explain the mild saturation-like behavior observed in the XS curves [19].

### *C. Discussion*

The results from proton irradiation show a clear distinction between the number of events observed in the configuration memory and those detected in the HARV-SoC logic. As expected for SRAM-based FPGAs, configuration memory exhibited significantly higher susceptibility, with SBU counts one to two orders of magnitude larger than those reported by the processor's internal monitors. In contrast, only a small number of logic-level events were captured by the HARV's processor, affecting a limited set of components.

A previous irradiation campaign using the same system was conducted under neutrons at the ChipIr beamline [20]. In that study, the device was exposed for a more extended period at a higher neutron flux, accumulating fluences on the order of $10^{12}$ n/cm$^2$. Under these conditions, a substantially larger number of events were detected in the configuration memory and in the processor. The total accumulated fluence in the current experiment reached approximately $10^9$ p/cm$^2$, since higher particle fluence was not feasible in this test campaign, which in turn influenced the total number of observable events. Despite the different radiation sources and experimental conditions, the XS values obtained in both works show strong consistency, particularly for configuration-memory SBUs, which remained within the same $10^{-8}$ cm$^2$/device range. This is aligned with SER data reported by Xilinx for the same technology node [4], reinforcing the reliability and reproducibility of the HARV-SoC behavior across different test environments. Some effects observed under neutron stress, such as system-level failures requiring power cycling, did not manifest here, even though the system included specific monitoring mechanisms to detect such conditions. With more prolonged exposure, it is reasonable to expect additional fault types to emerge, including more events in the HARV processor. Therefore, the absence of specific failure modes in this campaign does not imply immunity; rather, it reflects the limited statistical window afforded by the available beam time.

Overall, the proton irradiation campaign shows that the HARV-SoC remained stable throughout all exposures, with configuration memory as the dominant source of radiation-induced events, and processor upsets were rare. The system maintained regular operation even in the presence of configuration upsets, mainly due to the continuous scrubbing and reprogramming mechanism, which prevented the device from entering an unrecoverable failure state or requiring a power cycle. Together with the observations from the neutron campaign, these results indicate consistent cross-section behavior across different particle types and confirm the effectiveness of the HARV-SoC mitigation strategies. This reinforces the system's suitability for applications requiring reliable operation under radiation and highlights the importance of complementary irradiation studies to build a complete reliability profile.

## V. Conclusion

This work presented a proton irradiation characterization of the HARV-SoC implemented on a Xilinx Artix-7 SRAM-based FPGA, evaluating its behavior under four proton energies and using the system's architectural hardening and event-monitoring infrastructure to capture radiation-induced effects. The results showed that configuration-memory upsets dominate the fault population, particularly single-bit upsets. At the same time, processor-level events were significantly less frequent and limited to a small subset of internal components. No system-level failures were observed during the campaign, and the system remained operational throughout exposure, supported by the FPGA scrubbing mechanism that autonomously corrected most configuration upsets. The measured cross-sections remained stable across the tested energies and were consistent with previously reported values for similar Artix-7 devices.

The consistency between the proton results reported in this work and prior neutron-based studies further reinforces the reliability of the HARV-SoC architecture and the effectiveness of the protection mechanisms integrated into the processor and the system. Despite differences in particle types and test conditions, the measured SEU cross-sections, particularly for configuration-memory SBUs, remain within the previously reported range for the devices, aligning with vendor SER data and prior experimental evaluations. Future work includes extending the proton campaign to higher fluence levels, exploring lower-energy scenarios, and evaluating the same design across different SRAM-based FPGA families to consolidate further the reliability profile of hardened RISC-V implementations in radiation-prone environments.

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