Introducing 14A Nano-Sheet FET technology in Microwind

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Abstract: This paper describes the implementation of the Nano-sheet FET (NS-FET) for the 1.4-nm/14Å technology node in Microwind. After a general presentation of the electronic market and the roadmap to the atomic scale, we present design rules and basic metrics for the 14A node. Concepts related to the design of NS-FET using novel buried power rails are also described. Lastly, we analyze the performance of a ring oscillator, basic cells, sequential cells, and a 6-transistor RAM memory.

Keywords: Nano-Sheet, NSFET, Buried Power Rails, BPR, Through-Silicon-Via, nTSV, 1.4nm, 14A, Ring oscillator, interconnects, SRAM, logic gates

Introduction

The structural growth of the semiconductor industry can be attributed to the soaring demand for electronic equipment, ranging from smartphones & laptops to electric cars, renewable energy systems, high-end servers, and high-performance computing associated to Artificial Intelligence (AI). Giant IC foundries such as TSMC, Samsung and Intel have shown an outstanding ability to propose new technology nodes every two years (Table 1).

Technology node	Year of introduction	Key innovations	Application note
180 nm	2000	Cu interconnect, MOS options, 6 metal layers	
130 nm	2002	Low-k dielectric, 8 metal layers	
90 nm	2003	SOI substrate	[Sicard2005]
65 nm	2004	Strain silicon	[Sicard2006]
45 nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32 nm	2010	High-K metal gate	[Sicard2010]
28 nm	2012	High-K metal gate	[Sicard&Sharma 2015]
20 nm	2013	Double patterning, 12 metal layers	[Sicard2014]
14 nm	2015	FinFET	[Sicard2017]
10 nm	2017	FinFET, double patterning	[Sicard2017]
7 nm	2019	FinFET, quadruple patterning	[Sicard2017]
5 nm	2020	FinFET enhancement, EUV	[Sicard&Trojman2021]
3 nm	2021	Nano-Sheet FET, EUV	[Sicard&Trojman2021b]
2 nm /20A	2024	Buried power rail, nano Through-Silicon-Via	[Sicard&Trojman2022]
1.4 nm /14A	2027	2nd generation Nano-Sheet, NA-EUV	This application note
1 nm /10A	2030	3rd generation Nano-Sheet, NA-EUV	
0.7nm/7A	2032	Stacked Complementary FET	
0.5nm/5A	2034	2nd generation Stacked Complementary FET	
0.3nm/3A	2036	3rd generation Stacked Complementary FET	

Table 1: Most significant technology nodes introduced over the past 20 years and prospective vision for 2036.

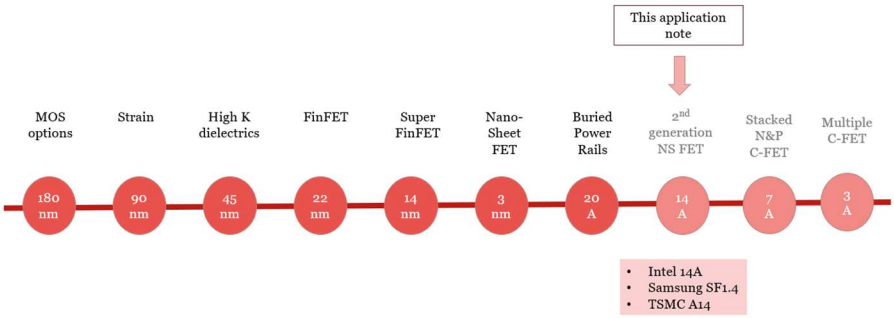

Figure 1: Technological innovation from 180 nm to 10Å technology, adapted from [Intel 2021].

Continuous advances in process fabrication are enabling a vision of future nodes such as 7Å, 5Å, 3Å for the next decade, reinforced by prospective roadmaps from giant semiconductor foundries. Through more than 10 application notes in open access from *hal.science*, we have tried to illustrate the increased performance of devices, specifically for the 14-nm and 7-nm nodes [Sicard 2017], and more recently the 3-nm & 2-nm nodes [Sicard & Trojman 2021b] [Sicard & Trojman 2022]. The key innovations of each technology node are summarized in Figure 1.

Three major silicon foundries, namely TSMC from Taiwan, Samsung from South-Korea and Intel from USA, are planning to introduce 1.4-nm/14A technologies in 2027-2029.

- Samsung is expecting to have 1.4 nm chips based on gate-all-around (GAA) transistor architecture in mass production by 2029, using its SF1.4 technology.
- TSMC is expecting to start production of integrated circuits (ICs) using its A14 technology by the end of 2028 without back side power rails (BSPR, see [Sicard & Trojman 2022]), and with BSPR in 2029 [TSMC].
- Intel announced in 2025 that its 14Aprocess would use a 2nd generation of nano-sheet FET named RibbonFET starting 2028.

In this application note, we describe the main characteristics of the 1.4-nm/14A node by making use of available scientific literature and information released by semiconductor manufacturers, with focus on the Nano-Sheet FET, the buried power rails (BPR) and the Through-Silicon-Vias (TSV). We review the basic design rules, describe the transistor characteristics and the changes induced by buried power rail on the cell design. The implementation and performance of basic cells such as the inverter, the ring oscillator, the static RAM (SRAM) memory and basic logic circuits are presented. We conclude this document by discussing the switching performances of the node.

What the technology node represents

For more than 50 years, Moore's Law [Moore 2020] has described and predicted the shrinkage of transistors and the doubling of the number of transistors in the same silicon surface, roughly every two years. Until 1995, we used a simple rule that stated that the minimum feature size was equal to the node. For example, in 0.35-µm technology, the minimum reachable feature size by the process is around 0.35 µm. In Microwind, the "lambda" parameter used for designing cells was simply half of the minimum feature size. For decades, the minimum gate length was simply fixed to 2 λ. As shown in Figure 2, the gate length became even smaller than the technology node from 1995 to 2010.

Starting in 2010, the reduction of minimum feature size slowed down, and became more and more disconnected from the node name, mostly due to fundamental physical limitations linked to lithography. In nano-scale technology, we are facing a confusion between the "brands" (e.g. 7 nm, 5 nm, 3 nm and 2 nm nodes) and the physical reality of minimum dimensions, which are physically

limited to higher values, despite small lithography improvements. For example, in a 2-nm node, the minimum feature size is in the order of 10 nm, 5 times more than the “commercial” denomination of the node.

To solve this issue, the semiconductor industry decided to switch from "Planar" to "3D" architecture. As a result, the smallest feature size remains much larger than the brand name. As the distribution of the device onto the Si surface is no more planar, we get on an equivalent silicon surface a transistor density and an amount of current equivalent to the technology node.

For example, the 7-nm technology using FinFET devices has a minimum feature size larger than 7nm but in term of transistor integration, it offers the same performance as a 7nm gate length planar MOSFET on the same silicon area (Figure 4).

As the limits of lithography have been reached, progress has been made at the device level through the introduction of more efficient switches (FinFET, Nano-Sheet FET, Complementary FET) and at the design level with new strategies for supplying the cells by means of buried power rails, nano-through silicon vias and back-side power delivery.

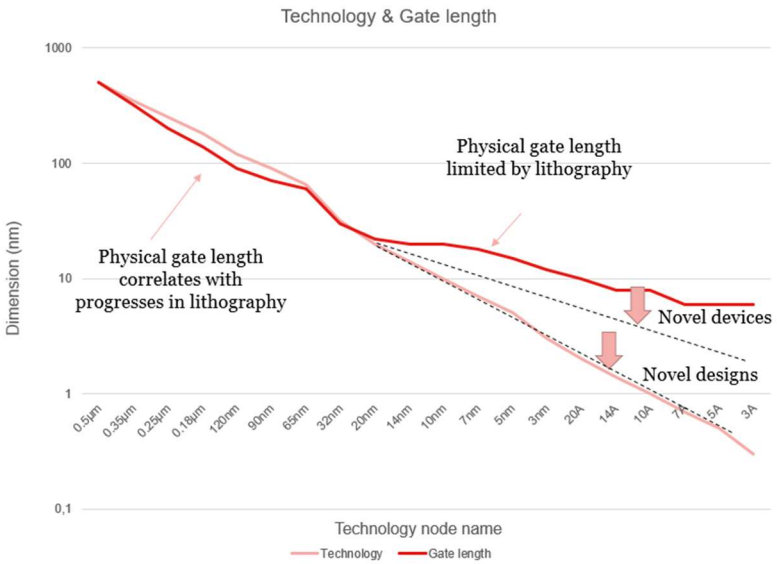

Figure 2: Link between technology nodes and device gate length: from 20 nm, the node name started being uncorrelated to the gate length. Adapted from [Moore 2020].

The Nano-Sheet era

The adoption of nano-sheet FET has followed the adoption of FinFET with a 10-year difference [Samsung 2021]. The 3-nm node has signaled the start of a migration process from FinFET to NSFET, so as to enable further gains in current drive while reducing the device surface, leading to smaller, faster, more complex and energy-efficient chips (Figure 3). The stacked nFET/pFET architecture called monolithic Complementary FET (mCFET or CFET) is announced for future nodes (7A, 5A, 3A) [Kuckner 2024b].

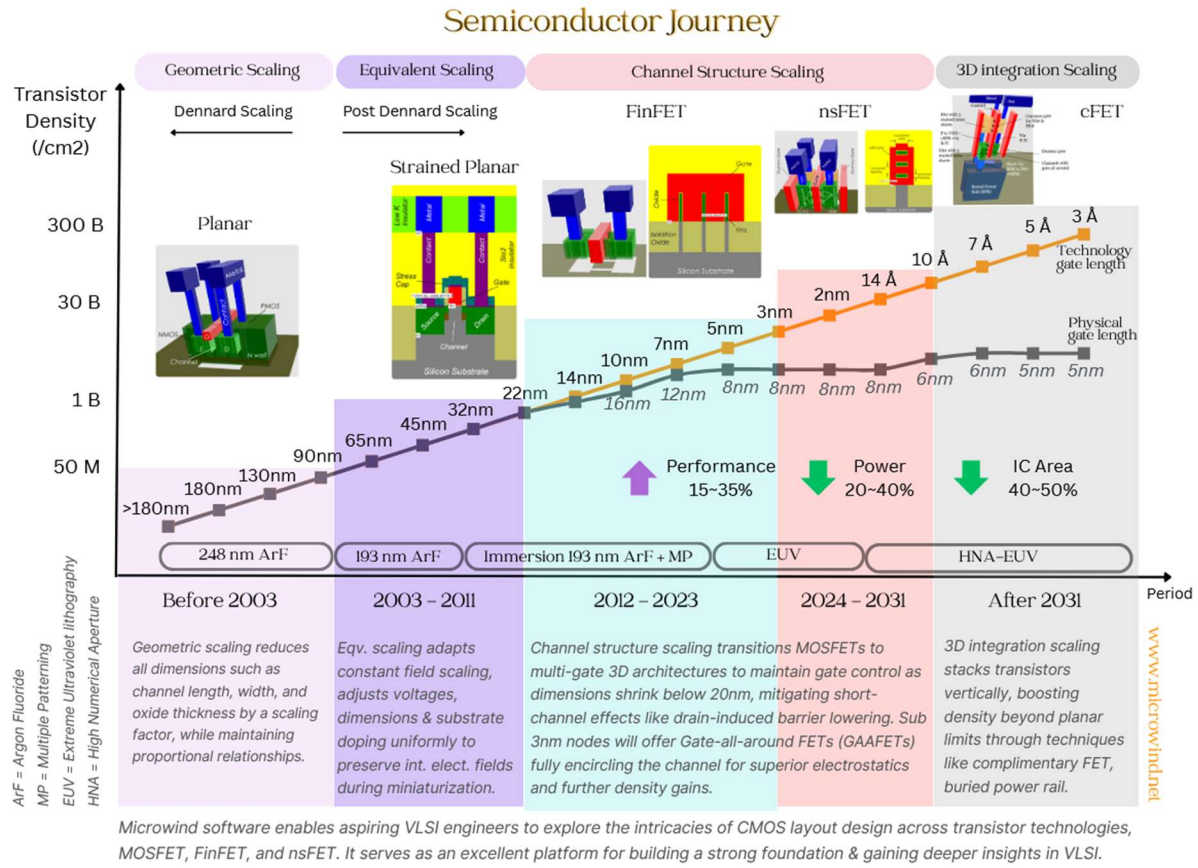

Figure 3: Evolution of CMOS technology from MosFET, FinFET, Nano-Sheet FET to CFET (Adapted from [Zhang 2024]).

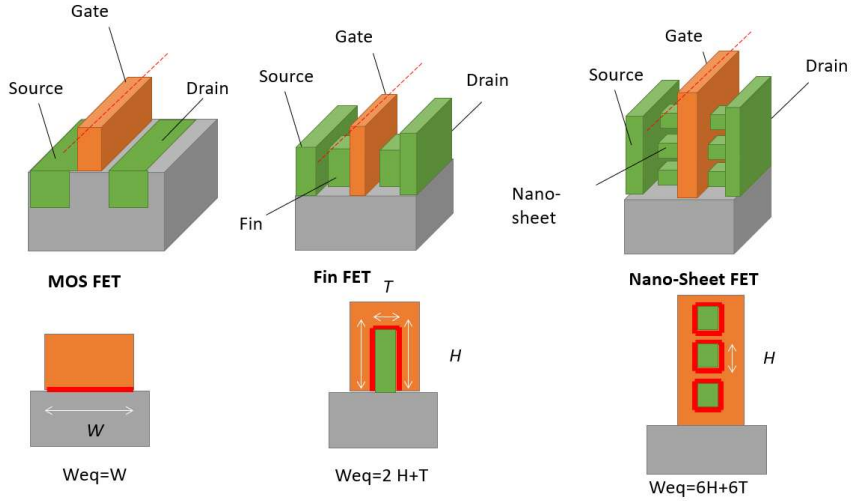

Figure 4: MosFET, FinFET & Nano-Sheet FET, with their corresponding equivalent channel width.

Within a reduced silicon surface, process engineers have been able to fabricate much more efficient devices than the original planar MosFET enabling to increase the device density. Stacking nano-sheets results in an equivalent channel width three times more area-efficient than for a planar MosFET, in its 3-stacked nano-sheet configuration. More details about the NSFET may be found in [Sicard & Trojman 2022].

We have fused key elements found in literature, without any knowledge of the process-design-kit (PDK) proposed by the foundries, due to severe non-disclosure agreements (NDA) restricting access to detailed technology specifications. The industrial process usually results from a careful approach known as design technology co-optimization (DTCO), as well as a precise evaluation of power, performance area and cost (PPAC). In our implementation of the 14A technology in Microwind, we keep the same thickness (called TNS, TCH, or TSH depending on the authors) and spacing (TSP) as those of the 3-nm node [Sicard & Trojman 2021b] (Table 2).

From EUV to HNA-EUV

High-Numerical-Aperture Extreme-Ultra-Violet (HNA-EUV) is the main novelty concerning lithography for the 14A node. It uses EUV light combined with anamorphic optics to create features on silicon wafers as small as 8 nm [Lazzarino 2025]. HNA-EUV tools such as Twinscan EXE:5000 from ASML are expected to cost 400 million $USB per unit, which should impact the overall fab cost and design costs significantly. Intel has demonstrated its ability to manufacture Ribbon-FET devices (the Intel's trademark for Nano-sheet FET) with gate length as small as 6nm [Agrawal 2024].

The reduction of the elementary feature size is translated in Microwind by a reduction of the drawing unit lambda (λ) from 4.0 nm to 3.6 nm, with immediate benefits in terms of silicon area reduction as compared to previous nodes (3nm, 2nm/20A).

Key metrics

We present in this section three key metrics: the gate pitch, the metal pitch, and the “track” design unit.

Gate pitch

The gate pitch, also called the Contacted-Gate-Pitch (CGP), refers to the minimum distance between active gates (vertical red lines in Fig. 5). In Microwind, you may generate vertical gates at regular CGP using the command `Edit > Generate > Tracks (MP) and Gates (CGP)`. Unselect metal tracks and click OK; four vertical gates will be drawn, with a CGP of 36 nm (10 λ). In Microwind, the gate pitch has remained constant at 40 nm in the 5, 3 and 2 nm nodes, and has been shrinked to 36 nm starting 14A node.

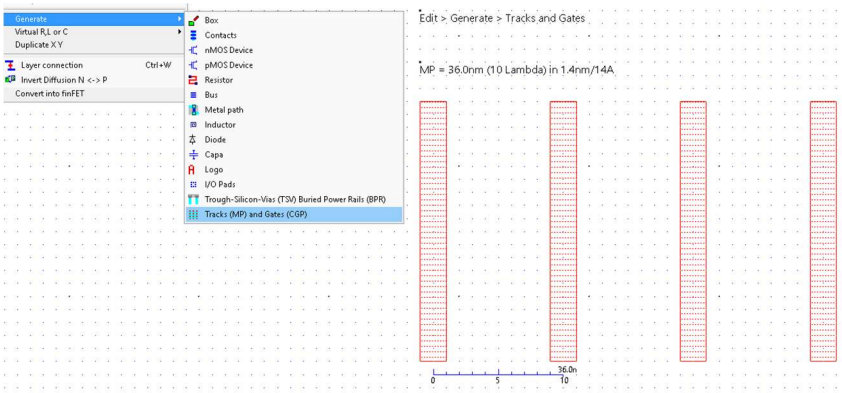

Figure 5: Generating gates with the 36 nm (10 λ) contacted gate pitch (CGP-4gates.MSK).

Metal pitch

Using the command `Edit > Generate > Tracks (MP) and Gates (CGP)`, we may select metal tracks that will be routed using the associated metal pitch, i.e. the sum of the minimum metal width (r501) and the metal 1 spacing (r502). In our implementation of the 14A in Microwind, the minimum metal width is 3 λ (11 nm) and the spacing is 2 λ (7 nm), which yields a metal pitch (MP) of 5 λ (18 nm), as illustrated in Figure 6. This metal pitch matches the M0 MP of [Kukner 2024].

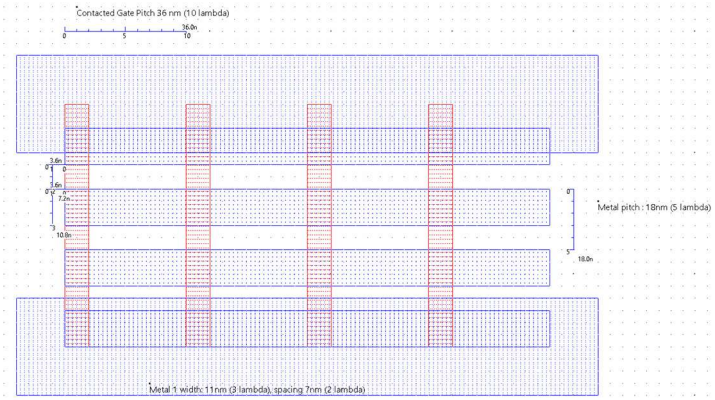

Figure 6: Generating gates with the 36-nm (10 λ) contacted gate pitch (cgp-mp-bpr-4x4.MSK).

DESIGN PARAMETER	UNIT	CODE	NAME IN RULE FILE	VALUE IN 14A PROCESS
LAMBDA	nm	λ	lambda	3.6
CORE SUPPLY	V	VDD	Vdd	0.65
DEVICE TYPE		NanoSheet	nsfet	3
WIDTH FAST	λ	WF	nswhp	8
WIDTH SLOW	λ	WS	nswlp	4
DEVICE HEIGHT	nm	HNS	thpoly	55
THICKNESS NS	nm	TNS	tns	5
SPACING NS	nm	TSP	tsp	10
NUMBER OF NS		NS	nsfet	3*
GATE LENGTH	λ	GL	R302	2
GATE PITCH	nm	CGP	cgp	36
SPACER WIDTH	nm	SW		10
CONTACT SIZE	λ	CS	R401	2
EOT	nm	EOT	b4toxe	0.95
M1 WIDTH	λ		R501	3
M1 SPACING	λ		R502	2
METAL PITCH	nm	MP	R501+R502	18
METAL TRACKS		5T	tracks	2
WIDTH BPR	λ		RK01	8
SPACING BPR	λ		RK02	12
VIA BPR	λ		RK03	4
DIE THICKNESS	µm		THDI	1.0
RULE FILE				Cmos14a.rul

Table 4: Basic parameters of the 14A process implemented in Microwind (cmos14a.RUL); (*) the number of nano-sheets (three by default) can be changed from two [Mii 2024] to four [Intel 2025]

14A Implementation in Microwind

The table-4 illustrates the parameters for 14A technology node implemented in Microwind software. The 14A technology offers a feature size reduction of 10% compared to 20A technology, offering 20% area advantage and 15% speed improvement at the same power, or up to a 30% power reduction at the same speed.

Basic Inverter

The layout of a basic inverter is shown in Figure 7 (left). The cross-section (Figure 7, right) follows the vertical axis A-A'. The NSFET devices have three stacked nano-sheets, with each nano-sheet being isolated from the gate by a thin oxide (Al_2O_3,ZrO_2, HfO_2..).

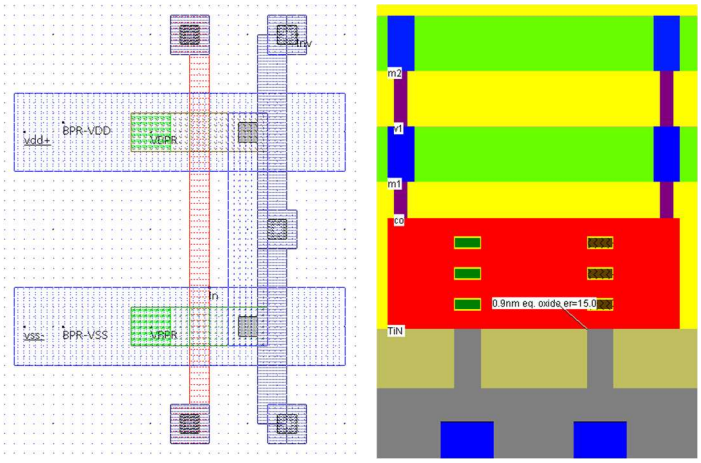

Figure 7: Basic inverter with BPR supply and slow mode (inv5Tracks.MSK).

Two versions of the NSFET are considered in Microwind, one called "slow" mode (W=4 λ), the other called "fast" mode (W= 8λ); both are shown in Figure 8 along with the associated cross-section showing the three stacked nano-sheets. The hand-made design of the NSFET can use any channel width larger than or equal to the minimum width (4 λ).

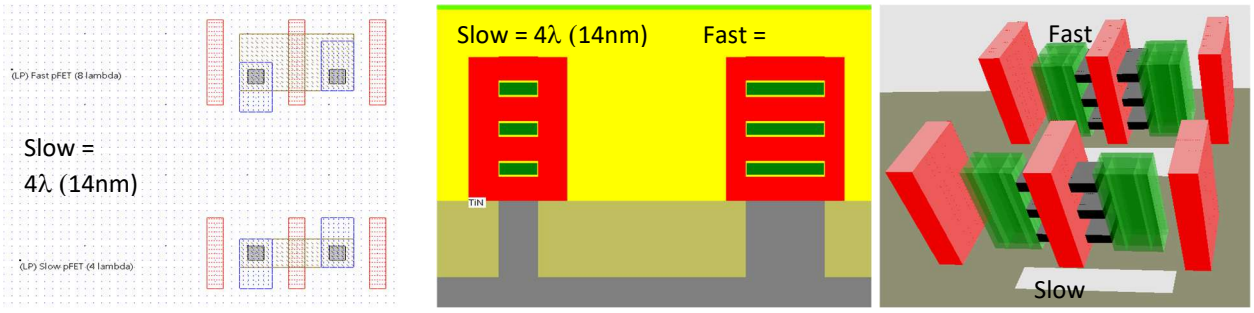

Figure 8: Slow and fast devices, layout view, cross-section and 3D view (nsFETs-slow-fast.msk).

NS-FET Performances

The ION/IOFF currents for nano-sheet devices in the 14A technology are similar to the currents of the NS devices described in [Sicard 2022] for the 2nm/20A technology.

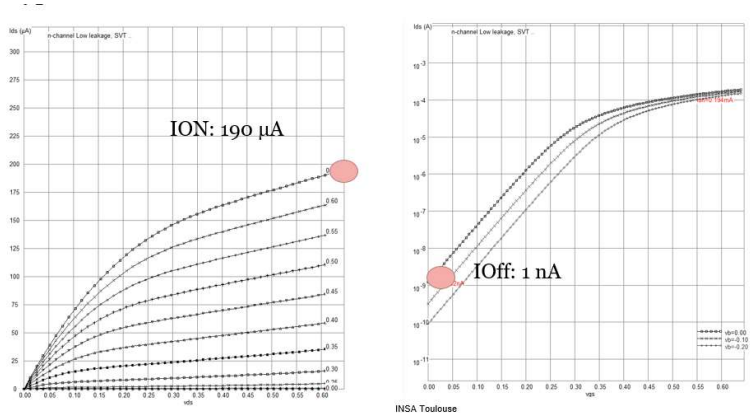

Figure 9: ION/IOFF for the slow NSFET, n-type @ 0.65 V.

The ION current for the slow n-type device is around 190 µA for total channel width of 115 nm (Figure 9) and corresponds to the maximum available current for this device at nominal voltage (VDD=0.65 V). The IOFF current corresponds to VG=0, which is around 1.2 nA. As for the slow p-type device, ION is 159 µA and IOFF is around 1.3 nA (Figure 10). The subthreshold slope is around 65 mV/decade.

The ID/VD curves of the slow and fast devices show an ION current that is nearly double. Using the option layer, we can turn the device to high-performance mode for a supplementary boost of around 25%, but at the cost of an IOFF multiplied by 10 (Figure 11). The use of such a device should be restricted to situations where the speed is critical (clock tree, critical logic path, needs for highest performance) and power saving is no more the priority.

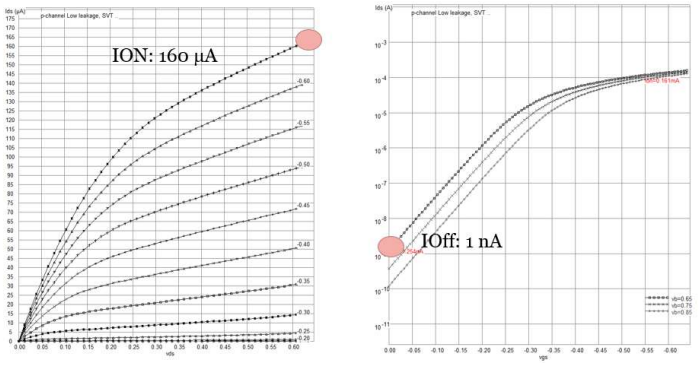

Figure 10: ION/IOFF for the slow NSFET, p-type @ 0.65 V.

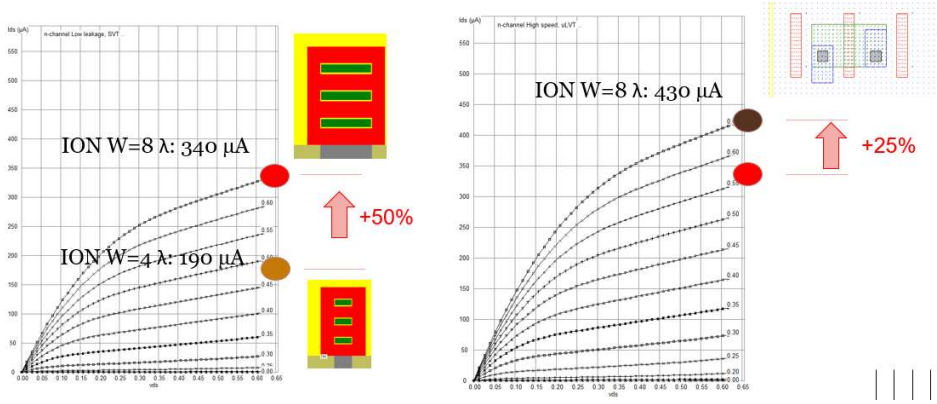

Figure 11: Comparing the ION of the slow & fast nFET (left), and the supplementary ION boost using the high-speed device option.

In our implementation of the 14A NSFET, the low-leakage default device has a threshold voltage around 0.30 V, while the high-performance device has a low Vt around 0.25 V. The Vt adjustment is achieved by modulating the effective work function (EWF) of the gate through the introduction of specific metallic material or modifying the oxide properties, as described in [Chen 2022].

NS-FET Booster

An approach for increasing the ION current furthermore is to increase the number of nano-sheets. In Microwind, the parameter `nsfet` (3 by default) controls the number of nano-sheets. It can be changed from 2 to 4 NS using a selection in the compiler menu, as illustrated in Figure 12. Low power devices such as smartphones may require only 2 NS, general purpose devices such as laptops 3 NS, and high-performance devices such as servers 4 NS.

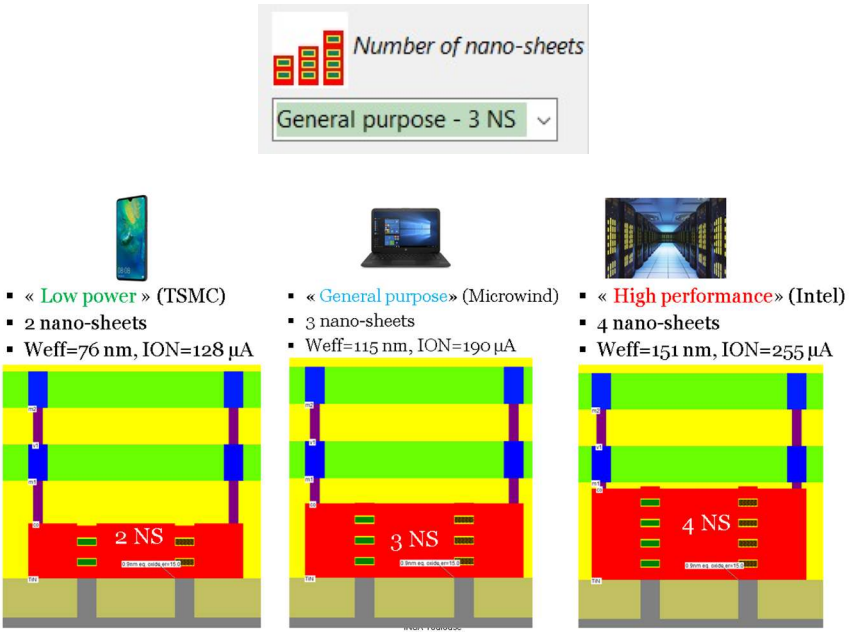

Figure 12: The number of nano sheets has a direct influence on the ION current and may be a booster to match high performance computing requirements (4 NS) or meet the low power requirements (2 NS).

Getting started with the 14A design

Hand-made design of an inverter

1. Select the “NsFET Gate” layer in the palette window (Red).
2. Fix the first corner of the box with the mouse. While keeping the mouse button pressed, move the mouse to the opposite corner of the box. Release the button. This creates a narrow gate. The box width should not be inferior to 2 λ, which is the minimum and optimal thickness of the gate.
3. Select “N+ diffusion” by clicking on the palette of the N+ Diffusion (Green).
4. Draw a n-diffusion box at the bottom of the drawing as in Figure 13. The N+ diffusion should have a minimum of 4 λ height and extension at both sides of the polysilicon gate. The intersection between the N+ diffusion and gate corresponds to the channel of the N-device.
5. Select “P+ diffusion” by clicking on the palette of the N+ Diffusion (Brown).
6. Draw a P+ diffusion box, as shown in Figure 27. The intersection between diffusion and gate creates the channel of the P-device.
7. Select “Metal 1” and draw a box over the N+ & P+ area. The minimum width is 3 λ.

8. Select the icon “Connect layers”  , click on the intersection N+/metal, and again on the intersection P+/metal.
9. Add VDD and VSS properties.
10. Add a clock to the input gate.
11. Add a “visible” property to the output (“Visible node”).
12. Click “Simulate”. Click “More” until you reach 1 ns.

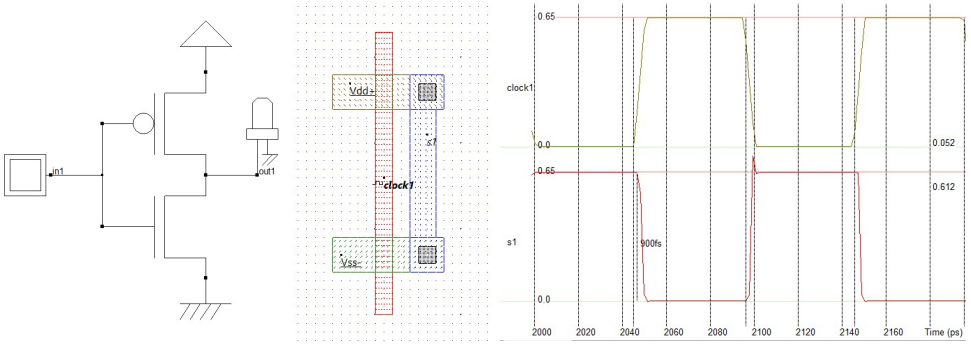

Figure 13: Steps to draw a simple inverter (mySimpleInverter.MSK).

Another approach to avoid design rule errors is to instantiate the n & p devices directly using the layout generator. Just click the device icon on the palette (“Generate Device”), place the component on the layout. Click the same icon, this time selecting “p-type”, and place the component on top of the n-type device. Dummy gates are added by default for manufacturability purpose. The devices should be aligned. The minimum distance between N+ and P+ diffusions is 6 λ. All gates should touch together in order to merge vertical layers in a regular way, as illustrated in Figure 14.

nsFET Parameter	Slow	Fast
Width (W)	4 λ	8 λ
Length (L)	2 λ	2 λ

Figure 14: Select a n-channel or p-channel NSFET.

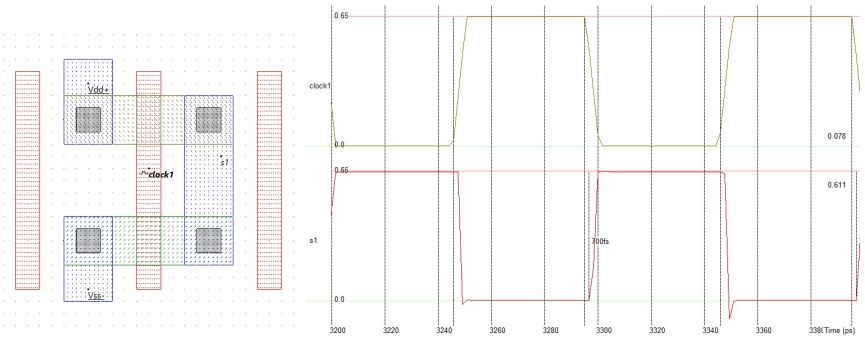

Figure 15: Creating an inverter with n-channel or p-channel NSFET generated by Microwind

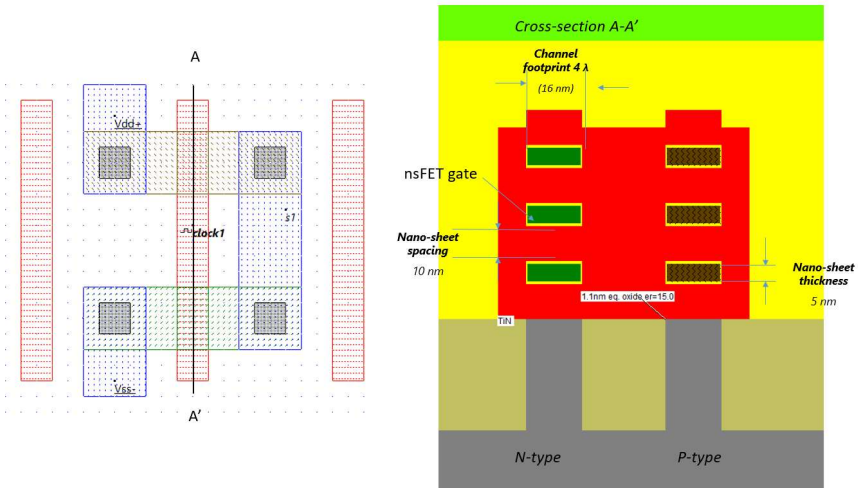

Figure 16: Cross-section of the n-channel or p-channel NSFET generated by Microwind.

The N & P devices use a 4 λ channel footprint, which corresponds to the "slow" design style. The nano-sheet cross section can be displayed using the icon , with the vertical selection corresponding to the active gate (A-A'). The three stacked nano-sheets are shown (Figure 30), each with a thickness of 5 nm and spacing of 10 nm. The equivalent channel width *Weff* is

$$W_{eff} = ns \times (2W + 2TNS) = 3 \times (2 \times 16 + 2 \times 5) = 128\,nm$$

where *ns* is the number of nano-sheets, *W* is the channel footprint and *TNS* the nano-sheet thickness.

Compile one inverter, 5T

Microwind includes a specific tool to handle the generation of a complete inverter. Other simple logic cells such as NAND, NOR, AND, OR can also be generated using this tool. The cell height corresponds to the "5T" approach, with the supply wires VDD and VSS routed by means of buried power rails. The link between BPR and diffusions is established using the "Via to BPR" (vbpr). The device width can be either "Slow" (4 λ footprint) or "Fast" (8 λ). An example of compiled inverter is shown in Figure 31. The performances correspond to 3-NS devices (default configuration). If you run the Design Rule Checker (DRC), the layout should be error-free.

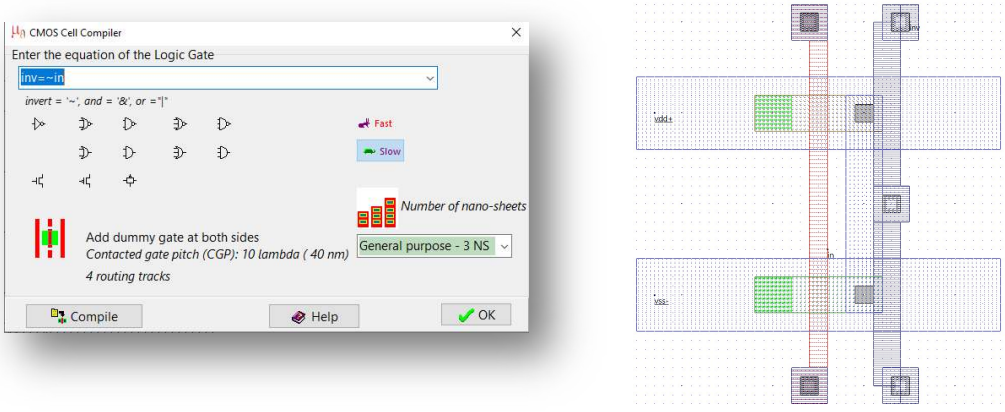

Figure 17: Compiling basic gates with the Microwind cell compiler.

Logic Design with Nano-Sheet

Ring Oscillator with Fan-Out

We design a 3-stage RO with a 3-input load, which will eventually used to study the performance of RO in the 14A technology. The corresponding layout is shown in Figure 18. The capacitance load of each stage is around 1 fF, which is similar to the 2nm/20A technology [Sicard 2022].

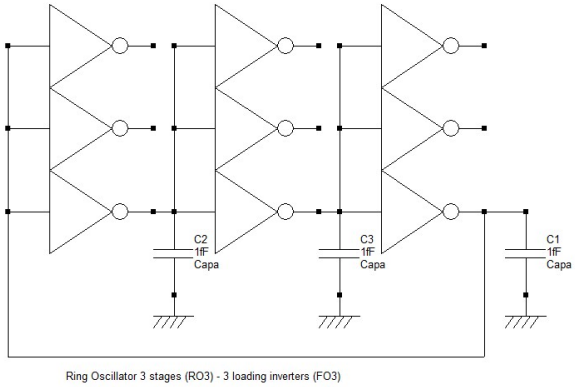

Figure 18: Each inverter output is connected to three inputs to emulate a significant load.

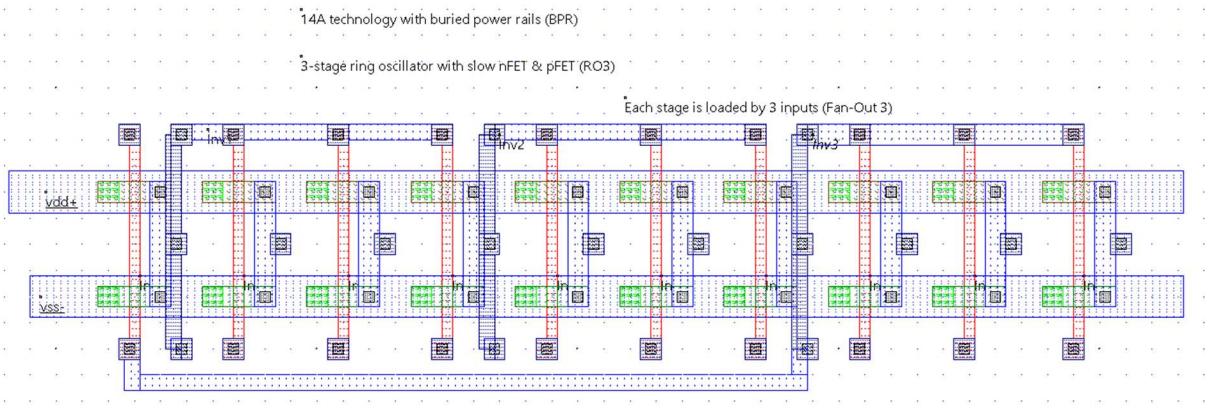

Figure 19: RO3, FO3 with slow design (RO3FO3.MSK).

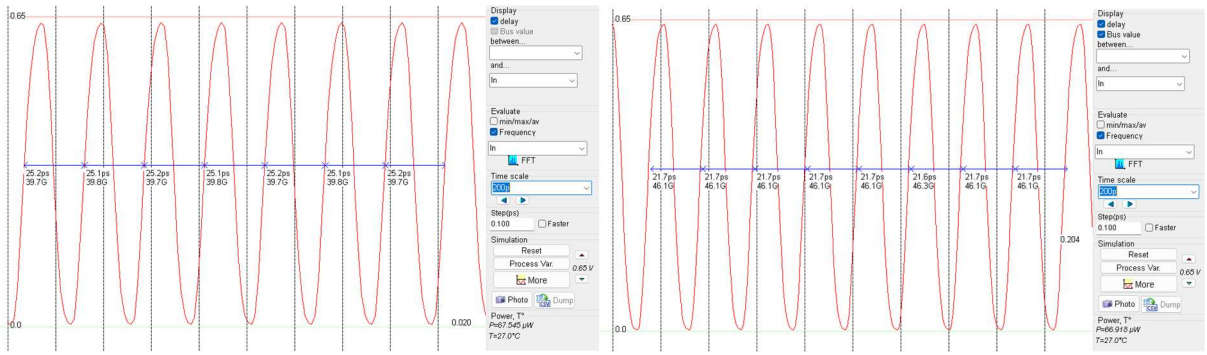

Figure 20: The ring oscillator frequency for 20A and 14A technology, where 14A illustrates 15% boost in oscillating frequency to 46Ghz from 40Ghz, the power consumption same at around 67 µW and the power supply identical at @0.65V (RO3FO3.MSK).

Basic cells

We use again the cell compiler to generate basic cells, namely the NAND, NOR, NAND3, OR3 and AND3 gates. The cells are placed horizontally with a regular CGP and share the same VDD (top of the cells) and VSS (bottom of the cells, Figure 38). The A, B and C inputs were merged to simulate the gate inputs simultaneously, by means of M1/M2 routing and appropriate vias on the bottom. The simulation shows a delay ranging from 1 to 2 ps for unloaded Nand & Nor gates, and increased to 3-4 ps for unloaded AND & Or gates, due to the supplementary inverter stage (Figure 21).

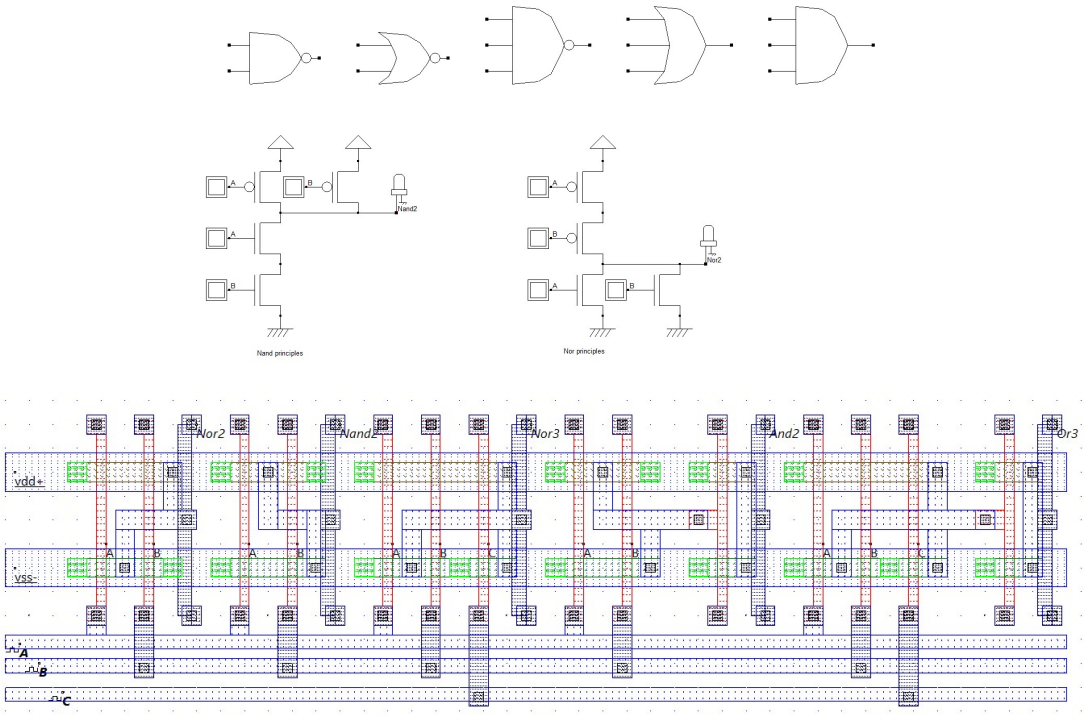

Figure 21: Compiled basic gates using the cell compiler in 14A NSFET technology, with 5T strategy (basicgates.MSK).

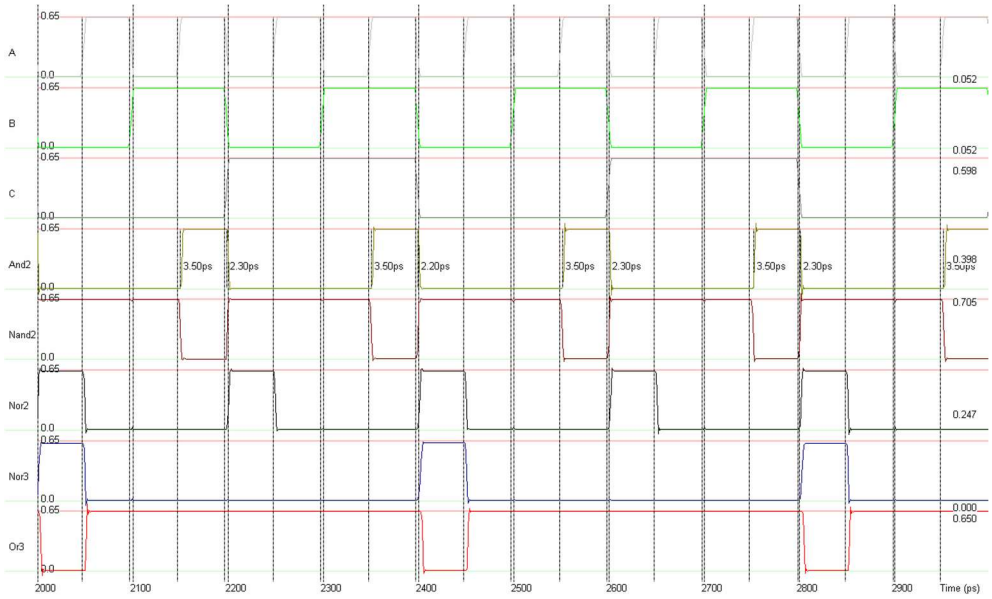

Figure 22: Simulation of Nor2 in 14A NSFET technology. The largest delay is observed for multiple-input AND & OR gates due to an inverter stage (basicgates.MSK).

SRAM design with BPR

The 6-transistor static memory (also called 6T-SRAM) consists of a 2-inverter stable loop that stores the data and two access transistors to either import or export the logic data through so-called bit lines. When the data is imported from the outside to the cell (the data through BL, its opposite through ~BL), we speak of the write cycle; when the data is exported, it is called the read cycle. The cell structure is optimized for multiplication in X, Y in order to create a matrix of cells, typically 1000 x 1000, leading to a 1 Mega-bit memory plane.

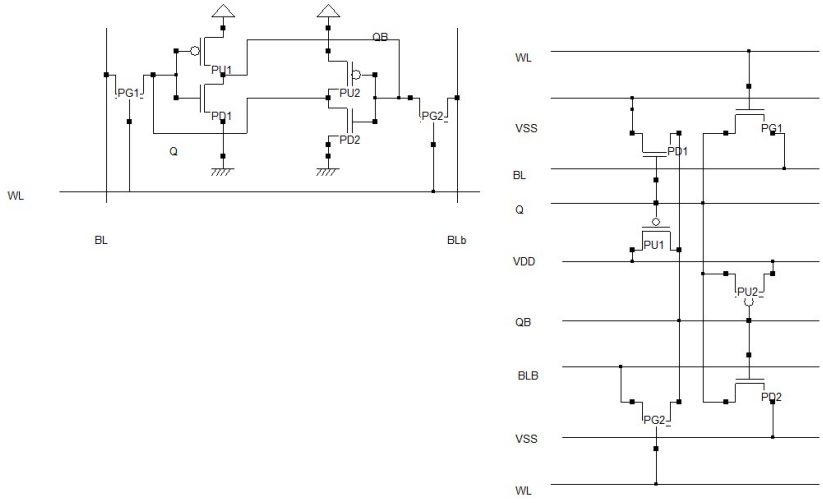

Figure 23: Proposed implementation of the 6T-SRAM adapted from [Gupta 2021c].

The schematic of a six-transistor SRAM bit-cell is shown in Figure 23 (left). A possible implementation with all signals routed horizontally is proposed in Figure 23 (right) [Gupta 2021c]. The cell consists of two pairs of inverters (*PU1-PD1, PU2-PD2*) and two pass gates (*PG1 and PG2*). The *bitline* signals *BL* and *BLb* are significantly enlarged by the introduction of the buried power rails (Figure 24), decreasing its serial resistance and thereby significantly enhancing the write margin and overall performances, without any silicon area penalty, as the SRAM area remains the same.

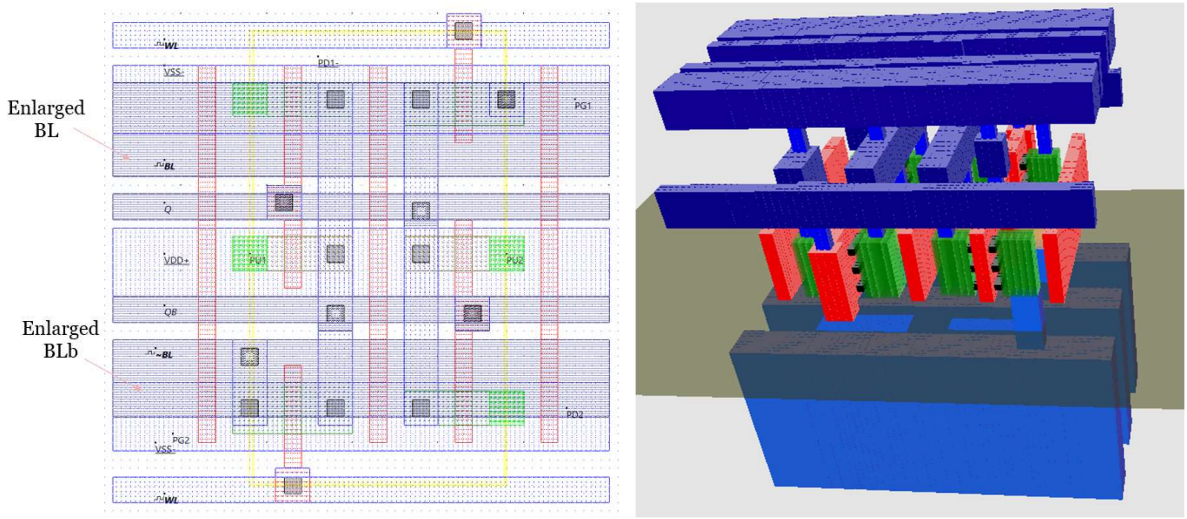

Figure 24: Proposed implementation of the 6T-SRAM with enlarged BL and BLb (SRAM-6T.MSK).

Environmental Impact - From the Natural sand to industrialized chip

Since the early 2000, organisms such as GIEC [GIEC 2018] have raised serious concerned to politic regarding the effect of the human activities on its own environment: the earth. Acceleration of temperature changes was among the very first measurable indicators to demonstrate this effect. By the time being, the temperature increase has induced the warming of the oceans, the shrinking of the ice sheets, the retreat of the glaciers, the decrease of the snow covering the sea level rising the decline of the arctic sea, the increase of the extreme event frequency and the acidification of the ocean [NASA]. Even though this observation brings many questions from the human perspective, the most cynical standpoint must be kept pragmatic. In terms of industrial needs, what we call global warming or climate changes challenge production yield, economy and geopolitical stability. The consequences are detrimental for commercial and technological development. Industries are among the first affected by this global effect. We propose in this chapter a rapid overview of the environmental impact of the semiconductor industry.

Power outage

Recently, PricewaterhouseCoopers (PwC) reported that 32% of the global semiconductor production will be reliant on Chilean copper supply at risk from climate disruption (doughtiness) by 2035 and 58% by 2050 if emission does not decline [PwC 2025]. We may also remember one of the several late hurricanes named Helen which disrupted the world's supply of high-purity quartz [Forbes 2024] required to produce semiconductors. In terms of financial perspective, we are talking about 650 Billion $USD loss today and 1 Tera $USD in 2035.

The semiconductor industry is known to be highly energy intensive: ovens for silicon melting, high-power laser for lithography, vacuum and cleaning systems necessitate hundreds of MW-h. The main energy consumption is electrical (80%) then, fossil (12%) [Wang 2023]. Yet the primary electrical source is 60% fossil energy [Khan 2019] [Ritchie 2020]. As a result, IC fabrication hit the 185 million-ton CO2 making the semiconductor industry among the major Green House Gaz contributor [Gallagher 2025].

On the other hand, relying on fossil-based energy for electricity production is risky. Oil and gas are at the center of many geopolitical conflicts. Any price variation or worst disruption in the supply of fossil fuels could have severe consequences for the production yield of semiconductors industry. This oil dependency and CO2 contribution urge the semiconductor industry to complete its energetic transition toward the renewable energy [Koirala 2025].

Semiconductors and the human society

Apart from this consideration, semiconductors have an unprecedent importance in human society [Silva 2025]. The turning point has likely been the sanitary crisis of the covid in 2019 where we learn two fundamental social facts.

- First the digital experience enabled human society to keep assuming functional mission and accelerate the transformation in the workplace (ethos at work).
- Second, the human society in many aspects is strongly dependent on semiconductor compound even in unexpected field: from health to education, transport, defense, security or for any industry field [Ardolino 2024]. It was clearly observed that a chip shortage has an impact more or less important and at some extent could paralyze a whole country hence, companies look for solution to cope with such situation in the future [Marinova 2021].

Recently it was reported in 2025 the global semiconductor revenue increased by 21.7% year to year [SIA 2025] and is expected to reach 1 Tera $USD by 2030 [PwC 2025]. In addition, the semiconductor industry also produces geopolitical uncertainty between eastern and western parts of the world

jeopardizing economy stability [Snarska 2025]. Up to a point the semiconductor race becomes a sovereignty warrant for countries as US or China, or, region in the world as Europe. Many indicators suggest that the semiconductor could be the new oil [Yusuf 2022].

From a technological standpoint, the digital transformation of society has generated major implications. Among them are the growing dependence on connected and smart objects, leading to an exponential increase in the number of IoT devices [Sinha 2025]. Recent surveys report that more than 400 zetta-bytes of data will be generated by 2025, requiring large-scale storage capacities in upscaled datacenters (Cloud), as well as massive data flows transported through limited communication infrastructures (Internet, 5G/6G) [Akbar 2025].

These developments lead to significant challenges: a rapid acceleration in the consumption of material resources for semiconductor manufacturing, and a dramatic increase in global energy consumption, since every data movement or storage operation relies on the QV-paradigm (charge potential). Indeed, several bottlenecks have already been identified, and only incremental optimizations have so far postponed the fundamental technological limits.

Environmental impact of the whole-digital era

In 2023 the environmental impact (fingerprint and energy consumption) from digital applications was largely concentrated on user terminals and digital objects than data center. And for this same year, digital applications are 2.2% of the total energy consumption in Earth and about 20% of the electricity consumption [Ritchie 2024].

But more dramatic, this digital transformation thrown the human society in the era of “whole-digital” information. Retrieving data in quasi real time is at some point substituting monetary exchange. This has been “handle” using Artificial intelligence (AI) model or automatization of information retrieving, either factual (Machine Learning - ML) or contextual (Transformer) datacenter. Yet AI models need a large amount of energy for their training.

According to the IEA [IEA 2025], the integration of AI in Data Center will have a tremendous environmental impact, expecting in 2030 a need for electricity at least twice as large as today. The other impact is “material” since the AI models required strong semiconductor resources and the highest performance technological nodes. As mentioned earlier, this semiconductor technology led to various economic and geopolitical risks, but AI contributed to exacerbating the tension to another level. A disbalance of the technology access generates politic of containment leveraged on import/exportation tariff rises or threat: e.g. TSMC build their new fab in USA territory [Miller 2022].

Next, the AI technologies are not mature enough to produce a good economical yield which forces the principal investors to use their own capital to feed R&D in this field. This strategy suffers from a significant risk: the obsolescence of the invested infrastructure mainly relying on technological node used for the chips when the AI will reach maturity. Also an AI speculation bubble is not discarded and for a multi-Trillions USD$ economy, the impact would be significant and not only the semiconductor industry.

Reducing energy use and environmental impact

Advanced patterning challenges are coming together with additional requirements for sustainable & low Global Warming Potential (GWP). Amongst the different process areas for chip-making manufacturing, dry etch processing is the area that contributes the most in direct emissions (70% estimated by [Filippidou 2024] on A14 node). In dry etching, fluorine-based gases such as CF4, NF6, C2F6 ou NF3 are commonly used during IC processing, which have high Global Warming Potential

(GWP) and negative environmental impact. The atmospheric lifetime of some gases can be hundreds of years so they will continue to trap heat in our atmosphere long after release.

The imec.netzero software platform [Imec 2025] from IMEC's Sustainable Semiconductor Technologies and Systems (SSTS) initiative gives a detailed look into the environmental impact of high-volume semiconductor manufacturing. The tool has been used by [Gross 2023] for reducing energy use and environmental impact of IC process. Replacing CF4 with alternative fluorocarbons can significantly lower greenhouse gas (GHG) emissions that while ensuring similar on-wafer etch performance.

Major companies such as Intel [Intel 2023] are committed to delivering the highest performance ICs while driving to the lowest possible environmental footprint, with a goal to achieve net-zero greenhouse gas emissions by 2040, by using greener chemistries, improve equipment designs, accelerate the use of renewable electricity and deliver more energy-efficient products.

TSMC has identified in 2023 potential climate risks and opportunities in the value chain. The company established indicators and target management to achieving a balance between technologies and ecology. TSMC has mapped out a roadmap setting the goals of zero emissions growth by 2025, 100% renewable energy consumption by 2040 and net zero emissions across the value chain by 2050 [TSMC 2025].

An estimation of the embodied carbon footprint of Solid-State Drives (SSDs) has been proposed by [Weppe 2025] around 22 kg CO2-equivalent per Tera-Byte, by analyzing the manufacturing complexity and the process steps required to fabricating these devices. The authors revealed that higher-density SSDs, which utilize more advanced multi-layer technologies, demonstrated an improved carbon efficiency.

In summary, the semiconductor industry is trapped in vicious circle where the modern ethos of human society requires a high yield semiconductor industry which in turn significantly contributes to global warming. This last one starves material resources pool and requests energy limitation while the decline of environmental conditions degrades geopolitics situation that requests more digital technology to answer these challenges. Novel solutions in terms of process integrations, molecules used for patterning modules, and overall stack of materials will have to meet sustainable and low GWP requirements while staying compatible with low-cost & high-volume manufacturing. A deep restructuration of the IC ecosystem to integrate eco-design and reuse will need to arise, either from top-down political intervention or company-driven initiatives [Alioto 2025].

Conclusion

This application note describes the implementation of the 14A technology in the educational tool Microwind, which the introduction of buried power rails and nano-Through-Silicon-Vias. In this paper, we discussed the NSFET characteristics, the performance tradeoff, the interconnect parasitic effects and the performances of basic cells such as logic gates, ring oscillators and memory cells.

Although limited gains are observed in terms of geometrical scale down, the NSFET efficiency—combined with back-side power delivery using BPR—leads to significant gains in terms of silicon area and the shrinkage of the logic cell height. Further improvements are forecast by introducing stacked P-FET and N-FET—also called Complementary FET (C-FET)—in future technology nodes [Kukner 2024b].

Acknowledgements

We gratefully acknowledge the numerous students, researchers and engineers who have used our applications notes related to integrated circuit technologies, and published more than 700 scientific papers using Microwind. This motivates us to release new application notes dedicated to the nano-CMOS technologies of the future. A sincere thank you to Ricardo Sepulveda Hirose for proofreading the article.

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industry requirements.
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