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Non-destructive characterization of Breakdown Voltage measurement and Application on a 55nm SiGe HBT featuring f_T/f_{MAX} of 400GHz/500GHz

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Abstract

This paper presents a study of the SiGe HBT 55nm Breakdown Voltages (BVs) related to Impact-Ionization (II) as an earlier reliability assessment. A non-destructive measurement setup allowing a complete Safe Operating Area (SOA) characterization and a derived study of the BV_{CEO} and BV_{CBO} is presented. An automatic extraction methodology of the Breakdown Voltage is proposed. The HiCuM compact model is validated against measurement using the same measurements methodology. Finally, the evolution of the BVs after a degradation is characterized.

1. Introduction

In the context of increasing demand of RF-circuits and of their performances with the new 6G and satellite constellation network [1][2], STMicroelectronics is upgrading the 55nm SiGe BiCMOS technology called B55. The enhanced technology named B55X features a SiGe Heterojunction Bipolar Transistor (HBT) reaching f_T/f_{MAX} respectively of 400GHz/500GHz [3]. The increasing RF-performance goes with a reduction of the BV_{CEO} and BV_{CBO} below 1.5V and 5V for High-Speed (HS) devices [2]. Therefore, the Safe Operating Area (SOA) of the devices is reduced leading the RF and mmW circuits to operate closer to the SOA edges. To achieve high RF performances and drive the transistor in these operating conditions over the circuit lifetime, circuit designers need an accurate ageing model based on an accurate SOA definition and a comprehensive ageing study.

This work presents a non-destructive BV_{CEO} and BV_{CBO} extraction methodology from measurement and HiCuM model, as a prerequisite for ageing study. The study of the BVs is conducted on different Emitter form factors enabling scalability analysis. Finally, a preliminary study of BVs evolution after ageing tests is presented.

2. Measurement setup and extraction methodology for SOA and BVs study

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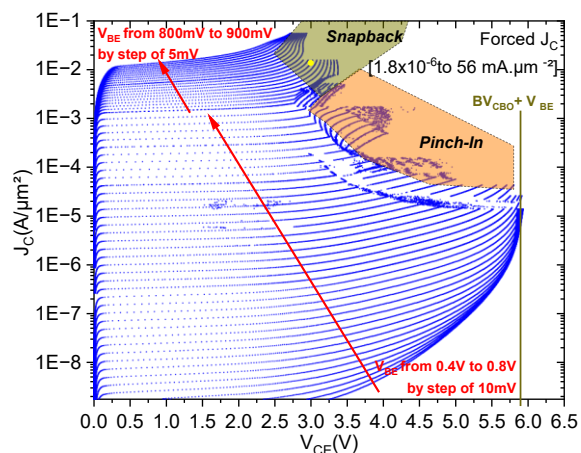


Fig 1. J_C versus V_{CE} for different V_{BE} showing the SOA of a B55X NPN HS device featuring $A_E = 0.2 \times 5\mu\text{m}^2$.

The SOA is defined as the bias conditions for which no critical failure occurs [4]. As shown in Fig 1., the SOA is limited by the BV of the Base-Collector junction with emitter grounded (BV_{CBO}), materialized by the current abrupt increase at $BV_{CBO} + V_{BE}$, according to two limiting charge transport mechanisms: the snapback and the pinch-in. The measurement of the SOA is challenging due to the occurrence of parasitic mechanisms: weak and strong avalanche as well as self-heating.

2.1. BV_{CEO} and BV_{CBO} description

The weak and strong avalanches consist in an

increase of the I_B and I_C currents due to Impact-Ionization (II) mechanism [5] and leading to critical failure. The II mechanism is triggered with a specific voltage known as the BV_{CEO} . The BV_{CEO} occurs at low Base voltage and corresponds to the voltage where I_B becomes negative due to the inversion of the majority carrier type in the Base. Beyond this voltage, the device suffers greater degradation [6].

$$M = \frac{1}{1 - \left(\frac{V_{CBi}}{BV_{CBO}}\right)^{n_{AVL}}} \quad (1)$$

$$I_C = M \times I_{C0} \quad (2)$$

Strong avalanche effect occurs at high V_{BC} and the BV_{CBO} corresponds to the voltage for which I_C tends to infinity and leads to catastrophic failure. The semi-empirical equations (1) and (2) describe I_C current values in avalanche conditions [4] with M the multiplication factor calculated with V_{CBi} the intrinsic Collector-Base voltage and n_{AVL} a fitting parameter close to 5.

2.2 Measurement setup

To measure BV_{CBO} , BV_{CEO} , and the SOA, the transistor is driven close to electro-thermal runaway and in weak and strong avalanche regimes. Consequently, the proximity of the electro-thermal destruction requires dedicated setup with controlled current. To avoid a catastrophic failure of the device, the J_C is controlled while the V_{BE} is swept [4]. V_{CE} and J_B are measured to obtain an I_C versus V_{CE} graph shown Fig 1. By forcing the current, the avalanche regime is controlled so that the unstable effect such as snapback can be measured (Fig 1). The measurements are performed using Ground-Signal-Ground RF-pad structures to ensure the measurement stability and to avoid measurement oscillations as well.

2.3 Extraction methodology

To extract the BV_{CEO} and the BV_{CBO} of the B55X $0.2 \times 5 \mu m^2$ HBT under test, the measurement setup presented in Section 2.2 is used. The BV_{CEO} values are observed when the absolute value of I_B drops to 0. To extract this value, J_C is controlled from $1.8 mA \cdot \mu m^{-2}$ to $8.8 mA \cdot \mu m^{-2}$ and a V_{BE} is set according to the HBT dimension to drive the transistor in the same operating condition i.e. same Base current density. The current densities are selected from a measurement of the reference dimension device for which the $|I_B|$ drop is clearly identified. Hence, the three current densities are $J_{B1}=655 nA \cdot \mu m^{-2}$, $J_{B2}=872 nA \cdot \mu m^{-2}$, $J_{B3}=1 \mu A \cdot \mu m^{-2}$.

BV_{CBO} measurements are conducted under the same conditions as the BV_{CEO} ones. However, the

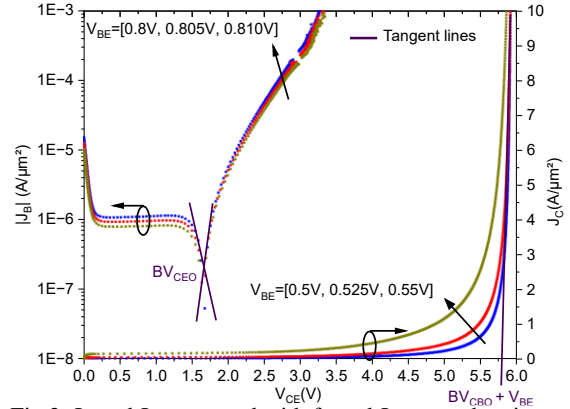


Fig 2. J_C and J_B measured with forced J_C setup showing BVs extraction methodology through tangent line tracing on B55X $0.2 \times 5 \mu m^2$ device.

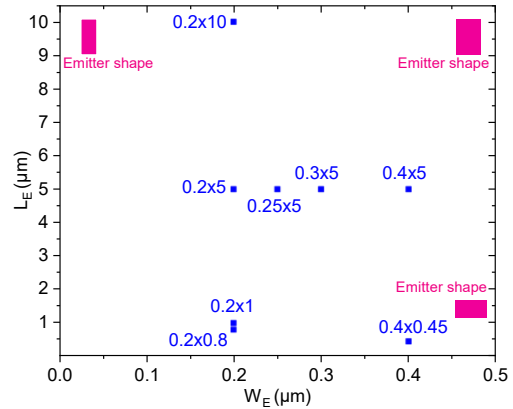


Fig 3. Representation of the different Emitter dimensions under study on a W_E versus L_E graph.

measurements are done below the pinch-in regime at low V_{BE} . So, the J_C is controlled from $1.8 nA \cdot \mu m^{-2}$ to $17.5 \mu A \cdot \mu m^{-2}$ with V_{BE} set at 0.5V, 0.525V and 0.55V.

$$BV_{CBO} = V_{CEt} - V_{BE} \quad (6)$$

with V_{CEt} extracted when slope crosses the x-axis.

The BV values are automatically extracted from the measurement data using a Python script. Fig 2. shows how the BVs are extracted using the tangent method. For BV_{CEO} , two tangent lines are traced along the $|J_B|$ drops, and the BV is extracted where the tangents lines intersect. As for the BV_{CBO} , one tangent line is traced where J_C tends to infinite, the BV is taken where the tangent line crosses the x-axis and calculated through equations (6). Therefore, the points to trace the tangent line are chosen at the middle of the drop or the middle of the infinite increase to fit perfectly the curve slope. Three values of V_{BE} are selected allowing bias conditions study and greater confidence in the results. For each BV measurement five transistors per A_E dimensions are measured, and the mean value is plotted with error bar computed thanks the standard deviation method.

The measurement has been performed on B55X devices for different Emitter dimensions, (see Fig 3). The dimensions are chosen to cover the reference dimensions and different width for a same length or reversely allowing form factor study dependencies.

3. Breakdown Voltage Study

3.1. BV_{CEO} and BV_{CBO} extraction against HiCuM/L2

Fig 4. presents the results of the forced V_{CE} (destructive) and the forced J_C setups BVs extraction methodology simulated through HiCuM L2 with model cards extracted through the typical extraction flow of HiCuM [6] using forced voltage setups. The results show no difference between the two setups, validating J_C forced setup for BVs extraction. Fig 5. and Fig 7. shows the measurements and simulations of BV_{CBO} and BV_{CEO} extracted through the extraction routine presented in **Section 2** as a function of A_E for the three Base current densities. Measurements and HiCuM L2 show same BV tendencies confirming the extraction routine viability and good agreement between HiCuM L2 and measurements. A slight difference is observed regarding the value of the different BVs. This difference is negligible regarding the BVs dispersion and is due to the model cards optimized for the reference dimension $0.2 \times 5 \mu m^2$.

On Fig 5,6,7,8. measurement error bars are negligible compared to the difference between two form factors allowing a qualitative study of the results. On Fig 5., the DUT with the lowest L_E ($0.45 \mu m$) features the lowest BV_{CEO} , with $BV_{CEO}=1.57V$ for $J_B=655nA.\mu m^{-2}$. The higher $BV_{CEO}=1.65V$ is reached by the larger device in terms of A_E and W_E for $J_B=1\mu A.\mu m^{-2}$. On Fig 6. is presented the BV_{CEO} versus the W_E for device featuring $L_E=5\mu m$. BV_{CEO} exhibits a positive linear dependence with W_E as well as an increase for higher J_B . The W_E dependance is mainly due to the increasing self-heating for larger W_E as regarding the J_B , indeed for higher J_B the device is driven in self-heating regime, leading to an additional increase of J_B for a given V_{CE} . Then the base current is reversed at higher V_{CE} i.e. higher II level.

On Fig 7., the BV_{CBO} values for $V_{BE} = 500mV$ in the range of between 5.1V and 5.35V and between 5V and 5.25V for $V_{BE} = 550mV$. On Fig 8., it can be highlighted a negative linear dependence with W_E and a decrease of BV_{CBO} for an increasing V_{BE} . Regarding the form factors dependence, larger W_E leads to an increase of II for the Base-Collector Junction due to the electric field management which depends on the form factors. In addition, the II

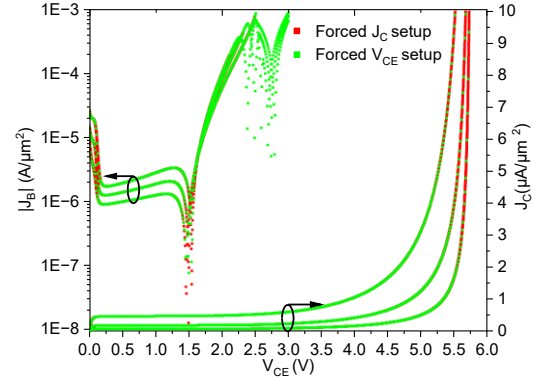


Fig 4. J_B, J_C for Forced J_C and V_{CE} setups from HiCuM L2.

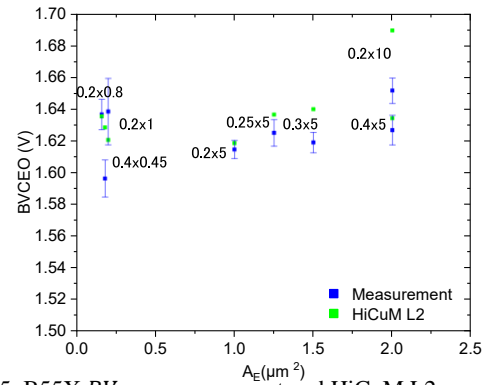


Fig 5. B55X BV_{CEO} measurement and HiCuM L2 simulation versus Emitter Area for $J_B=1\mu A.\mu m^{-2}$.

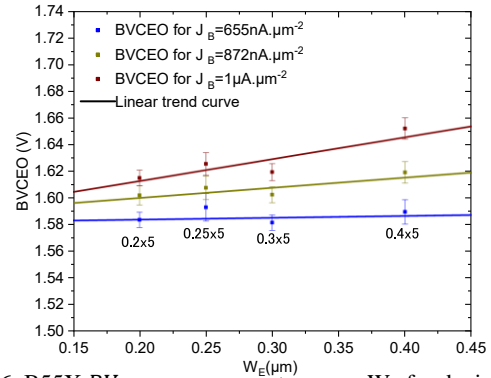


Fig 6. B55X BV_{CEO} measurements versus W_E for device featuring $L_E=5\mu m$ for the three V_{BE} .

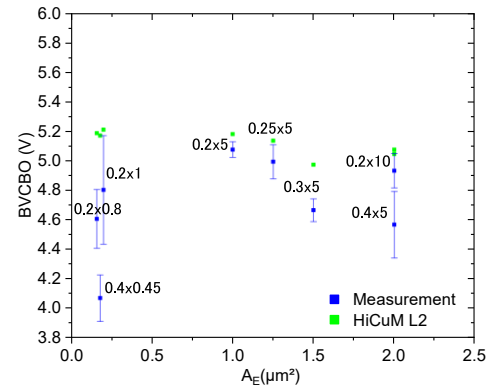


Fig 7. B55X BV_{CBO} measurement and simulation versus A_E for $V_{BE}=550mV$.

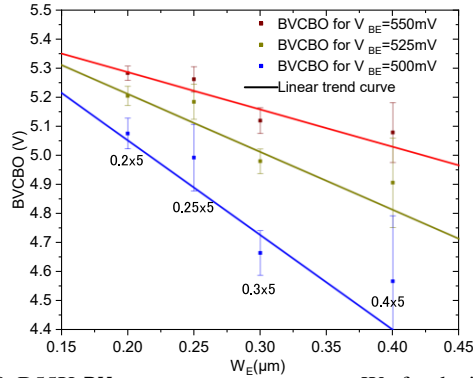


Fig 8. B55X BV_{CBO} measurements versus W_E for device featuring $L_E = 5 \mu m$ for the three V_{BE} .

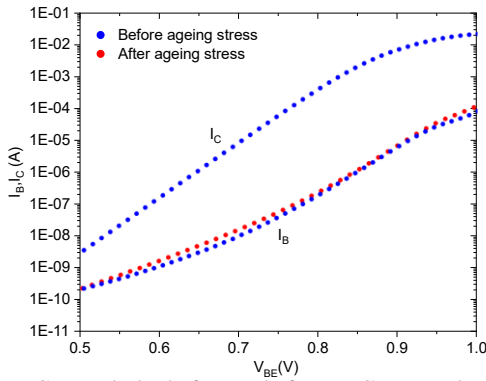


Fig 9. Gummel plot before and after a DC Forward stress of a B55X NPN HS device featuring $0.2 \times 5 \mu m$.

becomes more significant with the V_{BE} for a given V_{CE} then BV_{CBO} is reached at lower V_{CE} .

3.2. Application to Breakdown Voltage ageing

A DC Forward stress at $25^\circ C$ applying a $V_{BE}=0.85V$, $V_{CE}=2.75V$ (Yellow point in Fig 1.), choose beyond BV_{CEO} to assess the DUT reliability in a reasonable time range (30min), is performed on a HS B55X device featuring $A_E=0.2 \times 5 \mu m$. Fig 9. presents the result on a Gummel plot before and after stress. Due to Hot-Carrier-Degradation (HCD), I_B shows a positive drift, higher for V_{BE} below $0.8V$ [7,8]. The BVs extraction methodology is applied before and after the stress and results are shown on Fig 10. One observes a positive drift of BV_{CEO} around $0.01V$, and a slight negative drift of the BV_{CBO} around $0.1V$. The BV_{CEO} drifts are mainly due to the increase of I_B inducing of higher level of Π to reach BV_{CEO} . Regarding the BV_{CBO} drift, it might result from a degradation of the Emitter series resistances or an evolution of the electric field due to traps creation. The Gummel plot is a restrictive figure which does not show all the degradations of the DUT.

Conclusion

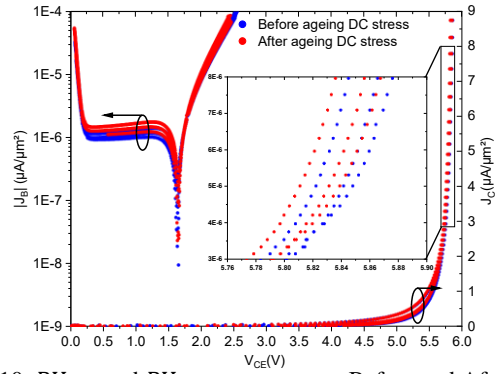


Fig 10. BV_{CEO} and BV_{CBO} measurement Before and After DC Forward stress performed on a B55X NPN HS device featuring $A_E = 0.2 \times 5 \mu m^2$.

In conclusion, the measurement setup and extraction methodology to study the SOA and the BVs are validated against the HiCuM simulation and the forced V_{CE} method for the BVs extraction. The forced J_C setup allows a non-destructive study of the BVs enabling before and after ageing measurements. The measurements performed on B55X technology show a dependence of the BVs with Emitter dimensions, mostly the Emitter Width. A study of the BVs after HCD showing slight degradations have been performed. The non-destructive methodology BVs extraction shows precise results, opening BVs ageing study through other stress levels/types or form factors.

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