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# A 100 V Input Common-Mode Range Compact Three-Step Incremental ADC Architecture Evaluation Achieving 101.48 dB SNDR and $6.46 \mu\text{V}_{\text{RMS}}$ Input-Referred Noise

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**Abstract**—This work presents a novel system-level architecture for the Three-Step Zoom-Incremental-Extended-Counting Analog-to-Digital Converter (ADC), designed to minimize area and power consumption while maintaining high resolution. It requires only a single sampling stage, integrator, multi-bit Digital-to-Analog Converter and 1.5-bit comparator across all three conversion phases, eliminating the need for additional interfacing circuits.

The proposed ADC is tailored for High-Voltage (HV) applications, operating within a constrained design space compared to standard literature. It achieves unprecedented HV Input Common-Mode capabilities of 100 V and the highest peak SNDR among HV ADCs, with the smallest sampling capacitance (1.25 pF), area ( $0.45 \text{ mm}^2$ ) and power consumption (240  $\mu\text{W}$ ). Unlike higher-order free-running  $\Delta\Sigma$  modulators in HV literature, this design employs a simpler first-order incremental conversion, enabling input multiplexing and further simplifying the design. To our knowledge, it is also the first Zoom-Incremental-Extended-Counting ADC architecture with HV capabilities.

Operating at a sampling frequency of 1 MHz, the proposed ADC achieves a simulated Signal-to-Noise-and-Distortion-Ratio of 101.48 dB and input-referred noise of  $6.46 \mu\text{V}_{\text{RMS}}$ , for a conversion time of 4.14 ms. Expected area is  $0.45 \text{ mm}^2$  in a  $0.11\text{-}\mu\text{m}$  BCD technology, making it highly suitable for space-constrained, power-efficient HV monitoring systems.

**Index Terms**—Incremental ADC, Zoom ADC, Extended-Counting ADC, Three-Step ADC, High-Voltage ADC.

## I. INTRODUCTION

The market for high-resolution, low-bandwidth Analog-to-Digital Converters (ADCs) with input multiplexing capabilities has been growing significantly over the last few years. These ADCs are required in a wide variety of applications, ranging from audio processing to biomedical signal acquisition. Battery Management Systems (BMS) applications also need high-resolution, low-bandwidth multichannels ADCs. However, these applications require High-Voltage (HV) capabilities and high integration potential, increasing design complexity.

This surge in demand has driven significant advancements in ADC design. Notably, the Zoom-Incremental ADC (Zoom-IADC) [1] and the Extended-Counting Incremental ADC (EC-

IADC) [2] are two architectures that achieve excellent power efficiency while maintaining high resolution (16+ bits).

Additionally, combining the Zoom-IADC and EC-IADC architectures further improves resolution for a given conversion time [3]. However, interfacing these two architectures to optimize the tradeoff between accuracy, conversion time, and power consumption presents challenges. The Zoom-IADC process significantly reduces the input swing of the IADC integrator by employing pseudo-multi-bit quantization, which enhances the Signal-to-Noise Ratio (SNR) for a given Oversampling Ratio (OSR). This approach relaxes the analog requirements for the integrator, enabling simpler architectures with reduced power consumption. Conversely, the EC-IADC relies on quantifying the residual voltage at the integrator's output, which is affected by the reduced swing.

To address this, it is often necessary to generate additional reference voltages ( $V_{\text{REF}}$ ) or amplify the residue before Extended-Counting (EC) quantization to extract meaningful information with a low number of bits (4-8). This quantization is typically performed using Successive Approximation Register (SAR) [3], [4] or IADC approaches [2], which require input amplitudes relevant to their full scale.

Adding extra gain or  $V_{\text{REF}}$  circuits also increases the circuit's footprint. Area considerations are increasingly critical for high-performance ADCs, and are sometimes even included in traditional Figures-of-Merit [5]. On top of that, extra sampling capacitors and circuits lead to higher area costs in HV technology, typically necessitating a Bipolar-CMOS-DMOS (BCD) process. HV sampling capacitors usually have lower density.

In this context, we propose a novel architecture that maximizes hardware-reuse for the Zoom-Extended-Counting-Incremental ADC (Zoom-EC-IADC) Three-Step conversion and simplifies  $V_{\text{REF}}$  generation for the EC phase. The design is sized for future integration in a  $0.11\text{-}\mu\text{m}$  BCD technology, targeting a compact HV BMS application.

## II. PROPOSED THREE-STEP INCREMENTAL ADC

### A. 1st-order Zoom-Incremental ADC

Fig. 1 shows the simplified architecture of the proposed Zoom-IADC. The Zoom output ( $k$ ) updates the references of the IADC with 2 LSB of over-ranging, such that  $V_{\text{REF-}} = (k-1) \cdot V_{\text{LSB}} \leq V_{\text{IN}} \leq V_{\text{REF+}} = (k+2) \cdot V_{\text{LSB}}$ , where  $V_{\text{LSB}}$  is the quantization step of the fine incremental modulator.

We chose a 1.5-bit comparator to reduce further the integrator swing while enforcing linearity. The Zoom-IADC thus has a symmetric comparison stage and dissymmetric feedback. Let  $D_0$ ,  $D_1$  be the output of respectively the first and second comparator. Then,

$$V_{\text{DAC}}[i] = \begin{cases} (k+2) \cdot V_{\text{LSB}, N_{\text{ZOOM}}} & \text{if } D_1[i]D_0[i] = 10 \\ k \cdot V_{\text{LSB}, N_{\text{ZOOM}}} & \text{if } D_1[i]D_0[i] = 01 \\ (k-1) \cdot V_{\text{LSB}, N_{\text{ZOOM}}} & \text{if } D_1[i]D_0[i] = 00 \end{cases} \quad (1)$$

Let  $x_1[i]$  be the integrator output voltage during the  $i$ -th incremental cycle. Then,  $D_0$ ,  $D_1$  relate to  $x_1[i]$  as follows:

$$D_1[i]D_0[i] = \begin{cases} 10 & \text{if } \frac{1}{4}V_{\text{LSB}, N_{\text{ZOOM}}} < x_1[i] \leq V_{\text{LSB}, N_{\text{ZOOM}}} \\ 01 & \text{if } -\frac{1}{4}V_{\text{LSB}, N_{\text{ZOOM}}} \leq x_1[i] \leq \frac{1}{4}V_{\text{LSB}, N_{\text{ZOOM}}} \\ 00 & \text{if } -V_{\text{LSB}, N_{\text{ZOOM}}} \leq x_1[i] < -\frac{1}{4}V_{\text{LSB}, N_{\text{ZOOM}}} \end{cases} \quad (2)$$

Such a first-order Zoom IADC is presented in Fig. 1.

### B. 1st-order Extended-Counting Incremental ADC

For the EC-IADC, the residue at the output of the integrator of a 1st-order Zoom-IADC holds information regarding the quantization error of the incremental conversion. Let  $\omega_0$  be the gain of the integrator,  $x_1[N]$  the voltage at the integrator

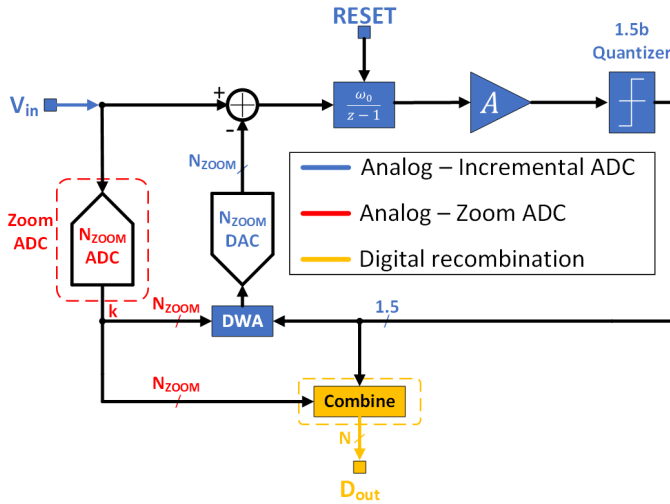


Fig. 1. 1.5-bit Zoom-IADC

output after  $N$  incremental cycles,  $u$  the ADC input,  $\hat{u}$  the ADC output and  $e_q$  the quantization error. Then,

$$\begin{cases} u = \hat{u} - e_q \\ e_q = \frac{x_1[N]}{\omega_0 \cdot N} \end{cases} \quad (3)$$

It is possible to quantize  $e_q$  and subtract it from the Zoom-IADC approximation,  $\hat{u}$ , to significantly increase the resolution of the ADC in a few clock cycles, without increasing further the OSR. However, as mentioned before, when combining Zoom and Extending-Counting approaches, the residue quantization becomes trickier if we want to do it using a simple, low-resolution ADC.

### C. Maximal-Hardware-Reuse Three-Step conversion

We propose a Zoom-EC-IADC architecture using only 1 HV sampler, 1 integrator, 1 multi-bit DAC, 1 1.5-bit comparator and digital logic as needed. The resulting system is shown on Fig. 2 through the 3 conversion phases. As illustrated in Fig. 2 (b), Correlated Double Samplings allows to handle the HV Common-Mode by canceling it out at the input of the system.

1) *Zoom Conversion*: First, we sample the input and store the sampled value onto the integrating capacitor. Next, we perform a pseudo-SAR algorithm on the sampled voltage, as pictured in Fig. 2 (a):

- A portion of  $V_{\text{REF}}$  is either added or subtracted from the integrated value.
- The resulting voltage is compared to 0 using one of the two comparators.
- Comparison result determines the next step of the pseudo-SAR algorithm.

Portions of  $V_{\text{REF}}$  are generated from the multi-bit DAC.

2) *Incremental Conversion*: Input sampling resumes, as shown in Fig. 2 (b). The recombination of the 1.5-bit comparator output with the  $N_{\text{ZOOM}}$ -bit Zoom conversion result produces the data stream for the incremental approximation.

To ensure satisfactory performance, even in the presence of capacitor mismatch in the multi-bit DAC, we perform Data Weighted Averaging (DWA) on its unit capacitors.

3) *Extended-Counting Conversion*: At the end of the IADC phase, we transition to the EC phase, as shown in Fig. 2 (c). The residue to be quantized is stored on the integration capacitor of the integrator at the end of the incremental conversion. This eliminates the need for transferring the residue to another stage, enhancing robustness and power efficiency.

The full-scale range of quantization in this phase is:  $[-V_{\text{REFEC}}; +V_{\text{REFEC}}] = [-V_{\text{LSB}, N_{\text{ZOOM}}}; V_{\text{LSB}, N_{\text{ZOOM}}}]$ , as shown in Eq. 2. This reduced range is enforced by the Zoom architecture, which limits the quantization error to  $\pm 1V_{\text{LSB}, N_{\text{ZOOM}}}$ .

$V_{\text{REFEC}}$  can be generated using a single unit capacitor from the main DAC thanks to hardware-reuse, simplifying the design immensely compared to the implementations in [3] or [4].

EC is performed using a Cyclic ADC scheme with 1.5-bit quantization, with comparator thresholds at  $\pm 0.25V_{\text{REFEC}}$ , using an extra capacitor matched to  $C_{\text{int}}$  for residue doubling, commuted using the  $S3$  switches on Fig. 2 (c).

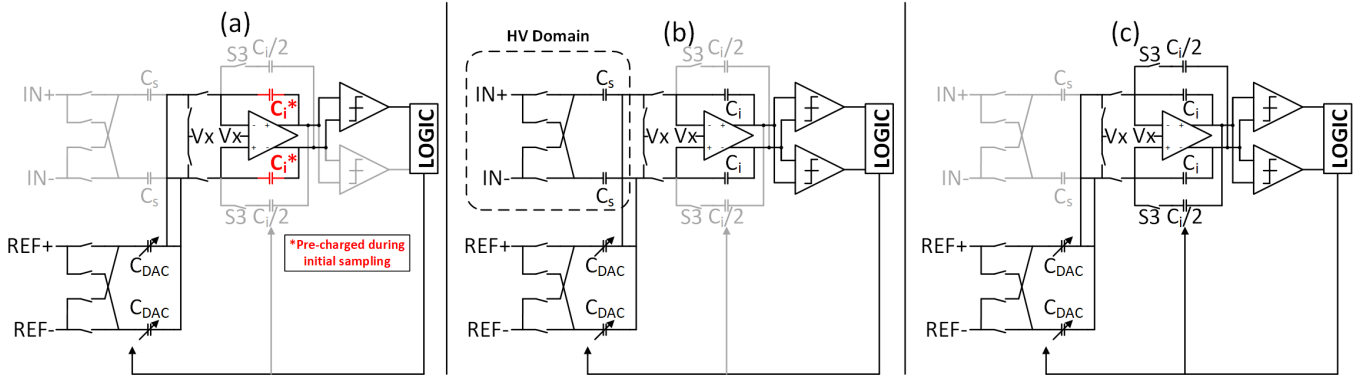


Fig. 2. Hardware-Reuse Three-Step Conversion (a) SAR-Zoom (b) 1.5-bit Incremental (c) Cyclic-Extended-Counting

As described in [6], we implement a 1.5-bit Redundant Signed Digit (RSD) correction scheme to correct comparator offsets up to  $\pm 0.25V_{REFEC}$ , making the EC conversion highly resilient to comparator offset.

### III. SIMULATION RESULTS

Simulation results are generated using a high-level MATLAB/Simulink model that accounts for noise and non-idealities. The following noise sources are considered: thermal sampling noise,  $V_{REF}$  and integrator thermal noise. Regarding non-idealities, the model includes the effects of capacitor mismatch in the multi-bit DAC, finite integrator gain and comparator threshold variations.

Components sizing is based on a 0.11- $\mu\text{m}$  BCD process. For the HV sampling capacitors, the tradeoff between thermal sampling noise and area resulted in  $C_{sens} = 1.25 \text{ pF}$ .

We set  $N_{ZOOM} = 5$  considering the tradeoff between the SNR improvement and area of the the unit capacitors of the main DAC. Similarly, Extended-Counting is performed on 7 bits considering the tradeoff between SNR improvement and conversion time. Global conversion time is then only determined by the OSR chosen for the IADC phase, going up to 4096 in our design.

The system operates under a 2.4 V power supply, with a full-scale input range of  $\pm 1.024 \text{ V}$  around the up to 100 V common-mode.

As illustrated in Fig. 3, we achieve a minimal input-referred noise of  $6.46 \mu\text{V}$ , for a conversion time of 4.14 ms. This guarantees that the ADC can reach 18 bits of peak-to-peak resolution under 5 ms of conversion time for the envisioned BMS application.

Peak SNDR was simulated at 101.48 dB, maintaining an INL of  $\pm 5.8 \text{ ppm}$ . Without DWA, SNDR falls to 87.83 dB, with an INL of  $\pm 13.2 \text{ ppm}$ . Capacitor mismatch was not considered during the EC phase, which could slightly degrade the INL.

Compared to the industrial state-of-the-art [9], our work achieves superior input-referred noise performance, approaching the performance levels reported in the literature [1] for low-voltage architectures.

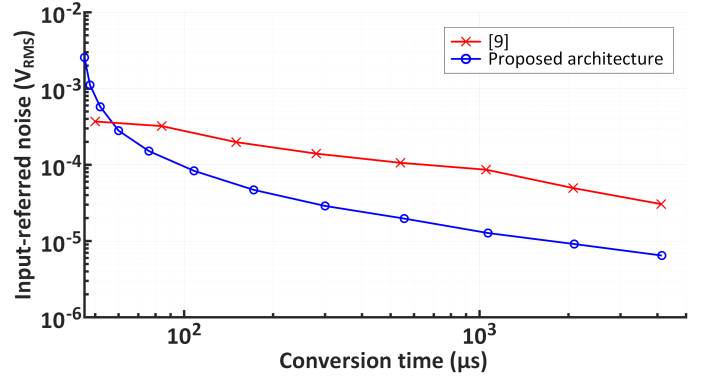


Fig. 3. Simulated input-referred noise for a full-scale input

To better highlight the design constraints, we propose a modified Schreier Figure-of-Merit (FoM),  $FoM_{ScHV}$ , based on the suggestions in [5]. In [10], it has recently been suggested crediting designs with a lower input swing, since they are easier to drive [10], with the correction factor  $F_{Swing}$ . We introduce two additional correction factors,  $F_{CM}$  and  $F_{kTC}$ , to factor in HV design constraints.

$F_{CM}$  rewards handling HV common-mode, which require added power, area and design complexity.  $F_{kTC}$  rewards smaller sampling capacitance, as larger capacitance reduces sampling noise but is area-costly in HV designs.

Let  $CM_{HV}$  be the Common-Mode input voltage handled by the ADC, in V. For the sake of uniformity in the FoM,  $CM_{HV} = 1$  for low-voltage designs. Let  $V_{DD}$  be the supply voltage,  $V_s$  the input swing,  $C_s$  the sampling capacitance and  $FoM_{Sc}$  the Schreier FoM of a given ADC.  $\bar{C}_s$  is the average  $C_s$  of the considered family of designs. Then,

$$\begin{cases} F_{Swing} = 10 \cdot \log_{10}(V_{DD}/V_s) \\ F_{CM} = -10 \cdot \log_{10}(1/CM_{HV}) \\ F_{kTC} = -10 \cdot \log_{10}(C_s/\bar{C}_s) \end{cases} \quad (4)$$

$$FoM_{ScHV} = FoM_{Sc} + F_{Swing} + F_{CM} + F_{kTC} \quad (5)$$

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

	This work <sup>a</sup>	[7] <sup>b</sup>	[8] <sup>b</sup>	[9] <sup>b</sup>	[1] <sup>b</sup>	[2] <sup>b</sup>	[3] <sup>b</sup>	[4] <sup>b</sup>
<b>Year</b>	2025	2015	2017	2022	2013	2015	2024	2022
<b>Architecture</b>	Zoom-EC-IADC	$\Delta\Sigma$ ADC	$\Delta\Sigma$ ADC	IADC	Zoom-IADC	EC-IADC	Zoom-EC-IADC	Zoom-EC-IADC
<b>F<sub>S</sub> [kHz]</b>	1000	150	5000	1000	100	96	48.83	512
<b><math>\Delta\Sigma</math> order</b>	1	3	3	N/A	3	2	2	2
<b>Tech. [nm]</b>	110 (HV-BCD)	180 (HV-CMOS)	180 (HV-BCD)	N/A	160 (CMOS)	65 (CMOS)	180 (CMOS)	180 (CMOS)
<b>Area [mm<sup>2</sup>]</b>	0.45	0.8	0.53	N/A	0.35	0.20	0.20	2.5
<b>Power [<math>\mu</math>W]</b>	240	505	670	1728	6.3	10.7	0.96	130
<b>Supply [V]</b>	2.4	5	1.5	2.7	1.8	1.2	1.8	1.8
<b>Conversion time [ms]</b>	4.14	5	0.05	4.12	40	2	5.26	0.5
<b>Input CM range [V]</b>	100	$\pm 30$	30	85	N/A	N/A	N/A	N/A
<b>Input DM range [V]</b>	$\pm 1.02$	4.4	1	$\pm 0.16$	$\pm 0.9$	$\pm 1.1$	$\pm 0.9$	$\pm 0.9$
<b>Input-referred Noise [<math>\mu</math>V<sub>RMS</sub>]</b>	6.46	N/A	N/A	30.5	0.65	N/A	N/A	N/A
<b>SNDR<sub>max</sub> [dB]</b>	101.48	100.6	89	N/A	119.8	90.8	97.6	99.3
<b>C<sub>sens</sub> [pF]</b>	1.25	5	2.5	N/A	10.2	8	3.2	2.56
<b>INL [ppm]</b>	$\pm 5.8$	N/A	N/A	20	$\pm 6$	$\pm 15.25$	N/A	$\pm 7.25$
<b>FoM<sub>Sc</sub> [dB]<sup>c</sup></b>	158.50	153.57	160.74	N/A	182.78	164.49	177.56	168.16
<b>FoM<sub>SCHV</sub> [dB]<sup>c</sup></b>	184.91	171.61	179.99	N/A	179.39	159.52	179.20	170.77

<sup>a</sup>System-level simulation. <sup>b</sup>Measured.

<sup>c</sup>FoM<sub>Sc</sub> = SNDR + 10 · log<sub>10</sub>( $\frac{1}{2 \cdot T_{conv} \cdot Power}$ ). FoM<sub>SCHV</sub> derived from Eq. 5.

Based on this modified FoM, we can see that we achieve state-of-the-art performance.

Among the HV designs [7]–[9], we achieved the best SNDR and Common-Mode input range. Compared to the HV academic designs [7], [8], we have the smallest sampling capacitance, power consumption and area. We also use a much simpler first-order loop filter, and have access to input multiplexing thanks to the incremental architecture.

Compared to low-voltage designs [1]–[4], there remains room for improvement in the Schreier FoM, mainly because of the smaller sampling capacitance and lower  $\Delta\Sigma$  modulator order, both enforced by specific application constraints. It is also worth noting that the power consumption was sized conservatively for our design and will most likely be reduced during further design stages. It is also skewed by the added power consumption from the HV sampler.

#### IV. CONCLUSION

This work presents a novel Three-Step Incremental ADC architecture. By employing a maximal-hardware-reuse approach, the proposed design completely removes the need for additional interfacing circuits, usually necessary to handle proper Extended-Counting quantization.

The system-level simulated ADC proposes to achieves 101.48 dB SNDR and 6.46  $\mu$ V<sub>RMS</sub> input-referred noise for a conversion time of 4.14 ms and power consumption of 240  $\mu$ W within a compact area of 0.45 mm<sup>2</sup> in a 0.11- $\mu$ m BCD technology, with 100 V input common-mode range.

To our knowledge, it targets to be the first HV Zoom-EC-IADC, achieving similar system-level specifications as HV  $\Delta\Sigma$  state-of-the-art solutions, while significantly reducing chip

area and power consumption. The proposed work opens new paths for compact BMS applications.

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