Towards Monolithic GaN Power ICs : A Comparative Analysis of four All-GaN Gate Drivers

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Abstract*— The constraints associated with the combination of a silicon CMOS gate driver and a GaN power transistor have driven the development of fully integrated, monolithic all-GaN solutions. This monolithic integration eliminates parasitic inductances in the gate drive loop while also reducing the overall size of the driver-transistor system. This paper presents a comparative analysis of four all-GaN gate driver architectures. These architectures are designed and simulated using the 200V GaN-on-SOI design technology provided by IMEC through EUROPRACTICE and are evaluated based on three key parameters: total area, static losses, and propagation delay. The comparative study highlights the strengths and weaknesses of each architecture. The dual power supply architecture for example, with a total area of only 0.018 mm², can provide a pull-up current exceeding 120 mA while maintaining static losses below 50 mW. In contrast, bootstrap-based architectures require only one single power supply to deliver the same pull-up current but at the expense of increased area and static losses. A bootstrap-based GaN gate driver was fabricated and experimentally validated. Measurements showed a static current consumption of 6.8 mA and when connected to the low-side of a GaN Half-bridge, it showed fast switching and minimal ringing on the power transistor's drain voltage at 100 V and 1 A, validating the effectiveness of the monolithic design.

***Keywords*— GaN, gate driver, monolithic integration, GaN-on-SOI, Integrated circuit**

I. INTRODUCTION

Power electronics converters used into a variety of applications, such as laptop chargers for consumer electronics and on-board chargers for electric vehicles have seen an increasing demand in both better power efficiency and better power density over the last years. To meet these demanding specifications, the use of Gallium Nitride (GaN) power transistors is considered as a promising solution [1]. The high switching speed and low specific resistance of GaN power transistors enable the design of power converters operating at high frequencies (above 100 kHz), consequently reducing the converter size while maintaining low losses. However, the interaction between the GaN power transistors and their silicon CMOS gate drivers introduces parasitic inductances as shown in Fig. 1, causing electrical stress on the gate of the power device or limiting the maximum switching speed. The conventional approach to address this issue consists in increasing the gate resistance between the silicon CMOS gate driver and the power transistor. Nevertheless, this leads to slower switching transients, thereby losing one of the main advantages of GaN power transistors. Thanks to the physical structure of the lateral power GaN transistor, monolithic integration of a power GaN transistor with its gate driver on a single chip is possible, resulting in near-zero gate loop parasitic inductance [2]. In addition to reducing parasitic inductance in the gate loop, this monolithic integration offers a more compact system, reduces manufacturing costs for both chips and packaging, and simplifies the design and layout of power electronic converters [3]. The first introduction of a GaN switching cell integrated with high-side and low-side gate drivers was provided by [4]. Bootstrap gate driver architectures integrated with a GaN transistor are presented in [5], [6], [7] and [8]. While multiple gate driver circuits have been proposed, no comparative analysis showing the strengths and weaknesses of each architecture has been published. This paper presents a description and a comparative analysis of four all-GaN gate driver circuits. The comparative analysis is based on three main criteria: the static power consumption of the gate driver, its size, and its propagation delay. Section II provides an overview of the four gate driver topologies and their operating principles. Section III presents a comparative analysis of their performances and Section IV presents the experimental results of a power GaN switching cell with an integrated bootstrap GaN gate driver.

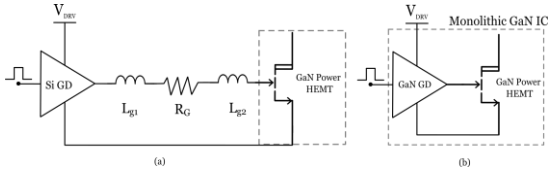

Fig. 1. (a) GaN HEMT with external silicon CMOS driver (b) GaN HEMT with integrated GaN gate driver

II. GATE DRIVER ARCHITECTURES

Although monolithic integration of multiple high voltage power components, as well as low-voltage components for analog and logic functions eliminates parasitic inductances, it also introduces challenges such as capacitive coupling through the shared substrate, back-gating effects, and isolation between different voltage levels within the chip. These challenges can be addressed using the GaN-on-SOI integration technology

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developed by IMEC. For the design of the GaN power integrated circuit in this study, we used the 200V GaN-on-SOI technology provided by IMEC through Multi-Project Wafer (MPW) via EUROPRACTICE. The MPW version of the 200V GaN-on-SOI integration technology includes four components: a 200V high-voltage e-mode GaN HEMT, a low-voltage e-mode GaN transistor, a 2DEG resistor, and a low-voltage MIM capacitor. Achieving state-of-the-art performance in integrated functions is thus challenging with this technology due to the absence of p-type and depletion-mode devices. Fig. 2 illustrates three types of gate driver output stages: a totem-pole structure, a push-pull structure, and a Resistor-Transistor-Logic (RTL) structure. To minimize the gate driver output stage losses, totem-pole and push-pull structures are generally preferred. Consequently, the absence of p-type components calls for the use of the push-pull configuration.

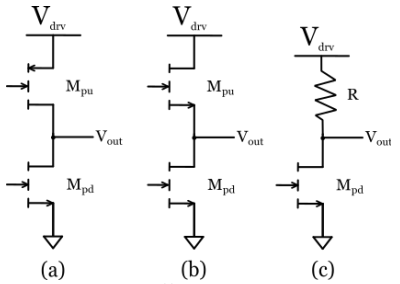

Fig. 2. Gate driver buffer stage: (a) Totem-pole, (b) Push-pull, (c) RTL

In this study, aside from the gate driver size, only the static power consumption and the propagation delay of the gate drivers are considered as relevant metrics for comparing the proposed driver architectures. Other parameters, such as dynamic power losses and total turn-on delay, are excluded from the comparative analysis because they are not solely determined by the gate driver itself but also depend on the characteristics of the power switch being driven. Specifically, dynamic power losses are not included in the comparison since all gate drivers are assumed to control the same power transistor, resulting in identical gate charge and switching conditions. These losses are given by the well-known equation:

$$P_{dyn} = Q_G . V_{drv} . F_{sw} \quad (1)$$

Where Q_G, V_{drv} and F_{sw} are the total gate charge, the driving voltage (assuming 0V turn-off) and the switching frequency respectively. As all these parameters are independent of the gate driver architecture (under the assumption of a common load), P_{dyn} does not provide a differentiating criterion. For timing analysis, two definitions of delay times are introduced for clarity: the propagation delay of the gate driver at turn-on named t_d and the turn-on delay named $t_{d_{on}}$. t_d refers to the intrinsic delay of the gate driver, defined as the time required for the driver to begin changing its output in response to a transition on its input at turn-on. More precisely, it can be interpreted as the time needed to charge the pull-up transistor to its threshold voltage. $t_{d_{on}}$ corresponds to the time interval between the rising or falling edge of the input control signal and the moment the power transistor reaches its fully conducting state. This turn-on delay is the sum of the gate driver's propagation delay and the time required to charge the gate of the power transistor. The latest depends on the transistor's gate capacitance and the available gate current, then, it does not only depend on the gate driver characteristics. Therefore, the focus of the comparison analysis is restricted to metrics that are inherent to the gate driver itself which are the propagation delay, the static power consumption and the size.

A. *Architecture A*

Fig. 3 presents the dual power supply architecture [4]. It mainly consists of a buffer stage and an inverter stage. The inverter stage not only serves as a pre-amplification stage but also ensures the complementarity of the control signals for M_{pu} and M_{pd}. The dual power supply gate driver ensures output rail-to-rail voltage when $V_{drvH} > V_{drvL} + V_{th_{pu}}$ where $V_{th_{pu}}$ is the threshold voltage of the pull-up transistor. The propagation delay of the PWM signal at turn-on is defined as the time required to charge the input capacitance $C_{iss_{pu}}$ of the pull-up transistor to its threshold voltage $V_{th_{pu}}$. It is given by:

$$t_{d_A} = -R_1 C_{iss_{pu}} * \ln(1 - \frac{V_{th_{pu}}}{V_{drvH}}) \quad (2)$$

The static power consumption is given by:

$$P_A = \frac{{V_{drvH}}^2}{R_1 + R_{d1}} \quad (3)$$

where R_{d1} is the resistance of transistor M_1.

Increasing R_1 thus reduces the static consumption, but it also increases the propagation delay. This results in the well-known trade-off between static power losses and propagation delay. The main disadvantage of this circuit is that it requires two external power supplies. However, the voltage V_{drvL} can be generated from V_{drvH} using a Low Drop-Out voltage regulator, at the cost of additional losses. To mitigate the main disadvantage of this circuit, V_{drvH} can be generated from V_{drvL} within the chip using bootstrap architectures.

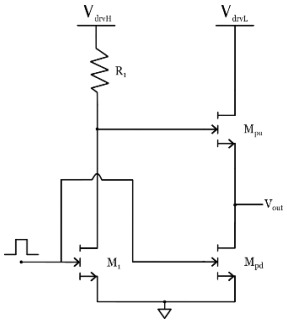

Fig. 3. Gate driver architecture A

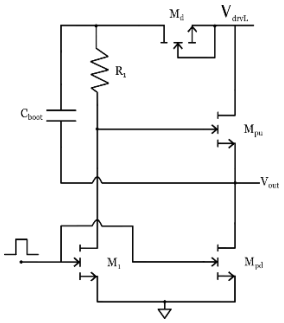

Fig. 4. Gate driver architecture B

B. *Architecture B*

Fig. 4 illustrates a driver with a bootstrap circuitry introduced in [5]. Given that no diode is available in the design kit, transistor M_d with its gate shorted to its source is then used as a diode-connected transistor. This configuration allows current to flow in reverse through M_d when $V_S > V_D$ with V_S

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and V_D being the source voltage and drain voltage of M_d respectively. The threshold voltage of these diode-connected transistors is high (~2V-2.5V), which results in a low voltage across the capacitor C_{boot}. This low voltage requires the use of a large pull-up transistor to supply a significant current to the gate of the power device, which in turn implies a high bootstrap capacitance value. Therefore, the bootstrap capacitor can take a relatively significant area within the driver, which is the main drawback of this architecture. The propagation delay is given by:

$$t_{d_B} = -R_1 C_{iss_{pu}} * \ln(1 - \frac{V_{th_{pu}}}{V_{C_{boot}}}) \quad (4)$$

where $V_{C_{boot}}$ is the voltage across the bootstrap capacitor. The static power consumption is given by:

$$P_B = \frac{{V_{drv_L}}^2}{R_1 + R_{d1}} \quad (5)$$

where R_{d1} is the resistance of transistor M_1.

C. Architecture C

By using the circuit shown in Fig. 5, similar to the one introduced in [7], it is possible to reduce the value of the bootstrap capacitor while maintaining the same pull-up current. Carefully sizing R_2 and M_2 ensure that $V_{GS_{pu}} > V_{C_{boot}}$ during the power transistor's turn-on transient. The propagation delay is given by:

$$t_{d_C} = -R_1 C_{iss_{pu}} * \ln(1 - \frac{V_{th_{pu}}}{V_{boot}}) \quad (6)$$

with $V_{boot} = V_{drvL} + V_{C_{boot}}$ where $V_{C_{boot}}$ is the voltage across the bootstrap capacitor. The static consumption is given by:

$$P_C = V_{drvL}^2 (\frac{1}{R_1 + R_{d1}} + \frac{1}{R_2 + R_{d2}}) \quad (7)$$

where R_{d1} is the resistance of transistor M_1 and R_{d2} is the resistance of M_2.

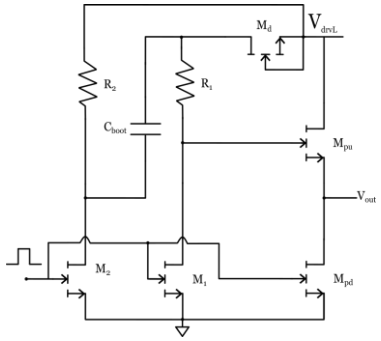

Fig. 5. Gate driver architecture C

D. Architecture D

To further reduce the value of the bootstrap capacitor and, consequently, the total size of the gate driver, one can use the gate driver with pump charge circuitry presented in Fig. 6 and similar to the one introduced in [8]. In this architecture, instead of operating M_{d1} as a diode-connected transistor with a high threshold voltage, a capacitor C_{boot2} is used to operate it in the linear region, thereby allowing the main bootstrap capacitor C_{boot_1} to be charged to almost V_{drvL}. The bootstrap voltage can then be close to $2V_{drvL}$. Despite the fact that this circuit can effectively reduce the size of the driver, the 3 inverters induce more propagation delay and losses than the other architectures. Another disadvantage of this technique is the increased complexity compared to the other architectures. The propagation delay is given by:

$$t_{d_D} = -R_3 C_{iss_2} * \ln\left(1 - \frac{V_{th_2}}{V_{drvL}}\right) - R_1 C_{iss_{pu}} * \ln\left(1 - \frac{V_{th_{pu}}}{V_{boot}}\right) \quad (8)$$

where C_{iss_2} and V_{th_2} are the input capacitance and treshold voltage of transistor M_2 respectively and $V_{boot} = V_{drvL} + V_{C_{boot1}}$. The static power consumption is given by:

$$P_C = {V_{drvL}}^2 (\frac{1}{R_1 + R_{d1}} + \frac{1}{R_2 + R_{d2}} + \frac{1}{R_3 + R_{d3}}) \quad (9)$$

where R_{d1}, R_{d2} and R_{d3} are respectively the resistance value of M_1, M_2 and M_3.

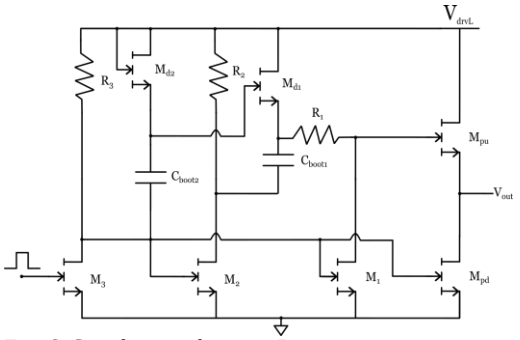

Fig. 6. Gate driver architecture D

III. Comparative Analysis

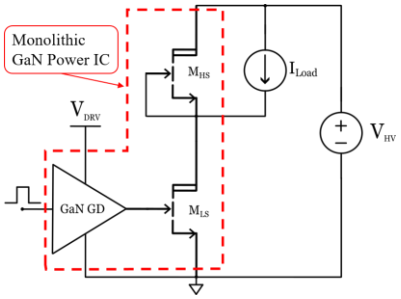

Fig. 7. Integrated gate driver simulation test bench

Fig. 7 presents the setup used to compare the performances of the different gate driver architectures. The gate driver is connected to the Low-side device of a power GaN switching

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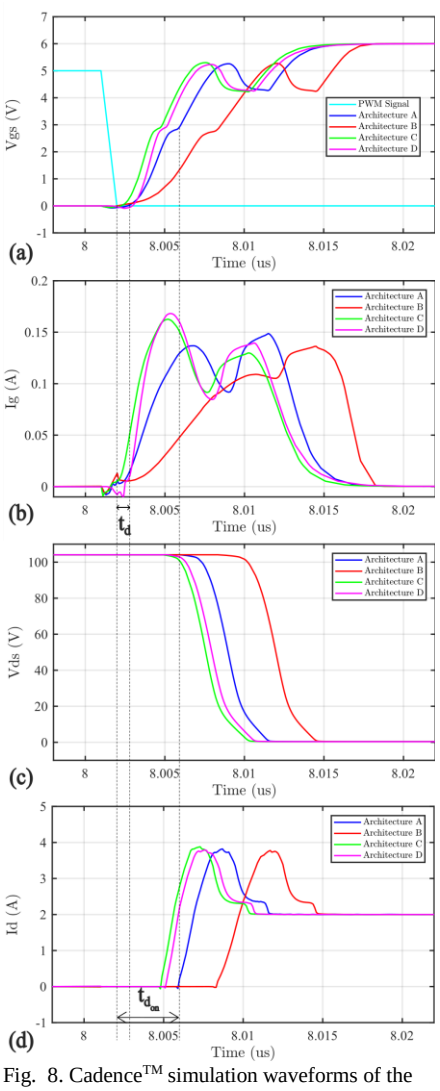

Fig. 8. Cadence™ simulation waveforms of the Low-side power GaN during turn-on using low-delay gate drivers: (a) gate-source voltage, (b) gate current, (c) drain-source voltage, (d) drain current

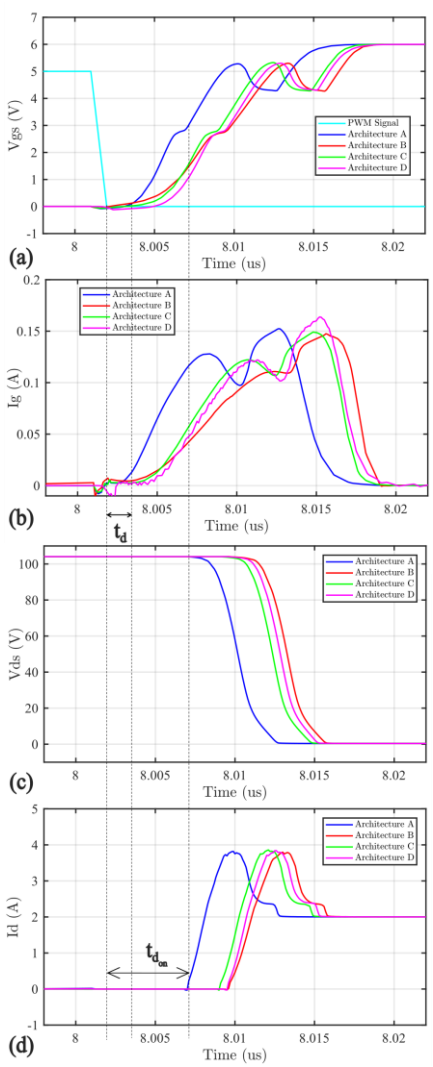

Fig. 9. Cadence™ simulation waveforms of the Low-side power GaN during turn-on using low-loss gate drivers: (a) gate-source voltage, (b) gate current, (c) drain-source voltage, (d) drain current

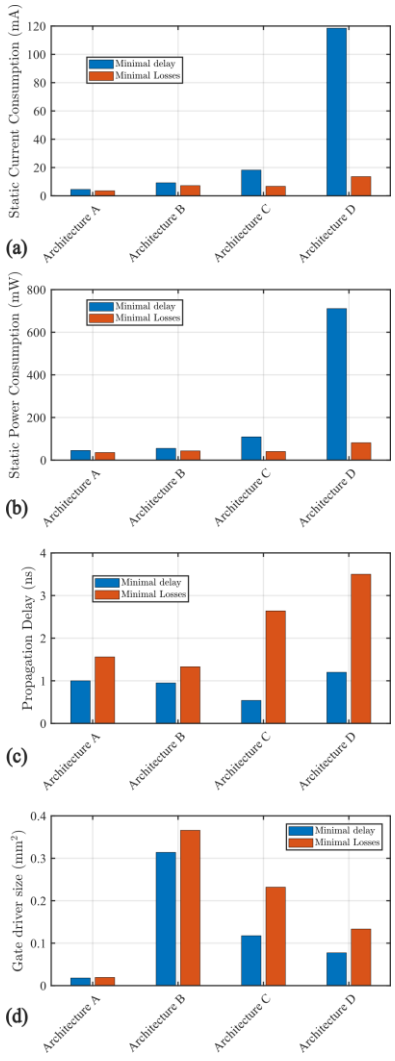

Fig. 10. Comparative analysis of the gate drivers: (a) current consumption, (b) Power consumption, (c) propagation delay, (d) size

cell and the High-side is diode-connected. In order to obtain a fair comparison, all circuits must meet the same specifications. V_{drvL} is fixed at 6V for each circuit to drive the power device. V_{drvH} is fixed at 10V for architecture A. For the bootstrap and pump-charge architectures, the main bootstrap capacitor is 10 times bigger than the input capacitance of the pull-up transistor. The pull-down transistor is the same for all the architectures to ensure that the Low-side power transistor turn-off transient is the same. For the turn-on transient, the goal is to get a mean $\frac{dV_{DS}}{dt}$ of 30 V/ns. This value is typical for 200 V class GaN devices switching 100 V and below. The gate drivers must then provide around 120 mA of pull-up current during the dv/dt sequence of the turn-on transient of the power device, based on the size of the GaN power transistor. For each circuit, two designs have been made: one with the lowest propagation delay and one with the lowest losses. The simulation parameters are given in TABLE I and the parameters of the power device are given in TABLE II. Fig. 8 and Fig. 9 illustrates the Low-side power transistor turn-on switching waveforms for the four gate driver circuits designed with the lowest propagation delay and the lowest static losses respectively. Finally, Fig. 10 presents the performance of all four gate drivers in regards to the three main criteria: static losses, propagation delay and size.

TABLE I. Simulation Parameters

Name	Parameter description		
	Description	***Value***	***Unit***
V_{HV}	Input bus voltage	100	V
I_{Load}	Output load current	2	A
α	Duty-cycle	0.5	n.u.
F_{sw}	Switching frequency	500	kHz

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TABLE II. Power GaN device parameters

Name	Parameter description		
	Description	*Value*	*Unit*
W_G	Gate width	36	mm
L_G	Gate length	1.3	µm
V_{th}	Threshold voltage	2.3	V
$R_{DS_{on}} @ V_{GS} = 6V$	On resistance	0.2	Ω

In Fig. 8, extremely low propagation delays ($\sim 1\,ns$) between the PWM control signal and the power transistor gate-source voltage waveforms can be observed for all architectures. Although the gate current waveforms provided by each gate driver does not perfectly match those of an ideal current source, the expected values during the Miller plateau are consistent, ensuring a mean $\frac{dV_{DS}}{dt}$ of $30\,V/ns$ at turn-on. Fig. 9 shows increased propagation times due to the minimization of static losses. Nevertheless, the expected switching speed is maintained, as shown by the gate current waveforms (around $120mA$ at Miller plateau). Fig. 8 and Fig. 9 show the difference between t_d and $t_{d_{on}}$ for circuit A. The advantages and disadvantages of each architecture can be found from Fig. 10. Although simple, circuit A appears to be the optimal solution due to its superior performance compared to the other architectures. However, its main drawback, as previously mentioned, is the requirement for an external dual power supply. Despite its low static power consumption, circuit B requires a larger driver area to achieve the same performance. On the other hand, circuit D significantly reduces the driver size at the cost of much higher static losses. Circuit C, therefore, emerges as the ideal trade-off between these two circuits.

IV. Experimental Results

Among the various driver topologies studied, Circuit C (lowest losses version) was selected for experimental validation due to its performances balancing those of Circuits B and D. Fig. 11 presents a microscopic view of the fabricated die, which integrates several circuit variants. These include both low and high-voltage elementary components, standalone gate driver configurations, and other test patterns. The chip was packaged in a QFN56 package for evaluation.

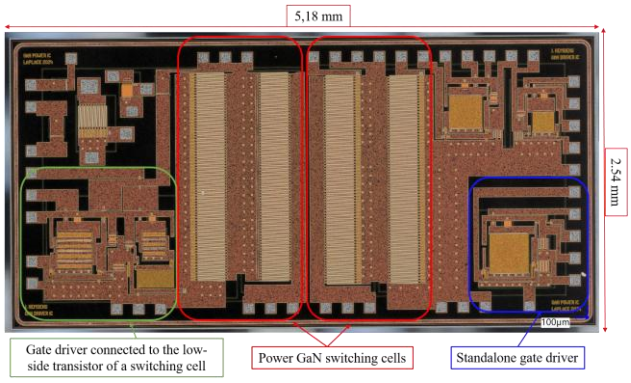

Fig. 11. Microscopic view of the fabricated GaN IC

A dedicated evaluation board (Fig. 12) is designed to characterize the proposed driver's performance under both static and dynamic conditions. An SN74AC04MDREP logic inverter is used to counteract the inherent signal inversion introduced by the internal gate driver architecture.

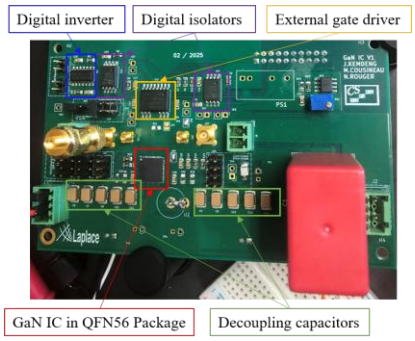

Fig. 12. Evaluation Board to test all integrated GaN functions and variants

Additionally, ADuM210N digital isolators are employed to ensure propagation delay matching between the high-side and low-side gate driver control signals (when the high-side transistor is not diode-connected). A commercial gate driver (2EDR7259) is also implemented on the same board to allow a direct comparison between the integrated solution and a discrete off-chip driver, driving the same GaN transistor (this comparative study lies outside the scope of the present article). PWM signals are generated by a dsPIC33CK microcontroller, which provides high-precision timing with a resolution of 2.5 ns. The microcontroller outputs a 0–3.3 V PWM signal, which is level-shifted to a 0–5 V logic level suitable for the gate driver input. The test bench, shown in Fig. 13, enables high-resolution measurements of the gate driver's output and the switching behavior of the power stage.

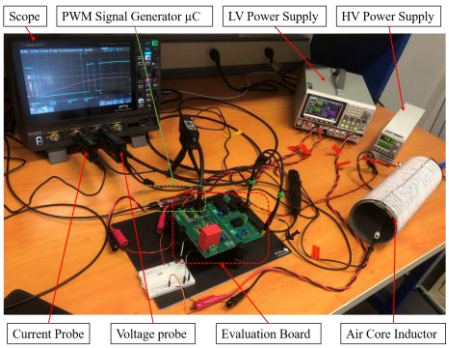

Fig. 13. Experimental setup to evaluate the GaN gate driver and monolithic power IC

A. GaN Gate driver on capacitive load

On the die picture (Fig. 11), the gate driver highlighted in blue is intended for standalone testing with a capacitive load. The gate driver input and output voltage are measured using 350 MHz bandwidth passive probes and a 12 bit (architecture) 500 MHz oscilloscope. The gate driver's output is connected to an external surface mounted 33 pF capacitor. Fig. 14 shows the

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input PWM signal and the corresponding output at the load capacitor. Static current consumption is 6.8 mA at $V_{drv_L} = 6$ V corresponding to 40.8 mW of static losses closely matching the simulated value (40.44 mW). Turn-on propagation delay measured between the 80% falling edge of the driver's input signal and the 20% rising edge of the driver's output is approximately 9.16 ns (Fig. 15), over 3 times higher than simulated. This is due to the parasitic capacitance introduced on the PCB between the bootstrap node trace and the ground plane on the PCB inner layer 1. This parasitic capacitance slows down the rise of the bootstrap voltage and prevent it from reaching the expected value. This also explains why the gate driver's output voltage does not reach exactly 6 V. This issue can be solved by removing the ground plane beneath the bootstrap node trace.

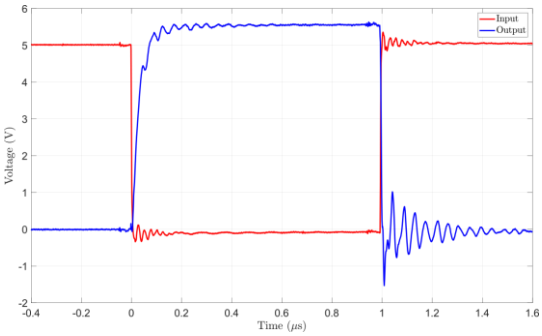
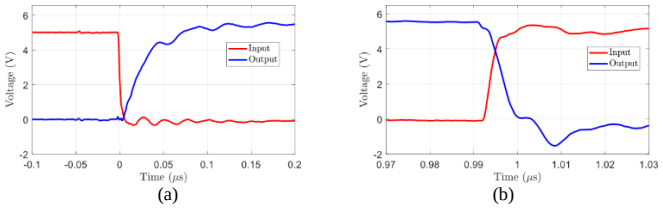


Fig. 14. Measured Input and Output voltage of the gate driver on capacitive load



(a) (b)

Fig. 15. ZOOM : Measured Input and Output voltage of the gate driver during load capacitor charge (a) and discharge (b)

B. *GaN switching cell with monolithically integrated low-side GaN gate driver*

The driver highlighted in green (Fig. 11) is internally connected to the low-side device of a GaN-based switching cell and is characterized with a Double Pulse Test (DPT). The high side GaN transistor is also integrated, but connected internally as a freewheeling diode. The experimental setup is similar to the one presented in Fig. 7 but the current source is replaced by a 215 µH air-core inductor. The parameters used for the DPT are the same as the ones in TABLE I except for the desired inductor current which has been set to 1 A instead of 2 A. The drain-to-source voltage of the low-side GaN transistor is captured using a MICSIG MOIP200P optical isolated probe with a 200 MHz bandwidth, while the inductor current is measured using a MICSIG CP503B Hall-effect probe with a bandwidth of 50 MHz. Fig. 16 and Fig. 17 show the switching waveforms of the low-side power transistor. The results demonstrate the gate driver's ability to effectively control a GaN power device, exhibiting clean switching behavior with minimal voltage overshoot (<10%), along with fast rise (12 ns) and fall (17 ns) times.

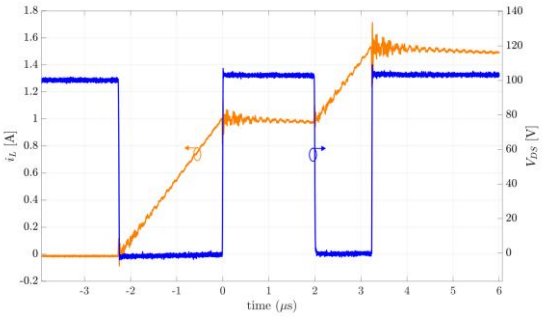
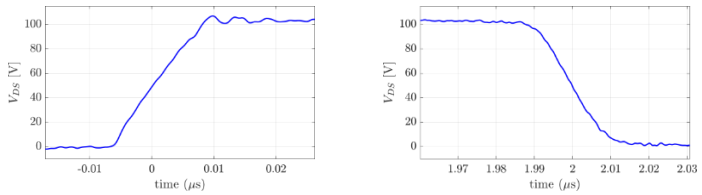


Fig. 16. Measured waveforms from the double pulse test



(a) (b)

Fig. 17. ZOOM : Measured Drain-source voltage of the low-side power GaN at turn-off (a) and turn-on (b)

V. Conclusion

Monolithic integration of the GaN gate driver suppresses parasitic inductances in the gate and power loops, unlocking the full performance of GaN transistors. This work compares four gate driver circuits based on GaN area, static power, and propagation delay, identifying trade-offs and highlighting Circuit C as the most balanced bootstrap-based solution requiring only one external supply. Circuit C was integrated into a GaN IC, and experimental measurements validated simulation results. The gate driver drew 6.8 mA static current, consistent with expectations. When connected to the low-side of an integrated GaN Half-bridge, clean switching was observed with minimal overshoot, low ringing, and sub-20 ns rise/fall times at 100 V, 1 A. Future work will target high-side capability validation and improved drive strength for higher-current GaN stages.

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