Back Barrier Integration for > 4kV Blocking in GaN HEMTs on Sapphire without Field Plates

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ABSTRACT - This work presents a significant advancement in optimizing the trade-off between on-resistance and breakdown voltage in GaN high electron mobility transistors (HEMTs) grown on sapphire substrates. By integrating an AlGaN back barrier and employing high carbon doping in the buffer layer, we achieve blocking voltages exceeding 4 kV while maintaining low on-resistance—without the use of gate dielectrics or field plates. In addition to improved electrical performance, transient measurements reveal a reduction in trapping effects thanks to the back barrier, which enhances carrier confinement and mitigates long recovery time traps. These findings highlight the potential of GaN-on-sapphire as a cost-effective and scalable platform for high-voltage power applications.

Key-words — Power HEMT, Back barrier, GaN on sapphire, high voltage

1. INTRODUCTION

Cost-effective GaN-on-Silicon HEMTs have emerged as a promising technology for low- to medium-voltage applications (up to 1200 V), particularly with the advent of vertical configurations that offer avalanche breakdown capability [1], [2]. However, GaN-on-Silicon faces limitations for higher voltage applications (typically beyond 1200 V) due to challenges in growing thick epilayers exceeding 10 µm, which are necessary for such operations.

GaN HEMTs grown on sapphire substrates have gained attention as an alternative platform for high-voltage applications due to the excellent insulating properties and thermal stability of sapphire, enabling vertical scalability and reduced substrate leakage [3].

Specifically, the combination of a highly carbon-doped buffer and an AlGaN back barrier provides enhanced electric field management and 2DEG confinement, resulting in blocking voltages exceeding 4 kV without the use of gate dielectrics or field plates. Furthermore, transient characterization highlights the role of the AlGaN back barrier in mitigating trapping effects commonly observed in GaN-based devices. Drain current transient (DCT) measurements reveal a reduction in slow-recovering traps, particularly in structures incorporating the back barrier, which effectively shields the active region from buffer-induced trapping.

2. DEVICE DESIGN

In our study, we used four different epitaxial structures (depicted in Figure 1). All were grown by MOCVD on 4 inches diameter sapphire. Two of these structures featured a 500 nm carbon-doped GaN buffer with a doping concentration of 1×10^{19} cm^{-3} while the other two utilized a bilayer buffer comprising a lower layer of iron-doped GaN (doped at 1×10^{18} cm^{-3}) and an upper layer of carbon doped (6×10^{18} cm^{-3}). Each pair of epitaxial structures included one configuration with a 350 nm unintentionally doped GaN channel without back barrier and another with a 150 nm unintentionally doped GaN channel incorporating a 100 nm AlGaN back barrier containing 6% of aluminum.

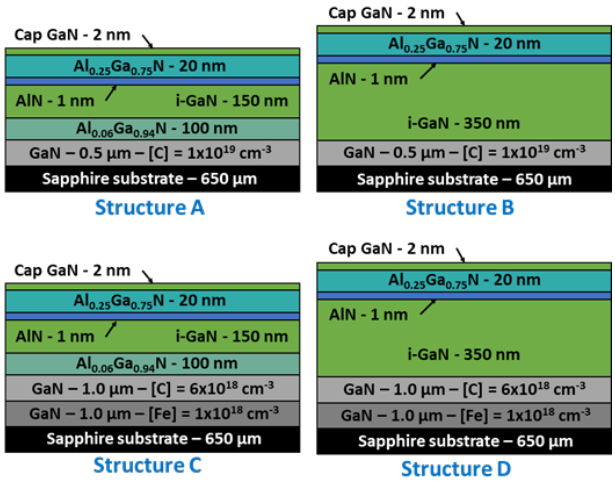

FIG. 1. Schematics cross section of the fabricated heterostructures

All the wafers were diced into quarters and only one quarter of each was processed. HEMTs with gate-to-drain distances (GD) ranging from 2 to 40 µm were fabricated on all structures.Device isolation was achieved through mesa etching to define the active regions, and no passivation layers, gate dielectrics, or field plates were used to simplify processing and isolate intrinsic material effects. Hall effect measurements showed that the AlGaN-containing structures exhibited comparable 2DEG properties, with a carrier concentration of 1×10^{13} cm^{-2}, an electron mobility of 1900 cm^2/V.s and a sheet resistance of 340 Ohm/sq. These baseline transport properties confirm uniform 2DEG formation across samples and provide a consistent reference for interpreting breakdown voltage and trapping variations linked to buffer and barrier design.

3. RESULTS AND DISCUSSION

All breakdown measurements were done using a Keysight B1505A Power Device Analyzer with a B1513C High Voltage Source Monitor Unit for measurement up to 3 kV, enhanced by a N1268A Ultra High Voltage Expander for the measurement up to 10 kV.

3.1. Buffer breakdown measurements

To evaluate the breakdown performance of the buffer, isolated ohmic contacts were fabricated with spacings ranging from 5 µm to 96 µm. A mesa depth of 500 nm was used for the electrical isolation between the contacts.

Figure 2 presents the average breakdown voltage values for each buffer configuration. Interestingly, the high-carbon-doped buffer exhibited significantly improved voltage handling capability, even with reduced thickness. This suggests that the carbon doping level has a more dominant effect on breakdown strength than buffer thickness, likely due to enhanced compensation of

deep traps and suppression of leakage paths.

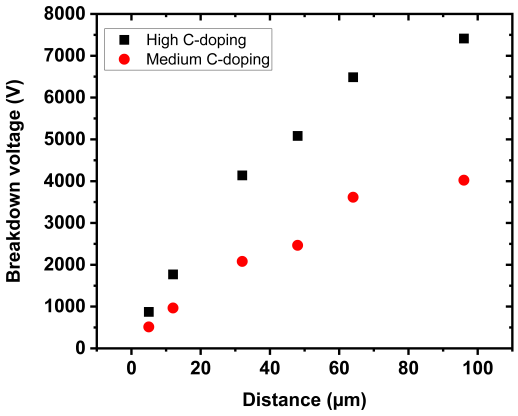

FIG. 2. Typical buffer breakdown voltages for each contact distance

3.2. *HEMT breakdown and on-state characteristics*

The blocking voltage of the fabricated transistors—across gate-to-drain (GD) distances from 10 to 40 µm-was measured using the same high-voltage setup. The gate voltage was fixed 4 V below the threshold voltage to ensure robust pinch-off during breakdown characterization.

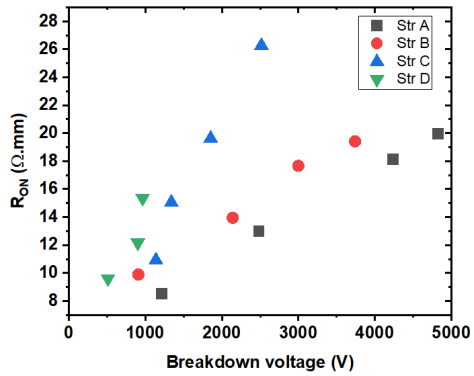

FIG. 3. Typical R_{ON} values as a function of the breakdown voltage for all GD

Figure 3 shows the ON-resistance (R_{ON}) values as a function of breakdown voltage, while Figure 4 presents the breakdown behavior for transistors with GD = 40 µm.

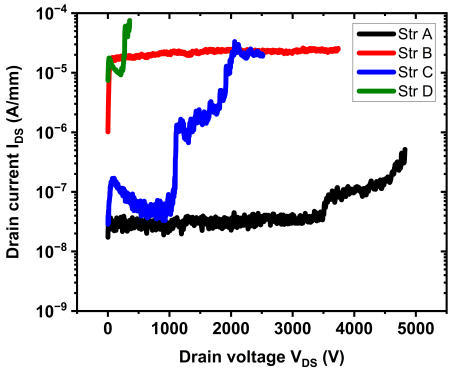

FIG. 4. Breakdown voltage measurements for HEMTS with GD=40µm

As expected from the buffer breakdown analysis, devices with highly carbon-doped buffers consistently show higher breakdown voltages. Lower carbon doping results in elevated off-state leakage currents and premature breakdown, consistent with reduced charge compensation in the buffer.

The inclusion of the AlGaN back barrier further enhances breakdown voltage while suppressing leakage, attributable to its role in improving 2DEG confinement and distributing the electric field more evenly under high bias, as previously observed in RF devices [4]. This enhanced confinement plays a pivotal role in achieving higher blocking voltages. It is important to note that a low R_{ON} is observed for all structures owing to the favorable 2DEG properties (see Figure 3).

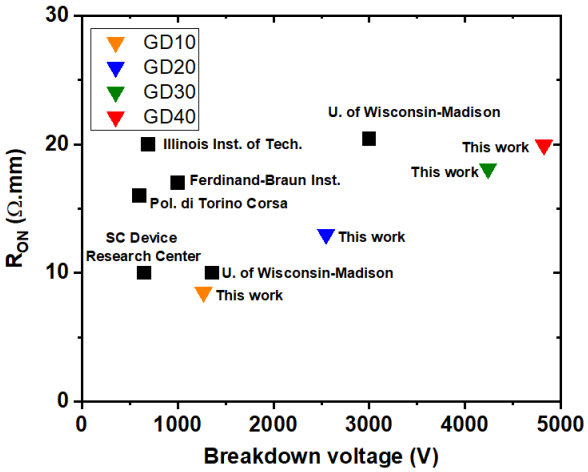

FIG. 5. Benchmark R_{ON} vs breakdown voltage for HEMT on sapphire

As shown in Figure 5, our HEMT devices on sapphire substrate exhibit R_{ON} and breakdown voltage performance favorably comparable to state-of-the-art benchmarks, showcasing their potential in high-voltage applications.

3.3. *Drain current transient (DCT) measurement*

Drain Current Transient (DCT) were conducted to identify traps inherent in the devices. In this measurement, a double pulse voltage sequence is applied to the transistor, consisting of a trapping phase (filling phase) and a detrapping phase (recovery phase). In the filling phase, the bias is set to induce trapping mechanisms. This typically involves configuring the gate and the drain bias ($V_{GS,Fill}$, $V_{DS,Fill}$) to create conditions favorable for charge trapping.

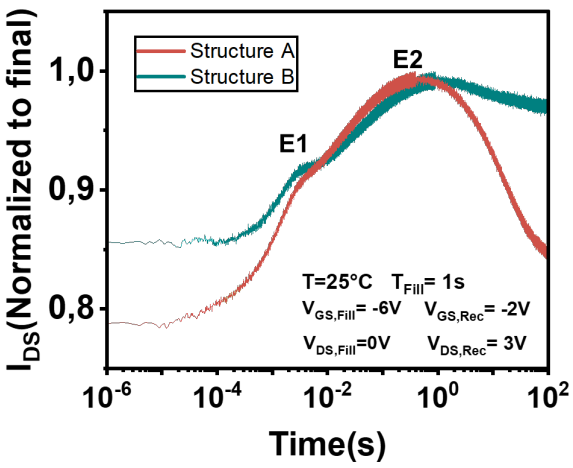

FIG. 6. DCT measurement for drain filling bias of 0 V

Subsequently, the bias is switched to ($V_{GS,Rec}$, $V_{DS,Rec}$) to favor charge detrapping processes. This transition marks the beginning of the recovery phase. During this phase, the transient of the drain current is recorded immediately following the bias switch until returning to its steady-state value. Figure 6 and 7 presents the drain current transients following a 1s filling phase under drain lag conditions at $V_{GS,Fill}$ = -6 V and and where the drain filling bias is 0 V for Figure 6 and 30 V for Figure 7, at room temperature.

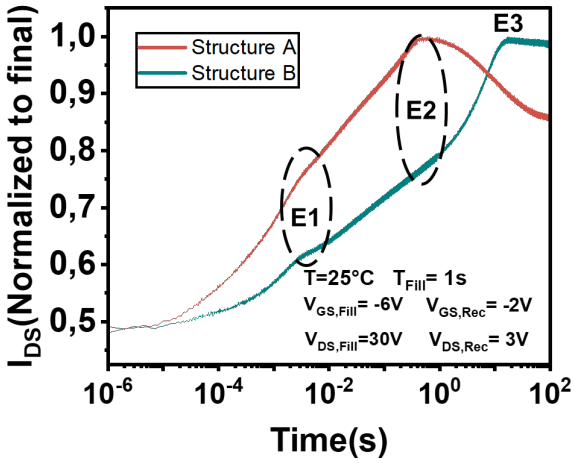

FIG. 7. DCT measurement for drain filling bias of 30 V

We can observed a trap with a long recovery time (1 to 10 s) detected on structure B but not on structure A although the buffer is closer to the biased contacts, thanks to the presence of the back barrier.

3.4. TCAD simulations

To explore design optimizations, TCAD simulations were carried out using Silvaco on a calibrated structure based on Structure A (Figure 8). These simulations investigated the impact of varying aluminum content in the back barrier from 6% to 20%.

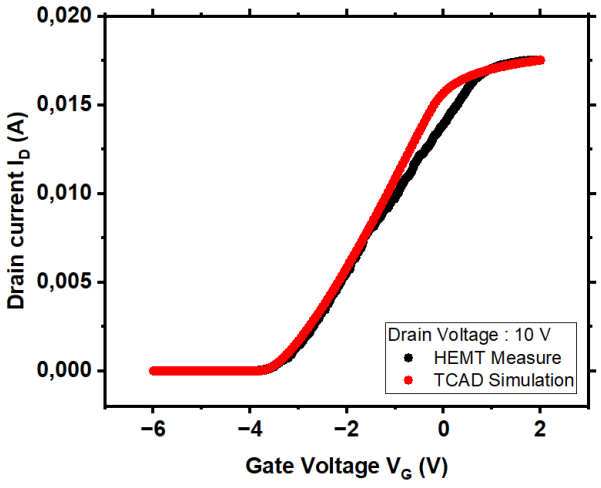

FIG. 8. Transfert curve comparison for a HEMT and the equivalent simulated structure

Simulations were based on a 40 µm gate-to-drain device, with incremental aluminum content to study its effect on electric field distribution and breakdown voltage. Breakdown voltage increased with Al content up to 15%, beyond which no significant improvement was observed—suggesting saturation of polarization effects.

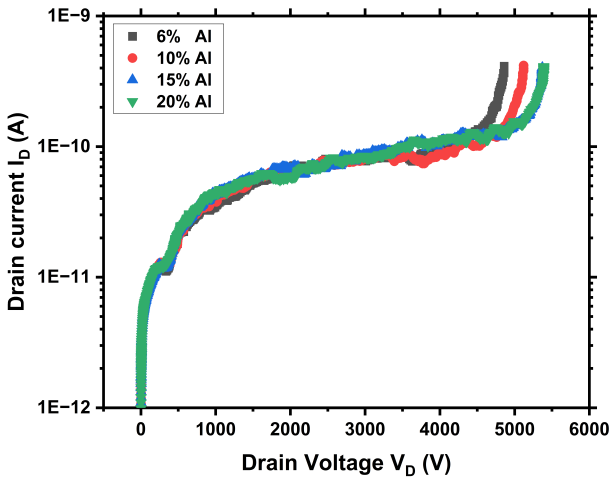

FIG. 9. Breakdown voltages curves obtained for various Al content in the back barrier

Additionally, replacing the sapphire substrate with AlN was simulated, given its higher dielectric strength despite its narrower bandgap. We conducted simulations using a 6% Al composition in the back barrier to evaluate its impact on breakdown. Despite AlN's smaller bandgap (6.2 eV vs. sapphire's 10 eV), its higher dielectric strength (12–15 MV/cm compared to 0.5 MV/cm for Al_2O_3) resulted in a higher breakdown voltage. However, this also led to increased leakage currents, as shown in Figure 10.

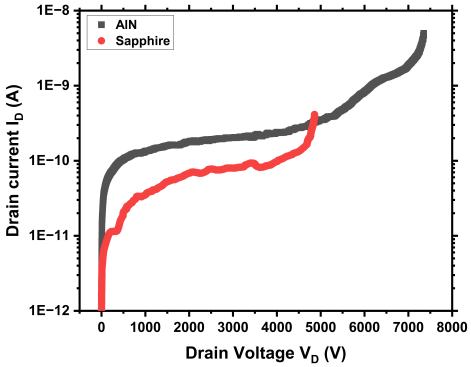

FIG. 10. Breakdown voltage curves for a simulated structure on sapphire and on AlN

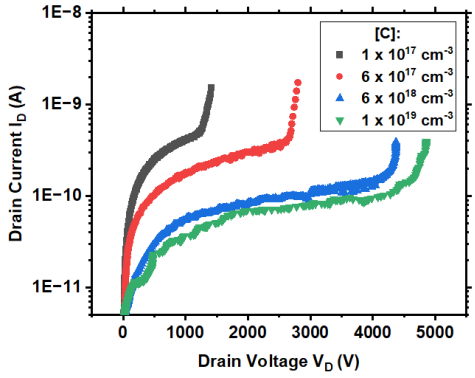

FIG. 11. Breakdown voltage curves for various carbon concentration in the buffer

Finally, simulations were performed with varying carbon concentrations in the buffer. Figure 11 shows that increasing the carbon concentration results in higher breakdown voltages and lower leakage currents. These findings are consistent with previous studies on HEMTs without a back barrier [5].

To further analyze the buffer's influence on the electric field distribution, breakdown simulations were extracted at 1000 V for structures with buffer carbon concentrations of 1×10^{17} cm^{-3} and 1×10^{19} cm^{-3}. The corresponding electric fields at this bias are illustrated in Figures 12 and 13, with close-up views below the gate - where the electric field peaks.

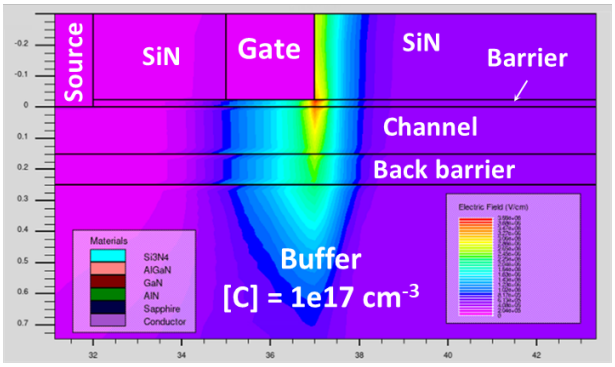

FIG. 12. Maximum electric field observed ont the structure with a low carbon doped buffer

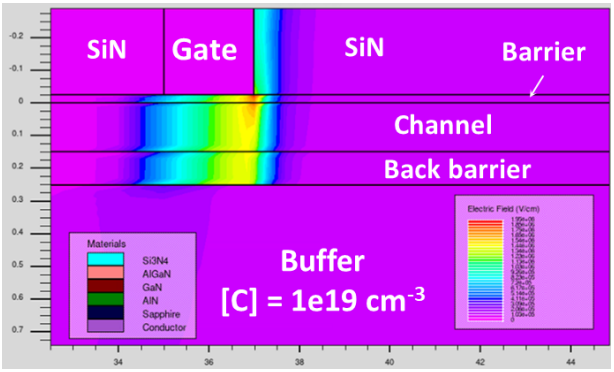

FIG. 13. Maximum electric field observed ont the structure with a high carbon doped buffer

The structure with a lower carbon concentration exhibits a higher electric field, reaching maxima of 3.9 MV/cm in the AlGaN barrier and 3.2 MV/cm in the GaN channel. In contrast, the second structure (higher carbon concentration) shows significantly lower peak fields of 1.95 MV/cm and 1.8 MV/cm, respectively. Additionally, the electric field remains very low in the buffer when its carbon concentration is high. This suppression of the electric field, particularly below the gate and within the buffer, likely contributes to the higher breakdown voltage and reduced leakage currents observed in Figure 11.

4. CONCLUSIONS

This work demonstrates the successful optimization of GaN HEMTs on sapphire substrates, achieving an exceptional balance between on-resistance and breakdown voltage through strategic design choices. The integration of a highly carbon-doped buffer layer (1×10^{19} cm^{-3}) proved critical, enabling breakdown voltages exceeding 4 kV while minimizing leakage currents. Simulations and experimental measurements revealed that the carbon-doped buffer effectively suppresses electric field penetration, reducing peak fields from 3.9 MV/cm to 1.95 MV/cm in the active regions, thereby enhancing device robustness.

The addition of an AlGaN back barrier (6% Al) further improved performance by confining the 2DEG under high electric fields, leading to higher breakdown voltages and reduced leakage. Simulation studies indicated that increasing the aluminum content in the back barrier up to 15% provides incremental gains, with diminishing returns beyond this point. Exploratory simulations replacing sapphire with AlN substrates highlighted the potential for even higher breakdown voltages due to AlN's superior dielectric strength, though this came at the expense of increased leakage currents.

Drain current transient measurements provided insights into charge trapping dynamics, revealing that structures with a back barrier exhibited fewer long-recovery traps, further validating its role in device stability. The fabricated HEMTs achieved state-of-the-art performance metrics, positioning GaN-on-sapphire as a viable and cost-effective solution for high-voltage applications without relying on gate dielectrics or field plates.

Looking ahead, future research should focus on optimizing AlN-based designs to mitigate leakage, as well as investigating dynamic performance under switching conditions. These advancements could unlock new opportunities for GaN HEMTs in demanding applications such as power grids and electric vehicles. The results presented here underscore the potential of GaN-on-sapphire technology as a competitive platform for next-generation power electronics.

5. REMERCIEMENTS

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