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# Permanent degradation of p-GaN HEMTs due to repetitive overvoltage stress during hard turn-off switching

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## Abstract

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) are promising candidates for power electronics but suffer from reliability concerns due to, for instance, their lack of avalanche capability. This study investigates the long-term impact of dynamic overvoltage stress on GaN HEMTs using a newly designed test circuit, UIS3, which isolates key stress factors. Devices were subjected to short-duration repetitive overvoltage stress near their dynamic breakdown voltage. Characterization before and after stress reveals permanent degradation in  $C_{DS}$  and  $I_{DSS}$ , suggesting structural damage within the device. A distinct alteration in the  $C_{DS}$  curve is observed, possibly linked to local breakdown in the insulating layer. Higher stress levels accelerate failure. Our results provide new insights into GaN HEMT degradation mechanisms under high-voltage stress.

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## 1. Introduction

GaN HEMTs are gaining popularity in power applications due to their superior performance compared to silicon-based technologies [1]. However, the lack of accurate aging models hinders their broader adoption in the industry. As a result, the reliability of GaN HEMTs remains a major research topic.

Unlike silicon (Si) and silicon carbide (SiC) components, GaN HEMTs lack avalanche capability [2], raising concerns about their robustness against voltage spikes that can occur in real-world applications. These transient overvoltages, often unavoidable due to parasitic inductances in circuits, could potentially affect the long-term reliability of GaN devices. Although prior research has explored this issue [2-4], further investigation is needed to better understand the underlying mechanisms and improve degradation prediction models.

A commonly used approach to study overvoltage stress is the Unclamped Inductive Switching (UIS) test [2-4]. However, this method does not allow for a clear distinction between the different stress effects experienced by the device in its OFF-state. This is particularly relevant for GaN HEMTs, which are highly sensitive to reverse-bias voltage stress in this condition [5]. As a result, existing studies do not fully isolate the specific impact of dynamic overvoltages on overall device degradation. Literature also highlights the strong need to study dynamic breakdown. In fact, the shorter the overvoltage duration, the higher the voltage the device can withstand [3].

Moreover, our objective is also to isolate the impact of temperature. The literature already discusses the potential thermal degradation associated with an

increase in  $R_{ON}$  over the test duration [6]. When applying repetitive stress, the DUT's temperature may increase due to the time it spends in conduction mode while charging the inductor of the UIS.

In this article, a new test circuit that combines the principles of UIS and DST (Double Source Test) [7] is proposed to better distinguish the different stress factors and minimize conduction time of DUT. Its operating principle, DUT and the test setup will be outlined in section 2. Results from its use will be presented in section 3. In section 4, an explanation of the phenomena affecting the device based on the observed results is proposed.

## 2. Device Under Test and test setup

### 2.1. DUT : GaN Systems 650 V - 30 A device

The device tested in this article is a commercial p-GaN HEMT with Schottky gate contact rated for a drain-source voltage of up to 650 V and a maximum drain-source current of 30 A. Field plates are used to enhance its ability to withstand high drain-source voltages [8].

To ensure accurate measurements, a Golden Device (GD) is used, which is not subjected to stress but undergoes characterization before and after the stress tests. This allows us to identify any potential drift caused by the characterization system itself.

### 2.2. Unclamped Inductive Switching, Supply Switched : UIS3

The developed stress circuit, presented in Fig. 1, uses a half-bridge of transistors  $M_1$  and  $M_2$  to couple

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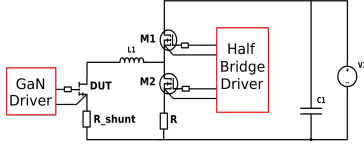


FIG. 1. UIS3 circuit schematic

TABLE 1. phases of a UIS3 cycle.

Phase	DUT	Half-bridge	Description
1	OFF	Low ON	DUT is at rest with $V_{DS}$ at zero, allowing the temperature to decrease.
2	ON	Low ON	DUT switches to ON state with $V_{DS}$ at zero. Therefore, no losses are generated during switching.
3	ON	High ON	Current flows, and inductor $L_1$ is charged. The slope of the current ramp is adjustable with $V_1 \cdot \frac{di}{dt} \approx \frac{V_1}{L_1}$ .
4	OFF	High ON	DUT switches to OFF state, and the energy stored in inductor $L_1$ is dissipated in the $C_{oss}$ capacitance of the DUT.
5	OFF	Low ON	After the overvoltage, the half-bridge switches, and the resulting RLC circuit dissipates the stored energy with $R$ adjusted for critical damping.

the DUT to a voltage source and charge inductance  $L_1$ , or decouple it to dissipate the energy. This circuit is referred to as UIS3. Table 1 describes a complete UIS3 cycle, which is repeatable to create periodic stress.

The inductance  $L_1$  is created using an LMR400 transmission line, providing a low and adjustable inductance (approximately 20 nH for 10 cm), ideal for high-frequency operation and low inductance values. This setup is designed to operate up to 1 MHz while minimizing noise.

### 2.3. Characterization setup

The characterization system used is a B1505A.

DUT and the GD are both characterized before and after the stress tests.

The characterization procedure on the B1505A follows this sequence :

- $V_{th}$
- Output characteristics
- $R_{ON}$  (same conditions as datasheet state)
- $V_{th}$  with preconditioning [9]
- $I_D$  vs.  $V_{DS}$  ( $V_{DS}$  up to 650 V)
- $C_{GD}$  vs.  $V_{DS}$  ( $V_{DS}$  up to 500 V)
- $C_{DS}$  vs.  $V_{DS}$  ( $V_{DS}$  up to 500 V)

One week after the stress tests, the same characterization procedure is repeated on the DUT to assess whether any observed drifts recover over time.

### 2.4. The applied stress

The stress cycle waveforms are outlined in Fig. 2. For each DUT, the stress cycle is repeated every 1

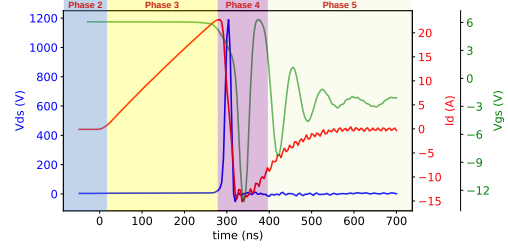


FIG. 2. An UIS3 cycle with phases described in Table 1, extracted from G1 during its stress protocol.

TABLE 2. List of DUTs and the corresponding stress conditions.

DUT ID	$V_{DS-peak}$	$I_{D-turnoff}$	million of cycles
G1	1200 V	22 A	0.9 (15 minutes)
G2	1280 V	22 A	0.9 (15 minutes)
G3	1280 V	22 A	3.6 (1 hour)
G4	1200 V	22 A	3.6 (1 hour)
GD1	Golden Device		

ms (1 kHz) for a specified duration. This frequency has been chosen to ensure that the case temperature,  $T_{CASE}$ , increases by no more than  $2^\circ\text{C}$  after 1 hour under the harshest stress conditions.

An overvoltage,  $V_{DS-peak}$ , is applied at a fixed peak current,  $I_{DS-toff}$ . Through preliminary testing on other DUTs of the same type, the dynamic breakdown drain-source voltage has been experimentally determined to be approximately 1.43 kV. At this voltage, a single event is sufficient to destroy the device, as it instantly reaches a dielectric breakdown. This finding is consistent with what is reported in the literature for this type of device [3]. Based on this, DUTs are tested near the breakdown voltage using repetitive overvoltages. Specifically, 1.2 kV (83% of  $BV_{dyn}$ ) and 1.28 kV (90% of  $BV_{dyn}$ ) were selected.

The stress conditions applied to each DUT are detailed in Table 2. To achieve the desired  $V_{DS-peak}$ , the inductance  $L_1$  and the bus voltage  $V_1$  were adjusted to maintain the same  $\frac{di}{dt}$  across  $L_1$ . For the 1.2 kV condition,  $L_1$  was set to 450 nH and  $V_1$  to 43 V. For the 1.28 kV condition,  $L_1$  was set to 520 nH and  $V_1$  to 49.7 V. The conduction time of the DUT is consistent with 250 ns. Since  $\frac{di}{dt}$  was kept constant, the ramp is the same for both cases. Therefore, the conduction losses in the DUT are identical for each test case.

## 3. Results

### 3.1. Experimental generation of a failure curve

The Fig. 3 shows the maximum number of cycles before failure for different  $V_{DS-peak}$  values. The failure observed is the inability to control the DUT, as the device remains in a continuously conducting state.

It was observed that more stress cycles can be en-

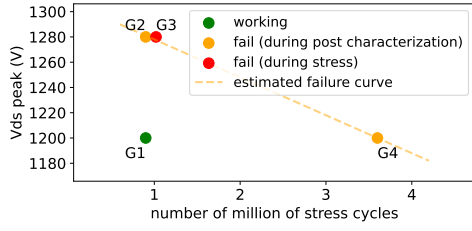


FIG. 3. The scatter plot shows the failure states of each DUT under 1 kHz stress. An estimated failure curve is included, though additional testing is required to validate and refine it.

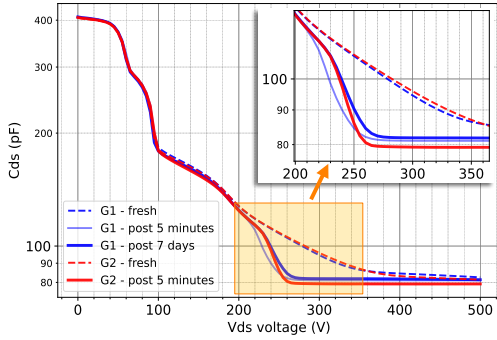


FIG. 4. Drift of  $C_{DS}$  against  $V_{DS}$  for DUT G1 and G2 before and after stress.  $V_{GS}$  is fixed at 0 V.

duced by a device when the  $V_{DS-peak}$  is lower. This is a preliminary result, which could contribute to developing an acceleration law for the aging of these devices under different overvoltage stresses during hard-switching turn-off. Further data points on this curve are needed to validate this potential aging trend.

### 3.2. Observed permanent degradations

Drifts have been observed in the characterized parameters of stressed DUTs. In this section, focus is made on devices G1 and G2, which can still be characterized after stress, in contrast to G3 and G4 that were not functional anymore. The latter failed due to high off-state drain-source leakage and gate-source leakage, which prevented the application of certain polarizations required for measuring  $C_{DS}$ . G2 failed during the post-7-day characterization. Indeed, the characterization process itself can be harmful to a device that has already been weakened by the stress test.

$R_{DS-on}$  and  $V_{TH}$  exhibit recoverable behavior, which has been well studied in the literature [10]. Therefore, these behavior are not studied here.

GD, did not show any drift, so its characterization is not reported here, for better readability of the figures.

Fig. 4 shows the  $C_{DS}$  versus  $V_{DS}$  curves for G1 and G2. The plots present their characterization before stress, 5 minutes after stress, and 7 days after stress (the latter only for G1). A pocket shape appears after the stress for a  $V_{DS}$  between 200 V and 400 V.

From the characterization of G1, this drift is

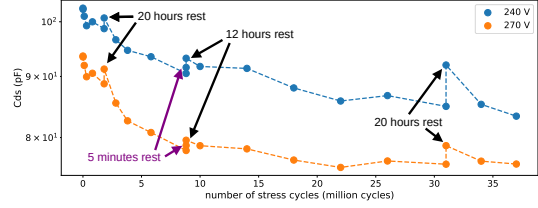


FIG. 5.  $C_{DS}$  drift against cumulative number of stress cycles for G5. Characterization are made 3 minutes after the last stress cycle.

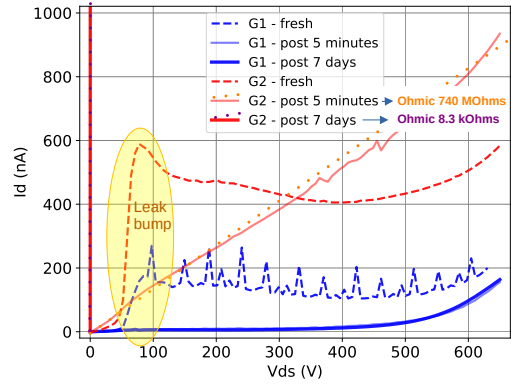


FIG. 6. Drain leakage current  $I_D$  against voltage  $V_{DS}$  drift for DUT G1 and G2 before and after stress.  $V_{GS}$  is fixed at 0 V.

nearly permanent, with almost no recovery after 7 days of rest.

The drift is more pronounced for the G2 device, which was subjected to a more stressful condition ( $V_{DS-peak}$  of 1.28 kV) compared to G1 ( $V_{DS-peak}$  of 1.2 kV). This suggests that device G2 experienced more permanent degradation than device G1, which is further confirmed by the fact that G2 failed during the post-7-day characterization. Moreover, device G3, which was under the same conditions as G2, failed after 17 minutes of stress during the test.

Another DUT G5 has been tested under the same conditions as G1, but with characterization performed after several set of repeated stress cycles. This allows us to confirm the cumulative nature of this degradation. The Fig. 5 shows the drift of  $C_{DS}$  against the cumulative number of stress cycles for G5 measured at  $V_{DS}$  equal 240 V and 270 V. A partial recovery is also observed after a period of rest, during which all pads of the DUT remain in a high-impedance state, preventing any current from flowing through the device. However, the drift reappears more rapidly with subsequent stress cycles, indicating that the recovery is clearly incomplete.

The Fig. 6 presents the  $I_{DSS}$  vs.  $V_{DS}$  characteristics, showing measurements taken before stress, 5 minutes after stress, and 7 days after stress.

A reduction in leakage current is observed at 50 V, where the initial bump disappears after stress. However, this bump is not present in the GD characterization (not shown). Its origin in the G1 and G2 measurements before stress remains unexplained.

G2 exhibits a significant change in its drain current leakage characteristics, transitioning to an ohmic

leakage behavior as the  $I_D$  vs.  $V_{DS}$  curve becomes linear after stress. In contrast, G1 did not undergo sufficient stress to induce this phenomenon.

G1 is the only device that did experience a series of peaks in the  $I_D$  vs.  $V_{DS}$  curve. Origin of these peaks for G1 are not explained, but as this is the only device to exhibit this behavior, it is likely an issue with the characterization system rather than a device-specific phenomenon.

#### 4. Discussion

The observed drift in  $C_{DS}$  at specific voltages indicates potential structural degradation in the HEMT, particularly within the capacitance structure of the device.

We hypothesize that repeated short-duration overvoltage stresses gradually damage the insulating layer above the 2DEG channel exposed to high electric fields. Overvoltages may create sudden conductive paths by locally shorting capacitances, which explains the observed decrease in  $C_{DS}$ . As a result, the insulating material becomes conductive at specific points, leading to an increase in  $I_{DSS}$  leakage current, as observed in G2. Over time, these conductive paths expand, eventually causing  $I_{DSS}/V_{DS}$  to become linear. This transition to a fully ohmic leakage path is a clear indicator of device failure.

In contrast, G1 did not experience an increase in leakage current, suggesting that the degradation rate depends on the applied overvoltage level. For the same stress duration, higher voltages accelerate the failure process, reducing the device's ability to withstand stress over time.

These degradations appear to be permanent and distinct from recoverable trapping effects, such as those responsible for variations in  $R_{DS-on}$  [10]. However, further simulations and failure analysis are needed to confirm these hypotheses and better understand the underlying mechanisms.

#### 5. Conclusion

This study investigated the impact of repetitive short-duration overvoltage stress on GaN HEMTs using the innovative UIS3 circuit, which improves OFF-state stress decoupling and minimizes thermal influence, allowing clearer isolation of overvoltage-induced effects.

Results indicate permanent degradation in the  $C_{DS}$  characteristic and increased drain leakage for G2. The degradation scales with overvoltage amplitude, pointing to accelerated failure mechanisms. The lack of recovery over time supports the hypothesis of structural, not transient, degradation.

These findings emphasize the importance of addressing long-term reliability in GaN power devices. Further studies should include microscopic failure analysis, predictive aging models, and testing of additional devices to validate and refine observed trends under dynamic stress.

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