Comparative Analysis of 3-L Inverters Considering Conducted EMI Emissions Performances

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***Abstract*—This paper presents a comparative analysis of the performance of 3-Level inverter topologies for variable speed drives that address EMI conducted emissions requirements at both the input and output sides, as outlined by IEC 61800-3. First, a preliminary design optimization technique is used to derive the 3-Level inverters Pareto-front regarding price, loss, and volume, focusing on functional constraints such as signal quality, ripple, and voltage variation. Next, a review of the EMI equivalent circuit of 3-Level inverters is conducted and completed for 3-L SNPC. An automated design methodology for EMI filters is then defined and applied to derive the optimal design that complies with standards while balancing the previously defined trade-offs. Finally, the contribution of the EMI filter in terms of price and footprint is added to the inverter performances, providing complete insights into the overall system. The analysis is conducted at various power levels to emphasize the importance of addressing EMI requirements when selecting the suitable topology, as this can reverse performance trends.**

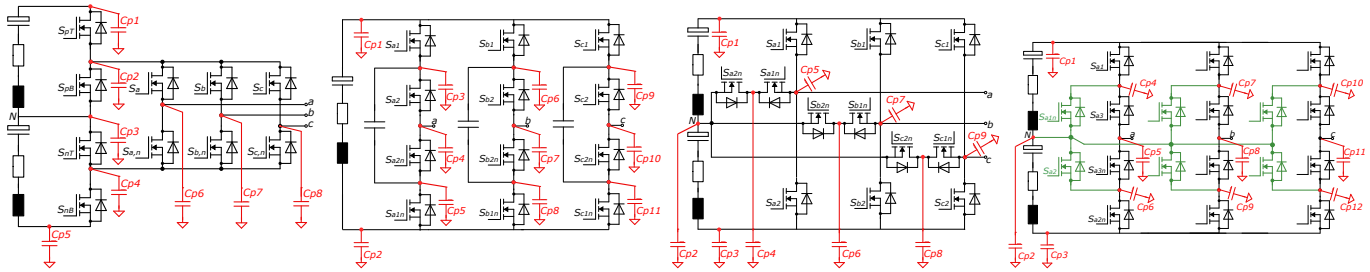
***Index Terms*—3-L inverter, EMI noise model, Optimization.**

I. Introduction

3-Level inverters based on wide-band-gap (WBG) semiconductors are becoming increasingly popular for next-generation variable speed drivers (VSDs) due to their high efficiency and compact design. 3-L topologies are characterized by three output voltage levels, which significantly reduce filtering requirements at the output compared to conventional 2-L voltage source inverters. Additionally, they experience lower semiconductor voltage stress, resulting in reduced switching losses [1]–[4]. Therefore, despite utilizing a higher number of switching devices, the benefits in passive components and enhanced performance make them a viable solution for VSDs application. Furthermore, the capabilities at high switching frequency of WBG semiconductors enables enhanced performances; thus, when paired with 3-L inverters, high-efficiency systems are achieved. However, the high dv/dt electrically stress the motor capacitors leading to high shaft voltage that cause bearing insulation breakdown that may results in electrical discharge machining and eventually reduce the motor mechanical life [5]. Additionally, the emissions on the grid side must be limited. Therefore, assessing EMI filter requirements on both the input and output sides is crucial during the early stages of the design process.

For each power inverter topology, a wide range of technological combinations can be explored to meet design specifications, resulting in various possible configurations that may lead to suboptimal solutions. Therefore, optimization techniques are essential to ensure optimal performance. Common optimization objectives include cost-efficiency, efficiency-power density, ripples-power density and efficiency-price-footprint [3], [4], [6]–[9]. The contribution of the EMI filter to these objectives must be carefully evaluated to assess overall system performance. Although simple indicators such as attenuation amplitude, cut-off frequency, and common-mode voltage provide preliminary insights, the most relevant approach is to fully design the filter and select technological components.

This work conducts a comparative analysis of performances of 3-L inverter topologies shown in Fig. 1 namely, 3-L Sparse Neutral Point Clamped inverter (SNPC), 3-L Flying Capacitor inverter (FlyCap), 3-L Ttype inverter and 3-L Active Neutral Point Clamped inverter (ANPC), considering optimal EMI



(a) (b) (c) (d)

Fig. 1: (a) 3-L SNPC, (b) 3-L Flycap , (c) 3-L Ttype, (d) 3-L ANPC

filters in both the input and output sides. These filters are designed in compliance with IEC61800-3 conducted emissions (CE) constraints. State-of-the-art EMI models used during the pre-design phase are typically valid within the frequency range of $150kHz$ to a few MHz. This range is critical for filter sizing and component selection. Beyond this interval, EMI performances are primarily improved through layout optimization, components placement and the reduction of PCB parasitics.

In this work, the contribution of EMI filters in terms of price, loss and volume is derived to give insight about the overall plug-and-play system performances and gives solid and fair basis to choose the suitable inverter topology. Section II presents conventional 3-L inverter optimization without EMI emissions limits constraint. Section III details EMI equivalent circuit of the different 3-L topologies. Section IV presents EMI filter design by optimization methodology and finally Section V presents the optimization result and EMI filter contribution to the overall system performances.

II. 3-L INVERTERS PARETO OF OPTIMAL DESIGN

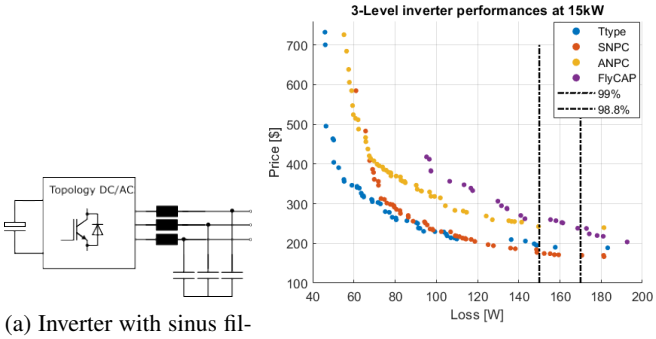
Power inverter design is a complex, multi-physical, and multi-dimensional problem. Decoupling certain phenomena and adopting an iterative approach helps balance trade-offs between modeling complexity, accuracy, and computational time within the design-by-optimization framework. Consequently, the design process focuses first on optimizing the inverter, selecting the appropriate topology, semiconductor devices etc., followed by the optimization of the EMI filter [10]–[12].

In this work,a highly precise multi-objective optimization of power inverter topologies with output sinus filter as shown in Fig 2 (a) is first conducted, focusing on functional constraints. The optimization relies on accurate modeling techniques, a comprehensive database of commercially available components, and avoids restrictive design rules, thereby preserving a high degree of design freedom. for the 3-L ANPC various PWM control strategies are considered, including PWM-1, PWM-2, and PWM-3 as introduced in [13], and PWM-4 as proposed in [14]. For the 3-L SNPC the space vector modulation (SVM) method described in [15] is employed, with various symmetrical control sequences such as strategies $'8'$, $'O'$, and $'U'$ defined as optimization variables. For 3-L FlyCAP and 3-L TType SVM and PWM are used.

Fig 2 (b) presents the optimization results at $15kW$, while the detailed methodology is described in [16].

- Topologies model : Based on semi-analytical approach that gives time-domain waveforms of current and voltage.
- Optimization constraint : Output signal quality $\Delta V_{out} < 4V$; DC bus variation $\Delta V_{DC} < 4\% V_{DC}$; semiconductors junction temperature $T_j < 120C$, and other constraints on component level to guarantee nominal lifetime.
- Component Library : +30 ref of SiC and GaN devices. +20 ref of magnetic material,+ 100 ref of Winding AwG, +20 ref core sizes, +40 ref of capacitors.

The optimization Pareto-front of 3-L topologies shown in Fig. 2 (b) accounts for various optimal solutions across



(a) Inverter with sinus filter

(b) Price-Loss Pareto Front

Fig. 2: 3-Level inverter functional optimization without EMI filter. $P_a = 15k$, $V_{dc} = 750V$, $v_{out} = 230V_{rms}$

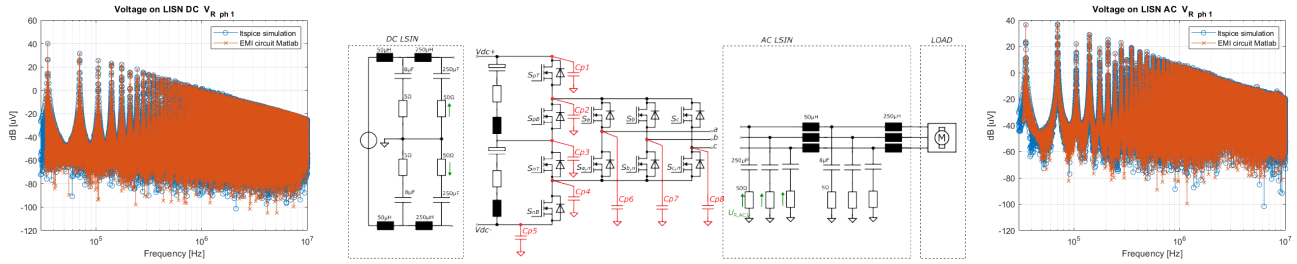
minimal price, loss and volume axis. The suitable design is determined by the project's highest priorities. In this work, we target minimal price for efficiencies between 98.87% and 99% ($150W - 170W$ losses for at $15kW$), Therefore, we focus on the 2D price-loss axes;. Table I summarizes key design variables, including the switching frequency f_{sw}, control strategy, inductor electrical value L_{DM}, filter capacitor value C_f and DC-bus capacitor value C_{dc}. The Pareto in Fig. 2 (b) must be completed by the contribution of the EMI filter to enable a comprehensive overall comparison.

TABLE I: Inverter Design Results

Parameter	**3-L SNPC**	***3-L TType***	***3-L ANPC***	***3-L FlyCap***
Design optimization results at $P = 15kW, V_{dc} = 750V, PF = 0.85$				
f_{sw}	$35kHz$	$40kHz$	$40kHz$	$45kHz$
Control	SVM seq '8'	SVM	SVM PWM-2	SVM
L_{DM}	$69\,\mu H$	$58\,\mu H$	$55\,\mu H$	$70\,\mu H$
C_f	$20\,\mu F$	$16\,\mu F$	$16\,\mu F$	$20\,\mu F$
C_{dc}	$28.2\,\mu F$	$4480\,\mu F$	$2800\,\mu F$	$10.5\,\mu F$
Design optimization results at $P = 75kW, V_{dc} = 750V, PF = 0.85$				
f_{sw}	$75kHz$	$55kHz$	$70kHz$	$40kHz$
Control	SVM seq'8'	SVM	SVM PWM-1	SVM
L_{DM}	$21\,\mu H$	$19\,\mu H$	$25\,\mu H$	$27\,\mu H$
C_f	$8\,\mu F$	$28\,\mu F$	$32\,\mu F$	$37\,\mu F$
C_{dc}	$56\,\mu F$	$1300\,\mu F$	$1100\,\mu F$	$44\,\mu F$

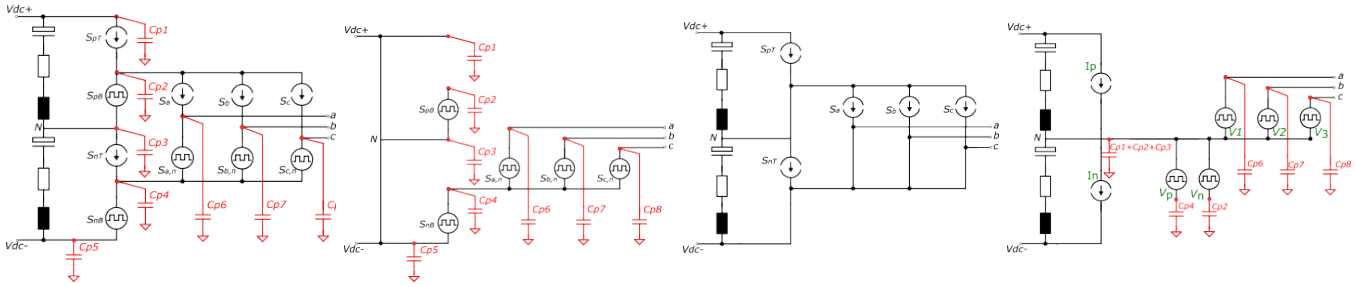
III. 3-L INVERTERS EMI EQUIVALENT CIRCUIT

EMI models for conducted emissions are derived to evaluate the performances of the different topologies. Among the various state of the art EMI modeling techniques, we chose frequency-domain analysis based on an EMI noise equivalent circuit, as it is more suitable for optimization studies [17]–[21]. The IEC 61800-3 standard for plug-and-play systems requires the evaluation of conducted emissions on both the DC input and AC output sides. For this evaluation, two Line Impedance Stabilization Networks (LISNs) are connected on the DC main side and on the load side, respectively, in order to guarantee reproducible measurements [19], [20], [22]. Fig 3 (b) illustrates the 3-L SNPC topology with the corresponding configuration. The LISN circuit complies with CISPR 16 (International Special Committee on Radio Interference).



(a) (b) (c)

Fig. 3: (a, c) LTspice validation in input and output side, (b) 3-L SNPC Inverter with DC input and AC output LISN



(a) (b) (c) (d)

Fig. 4: (a) EMI noise sources circuit , (b) voltage circuit , (c) current circuit, (d) unified circuit

A. 3-L SNPC proposed EMI circuit

The EMI model of the 3-L SNPC topology is derived using the noise equivalent circuit method under the assumption of a balanced system [23]. The noise sources are modeled as equivalent voltage and current generators that replicate the waveform discontinuities as illustrated in Fig. 4(a). By applying the superposition theorem, the voltage-source-based circuit shown in Fig. 4(b), is obtained by opening the current sources, while the current-source-based circuit in Fig. 4(c) is derived by short-circuiting the voltage sources. The current sources can be simplified into two components, I_p and I_n representing both the chopper and inverter-side current discontinuities. The total conducted emissions result from the combined effect of both models, which are integrated into a unified representation shown in Fig. 4(d). The current and voltage source are given in Equation 1. Where S_x is the switching sequences of the device x as illustrated in the Fig 3 (b).

$$
\begin{aligned}
&V_{1,2,3} = [(S_{pT} - S_{nT} + 1)S_{a,b,c} + (1 - S_{nB})]V_{DC}/2 \\
&V_{p\,,n} = (1 - S_x)V_{DC}/2 \quad x = pB, nB \\
&I_P = S_{pT}(S_a i_a + S_b i_b + S_c i_c) \\
&I_N = S_{nT}(S_{an} i_a + S_{bn} i_b + S_{cn} i_c)
\end{aligned}
\tag{1}
$$

The time-domain voltage and current waveforms used in equation 1 are obtained from a semi-numerical inverter model implemented in MATLAB. Subsequently, a Fast Fourier Transform (FFT) is applied to analyze the unified circuit in the frequency domain. The circuit is then evaluated using a custom-developed tool that computes the impedance from the circuit netlist and derives the voltage and current spectra at each node. This methodology is general and can be implemented using alternative tools as well. The EMI model was validated with LTspice time domain simulation, as shown in Fig. 3 (a) and Fig. 3 (d). The model was validated using trapezoidal voltage and current waveforms, which are appropriate within the validity range of the EMI model.

B. Classical 3-L toplogies

The EMI model of the 3-L FlyCAP inverter is derived following the same approach, the model is shown in Fig. 5 with the voltage and current waveforms given in equation 2.

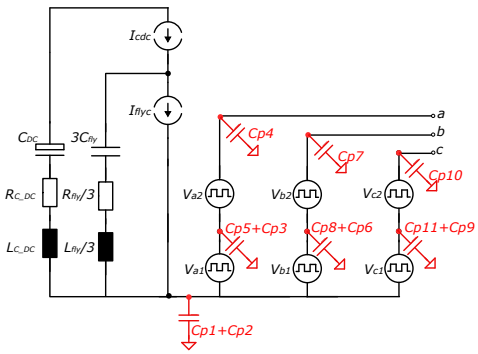


Fig. 5: 3-Level Flying capacitor EMI noise model

$$
\begin{aligned}
&V_{x1} = V_{x1}V_{DC}/2 \quad \text{where } x = a, b, c \\
&V_{x2} = S_{x2}V_{DC}/2 \\
&I_{cdc} = S_{a1}i_a + S_{b1}i_b + S_{c1}i_c \\
&I_{flyc} = (S_{a1} - S_{a2})i_a + (S_{b1} - S_{b2})i_b + (S_{c1} - S_{c2})i_c
\end{aligned}
\tag{2}
$$

3-L T-Type inverter: EMI noise model is presented in [24]
3-L ANPC inverter: EMI noise model is detailed in [25].
Due to space limitations, the models are not presented in this paper but can be easily derived using the same method.

IV. EMI FILTER DESIGN BY OPTIMIZATION

Various EMI filter optimization approaches are presented in the literature [11], [21], [26]. In this section a multi-objective optimization process is defined to derive the optimal EMI filter in terms of price, loss and volume similar to the one used in section II. A genetic algorithm is used to explore a discrete design variables representing technological references and filter topology; one stage LC filter and two stage $LCLC$ filter are considered as shown in Fig 6.

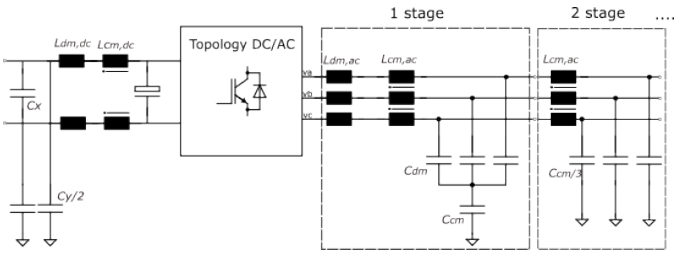


Fig. 6: Input and output EMI Filter

The design of the common mode choke (CMC) utilizes a library of high-permeability magnetic materials, including nanocrystalline materials, amorphous materials and ferrites. The CMC winding is implemented in a single-layer configuration to minimize inter-winding parasitic capacitance; The design targets a high coupling factor $k_{coupling} > 98.5\%$ to reduce fringing flux and mitigate leakage currents. The leakage inductance L_l is calculated using the model given in [27].

The C_x and C_y capacitors are standard off-the-shelf components. The values of the C_y capacitors are constrained by the requirement to limit ground leakage current, which must remain below the threshold of the protective circuit breaker, typically set at $30mA$; for inverters controlled with PWM with zero injection, it's the low frequency component that cause the main leakage; $C_{EMI\,ground} 2\pi f_{150hz} Vcm_{150hz} < 30mA$

A. Optimization inputs

The fixed parameters are the results of the functional optimization described in Section II, including the voltage and current sources of the EMI model, the DC-bus capacitor, and the sinusoidal filter parameters.

B. Optimization design variables

The design variables represent the topology configuration and technological choices for the DC-side and AC-side common-mode chokes (CMCs), including the magnetic material, core size, core stacking, wire gauge (AWG), wire material, number of winding turns, parallel windings, as well as the C_x and C_y capacitors. The reference components are stored in discrete databases along with their associated parameters, such as saturation characteristics, loss coefficients, volumetric density, and electrical properties.

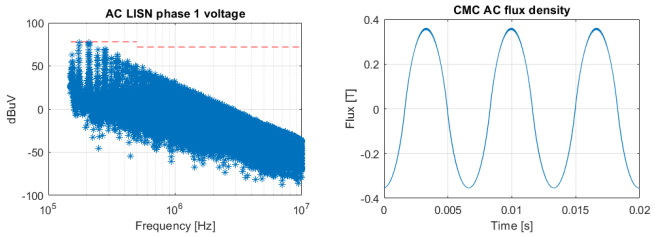
C. Optimization framework

1) The set of technological design variables selected by the algorithm is used to derive the electrical characteristics of the components.
2) The circuit of the topology with EMI filter is solved in frequency domain to compute the voltages and currents across the components, as well as to determine the voltages at the DC and AC LISNs phases.
3) Inverse FFT is performed to reconstruct the time-domain waveforms of current and voltage in CMCs and capacitors, which are subsequently used in the performance model, and in the constraints such the peak flux.

D. Optimization constraint

EMI constraints compare the LISNs voltage with IEC61800-3 limits as shown in Fig 7 (a):

$$V_{\mathrm{dB}\mu\mathrm{V}} = \begin{cases} 80dBuV, & \text{for } 150\,\mathrm{kHz} \le f < 500\,\mathrm{kHz} \\ 74dBuV, & \text{for } 500\,\mathrm{kHz} \le f \le 10\,\mathrm{MHz} \end{cases}$$



(a) LISN AC voltage (b) CMCs AC flux

Fig. 7: (a) From frequency model (b) obtained through iFFT

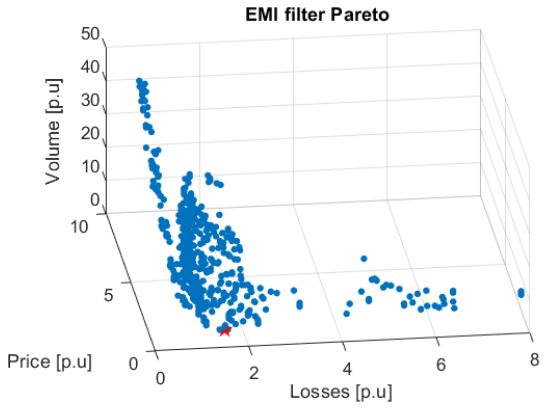
Other constraints are on component level; core saturation, capacitor voltage and allowable current, current density etc. The flux density inside the common mode choke is derived from the voltage time-domain waveform reconstructed via the inverse FFT of the frequency-domain data, the spectral analysis accounts for low frequency harmonics up to $10f_{sw}$; Thus; $B = \frac{1}{NS}\int vdt$ with N the winding turn numbers and S the core section as shown in Fig 7 (b). The design of CMCs is primarily driven by the presence of a low-frequency component in the flux density, which arises from the combined effect of the two-LISN configuration and the control strategy employing zero-sequence injection. Accordingly, The common-mode voltage component at $150Hz$ originating from the control, causes high ground current due to the low-impedance circuit formed by the two LISNs, which can be approximated as:

$$I_{g\,150hz} \approx \frac{|V_{cm\,150Hz}|}{Z_{RSIL,ac} + Z_{RSIL,dc} + Z_{CMC,ac} + Z_{CMC,dc}}$$

$$I_{g\,150hz} \approx \frac{|V_{cm\,150Hz}|}{2\pi \frac{C_{RSIL,ac\,24uH} C_{RSIL,dc\,16uH}}{C_{RSIL,ac\,24uH} + C_{RSIL,dc\,16uH}}}$$

E. Optimization results

Figure 8 shows the Pareto front of EMI filter optimal designs for the $15kW$ 3-L T-Type inverter specified in Table



(a)

Fig. 8: Optimization of 3-L TType inverter at $15kW$

I. The Pareto front represents set of feasible design with no single design being optimal in all aspects. For this analysis, the selected design balances cost and volume (red point), while ensuring losses remain below 10% of the total inverter loss.

V. Inverter performances with EMI filter

The performance contributions of the EMI filter, obtained through optimization, are integrated with the functional characteristics to derive the overall cost and footprint of the 3-L topologies, as illustrated in Fig. 9 and 10

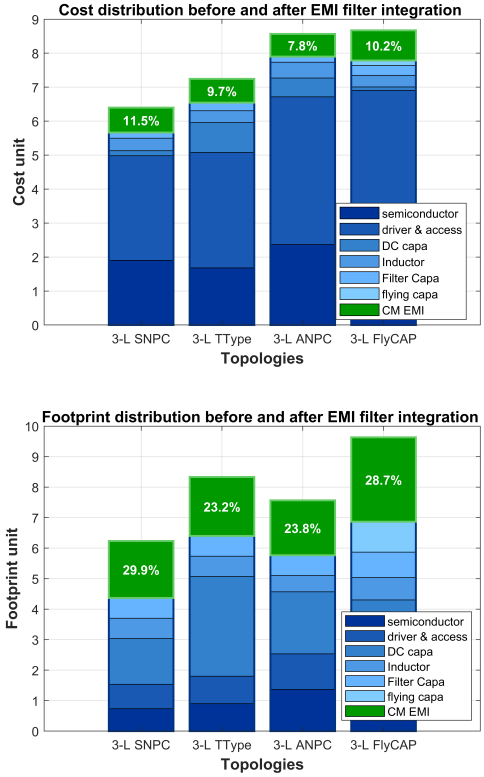


Fig. 9: 3-L topologies overall performances at $15kW$

At the $15kW$ power level, the performance trends before and after the addition of the EMI filter remain consistent, as illustrated in Fig.9. The percentage contribution of the EMI filter to both cost and footprint remains within a comparable range, despite variations in EMI emissions. In the 3-L FlyCAP, the second high-frequency harmonic falls within the regulated interval at $2(2f_{sw})$, due to the phase-shift control effectively doubling the output's apparent frequency. In contrast,for the 3-L ANPC, 3-L T-Type and 3-L SNPC it's the 4th and 5th high frequency harmonics at $180kHz$, $160khz$ and $175kHz$ respectively. The 3-L ANPC and 3-L T-Type topologies, when controlled using phase disposition, exhibit comparable performance. In contrast, the EMI emissions of the 3-L SNPC are influenced by its two-stage conversion structure and are highly dependent on the control sequence; for instance, with sequence '8', the emissions are higher.

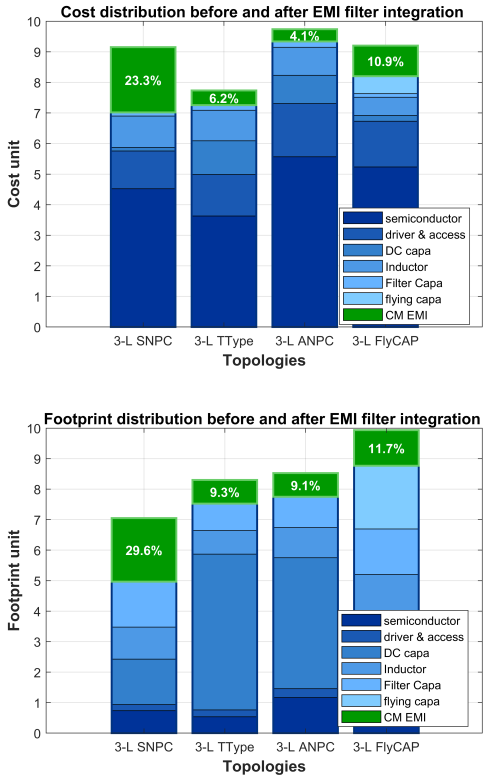


Fig. 10: 3-L topologies overall performances at $75kW$

At an operating power of $75kW$, the overall performance trends shift after adding the EMI filter contributions, as shown in Fig.10. The 3-L Ttype becomes the cost-optimal topology, replacing the 3-L SNPC, which requires larger EMI filters due to its $75kHz$ switching frequency placing the second harmonic within the regulated EMI band. A similar observation applies to the 3-L FlyCAP, whose second harmonic at $160kHz$ also falls within the critical range; however, its superior performance results in a slightly lower overall cost than the SNPC. In contrast, the 3-L T-type and 3-L ANPC require less attenuation, making them strong candidates when

EMI filter contributions are considered.

VI. Conclusion

This paper evaluated various 3-level inverter topologies under state-of-the-art functional constraints and performed an optimization-based analysis of the required EMI filters within a plug-and-play system. The results reveal that the EMI filter's contribution in terms of cost and footprint can be substantial and reverse the relative performance trends among topologies performances curves. This emphasizes the importance of addressing EMI constraints at the initial stages of the design process. Additionally, the EMI equivalent noise circuit for the 3-L SNPC inverter was proposed, and the EMI filter design for the 3-L FlyCAP topology was detailed. Furthermore, a multi-objective design-by-optimization approach was introduced to develop EMI filters optimized for both cost and volume constraints.. Future work will present a comprehensive design framework that integrates both functional and EMI constraints to support global inverter optimization.

It is important to emphasize that EMI filter sizing using a two-LISN configuration on both the DC input and AC output sides enables reproducible measurements within plug-and-play systems, but results in significantly larger requirements compared to a single-LISN setup. This is partly due to the high saturation component of the common-mode chokes (CMCs) and the lower impedance path provided by the two LISNs relative to the C_y impedance path.

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