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Impact of Multi-Bias on the Performance of 150 nm GaN HEMT for High-Frequency Applications

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Abstract

This study examines the performance of a GaN HEMT with a 150 nm gate length, fabricated on silicon carbide, across various operational modes, including direct current (DC), radio frequency (RF), and small-signal parameters. The evaluation of DC, RF, and small-signal performance under diverse bias conditions remains a relatively unexplored area of study for this specific technology. The DC characteristics revealed relatively little I_{ds} at zero gate and drain voltages, and the current grew as V_{gs} increased. Essential measurements include I_{dss} at 109 mA and I_{dssm} at 26 mA, while the peak g_m was 62 mS. Because transconductance is sensitive to variations in V_{gs} and V_{ds}, it shows "Vth $_{roll\text{-}off}$," where Vth decreases as V_{ds} increases. The transfer characteristics corroborated this trend, illustrating the impact of drain-induced barrier lowering (DIBL) on threshold voltage (Vth) values, which spanned from −5.06 V to −5.71 V across varying drain-source voltages (V_{ds}). The equivalent-circuit technique revealed substantial non-linear behaviors in capacitances such as C_{gs} and C_{gd} concerning V_{gs} and V_{ds}, while also identifying extrinsic factors including parasitic capacitances and resistances. Series resistances (R_{gs} and R_{gd}) decreased as V_{gs} increased, thereby enhancing device conductivity. As V_{gs} approached neutrality, particularly at elevated V_{ds} levels, the intrinsic transconductance (g_{mo}) and time constants (τ_{gm}, τ_{gs}, and τ_{gd}) exhibited enhanced performance. f_t and f_{max}, which are essential for high-frequency applications, rose with decreasing V_{gs} and increasing V_{ds}. When V_{gs} approached −3 V, the S_{21} and Y_{21} readings demonstrated improved signal transmission, with peak S_{21} values of approximately 11.2 dB. The stability factor (K), which increased with V_{ds}, highlighted the device's operational limits. The robust correlation between simulation and experimental data validated the equivalent-circuit model, which is essential for enhancing design and creating RF circuits. Further examination of bias conditions would enhance understanding of the device's performance.

Keywords: GaN HEMT; 150 nm gate length; multi-bias characterization; small-signal analysis; on-wafer measurements

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1. Introduction

The beneficial properties of GaN HEMTs have made them a focal point in the semiconductor industry. Due to their high breakdown voltage, high electron mobility, and high thermal conductivity, they are suitable for high-power and high-frequency applications [1–4]. Compared to conventional silicon and GaAs devices, GaN HEMTs that utilize silicon carbide (SiC) substrates offer even greater benefits. SiC's exceptional

thermal conductivity enhances the efficiency and power density of various systems, including radar systems and RF amplifiers, by effectively dissipating heat during high-power operation [5–10]. Despite numerous studies examining the DC and RF performance characteristics of GaN HEMTs [11–24], there is limited information available regarding their behavior under varying bias conditions, especially concerning small-signal and multi-bias performance [25–30]. To design and analyze GaN RF circuits, it is essential to investigate how multi-bias conditions influence crucial parameters, including transconductance (g_m), output resistance (R_{ds}), and intrinsic capacitances. Existing literature has primarily focused on basic DC characteristics under static bias conditions, with earlier work addressing only the influence of bias on switching ability and efficiency. Prior research has focused on the effects of passive and active parasitics, leaving the dynamic impact of bias on RF and small-signal parameters less studied. For example, some research has examined the effects of parasitic components on frequency response and stability [31–33], while other research has focused on bias-related noise performance [14,34,35]. However, there has not been a thorough examination of DC, RF, and small-signal characteristics under various bias conditions. The objective of this research is to investigate the behavior of a GaN HEMT 150 with a 150 nm gate length, built on a SiC substrate, and to highlight the impact of bias conditions on equivalent circuit components and high-frequency performance.

Key DC results that highlight the device's performance capabilities include I_{dss}, which was measured at 109 mA, and I_{dssm}, which was measured at 26 mA. The device's sensitivity to these biasing parameters is further illustrated by the transconductance (g_m), which attained 62 mS at $V_{gs} = -4.8$ and $V_{ds} = 10$ V. Due to short-channel effects, such as DIBL, the threshold voltage (Vth) decreased as V_{ds} increased, with values ranging from −5.06 V to −5.71 V. At higher V_{ds}, the dark current (I_{dso}) increased exponentially, indicating an increase in carrier generation. An equivalent circuit analysis shows how extrinsic elements, such as parasitic resistances and capacitances, affect performance. Biasing ranged from V_{gs} = −6.0 V to −3.0 V and from Vds = 3 V to 15 V, with a focus on frequencies between 45 MHz and 50 GHz. The extraction process for device parameters starts by identifying extrinsic components to determine intrinsic parameters. C_{gs} increased with both V_{ds} and V_{gs}, while C_{gd} decreased. Simultaneously, C_{ds} rose as V_{gs} neared pinch-off. Owing to non-quasi-static phenomena, the series resistances R_{gs} and R_{gd} exhibited charging delays, whereas R_{ds} increased with V_{ds}, necessitating a balance for optimal design. At $V_{ds} = 11$ V and $V_{gs} = -4.8$ V, the intrinsic transconductance g_{mo} reached a maximum of 71 mS. It escalates with V_{gs}. Transistor inertia at elevated frequencies is indicated by intrinsic g_{mo} and time constants (τ_{gm}, τ_{gs}, and τ_{gd}), with g_{mo} reaching its maximum at reduced V_{gs} as V_{ds} increased. Increased V_{ds} and decreased negative V_{gs} yielded enhanced frequency performance metrics, with f_T ranging from 1.18×10^8 Hz to 5.16×10^{10} Hz and f_{max} from 5.23×10^8 Hz to 9.96×10^{10} Hz. The S_{21} parameter peaked at 11.2 dB with V_{gs} = −4.8 V and V_{ds} between 11 and 15 V. Furthermore, the stability factor K increased with higher V_{ds} and lower V_g, reaching a maximum of approximately 1.3, indicating unconditional stability. This work utilises small-signal parameters derived from measured S-parameters in ADS software 2022 to compare simulations with measurements through an equivalent circuit model.

This research aims to investigate how biasing influences GaN HEMTs, particularly their small-signal operation and RF performance. It proposes a systematic method for evaluating circuit components under varying bias conditions, which is crucial for optimizing GaN HEMTs for high-power and high-frequency applications, thereby advancing semiconductor technology.

2. Fabrication and Measurements

This study aims to investigate a HEMT based on an AlGaN/GaN heterostructure [36] grown by metalorganic vapor-phase epitaxy (MOVPE) on a 400-µm-thick silicon carbide substrate, as in Figure 1. A GaN buffer layer was incorporated into the design to achieve a 2-DEG at the AlGaN-GaN junction, which relies on the charge induced by polarization between the AlGaN and GaN layers, thereby providing a good number of electrons without the need for impurity doping. The device utilized a 20 nm Al0.253Ga0.747N barrier and a 1.5 µm GaN buffer epitaxial layer to achieve a good lattice match with the substrate (SiC). This was succeeded by a GaN channel layer and a very thin 5 nm AlGaN spacer layer, which also enables high-speed electron motion and facilitates the modulation of charge density through control of the gate bias voltage applied. To obtain low-resistance ohmic contact at the source and drain regions, a thin 5 nm cap layer of GaN was deposited. Important parameters recorded include the sheet resistance (RSH) of 324 Ω/□ from Hall measurements, and TLM showed the contact resistance (Rt) to be 0.36 Ω·mm. In Hall measurements, the charge density (N_S) was greater than 1.3×10^{13} cm^{-2}, and the most significant electron mobility was higher than 1400 $cm^2/V{\cdot}s$. The gate configuration comprised four 50 µm fingers, resulting in an overall gate width of 200 µm and a gate length of 0.15 µm. Ohmic contacts of Ti/Al/Ni/Au were created by thermally annealing at 900 °C. The mushroom-shaped Schottky gate consisted of a Pt/Ti/Pt/Au stack, which helps reduce the gate capacitance and consequently enhances the control of transconductance, while decreasing leakage and noise. The device was encapsulated with a 240 nm thick Si_3N_4 layer, deposited by PECVD at 340 °C, to further enhance efficiency and reliability. The transistors were manufactured using the UMS GH15 process. They were created through Molecular Beam Epitaxy (MBE) at IEMN in the University of Lille, France.

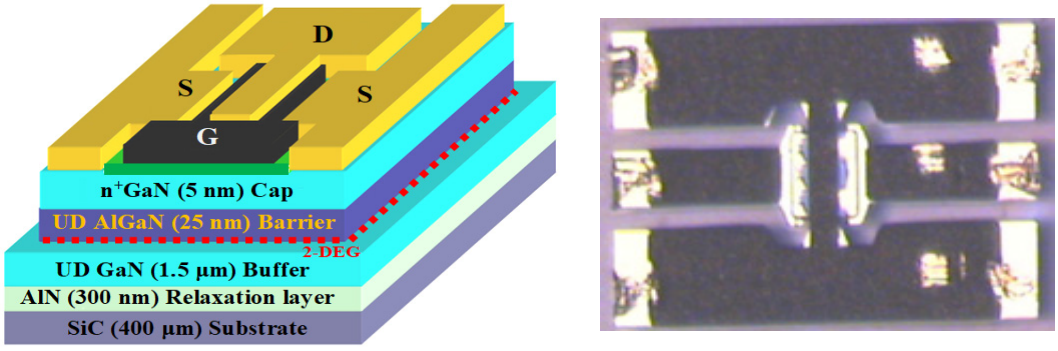

Figure 1. (**a**) Cross-section view of AlGaN/GaN/SiC HEMT structure (not to scale); (**b**) optical micrographs [36].

Four main steps comprise the device characterization process as illustrated in Figure 2: (1) S-parameter acquisition, (2) cold pinch-off technique, (3) de-embedding, and (4) ADS simulation flow. First, an HP8510C Vector Network Analyzer (VNA), with the aid of an HP4142B DC source, supplied the required current, connected via Ground-Signal-Ground (GSG) radio frequency probes that spanned 45 MHz to 50 GHz, to measure S-parameters. Multiple biasing conditions (V_{gs} from −6 V to –3 V and V_{ds} from 3 V to 15 V) were used for the measurements, and IC-CAP software 2022 was employed to automate data acquisition and ensure accuracy. In the second step, extrinsic parasitic components like inductances (L_g, L_d, L_s), resistances (R_g, R_s, R_d), and pad capacitances (C_{pg}, C_{pd}) could be accurately extracted by suppressing intrinsic device activity using the cold pinch-off technique with V_{gs} = −10 V and V_{ds} = 0 V. Third, by gradually modifying and eliminating capacitance values (C_{pg} and C_{pd}), a de-embedding procedure was carried out to eradicate

parasitic effects, especially the PDRZ effect, until the frequency-dependent anomalies in Re (Zij) were removed. Inductive and resistive parameters were also extracted using OFF-state bias data (V_{gs} = 0 V, V_{ds} = 0 V). A comprehensive small-signal equivalent circuit model was then constructed by importing the cleaned and bias-dependent S-parameter data into the Advanced Design System (ADS). Both extrinsic and intrinsic components (g_m, C_{gs}, C_{gd}, C_{ds}, R_{gs}, R_{gd}, and R_{ds}) were included in this model, which was validated through simulations under all tested frequencies and bias conditions.

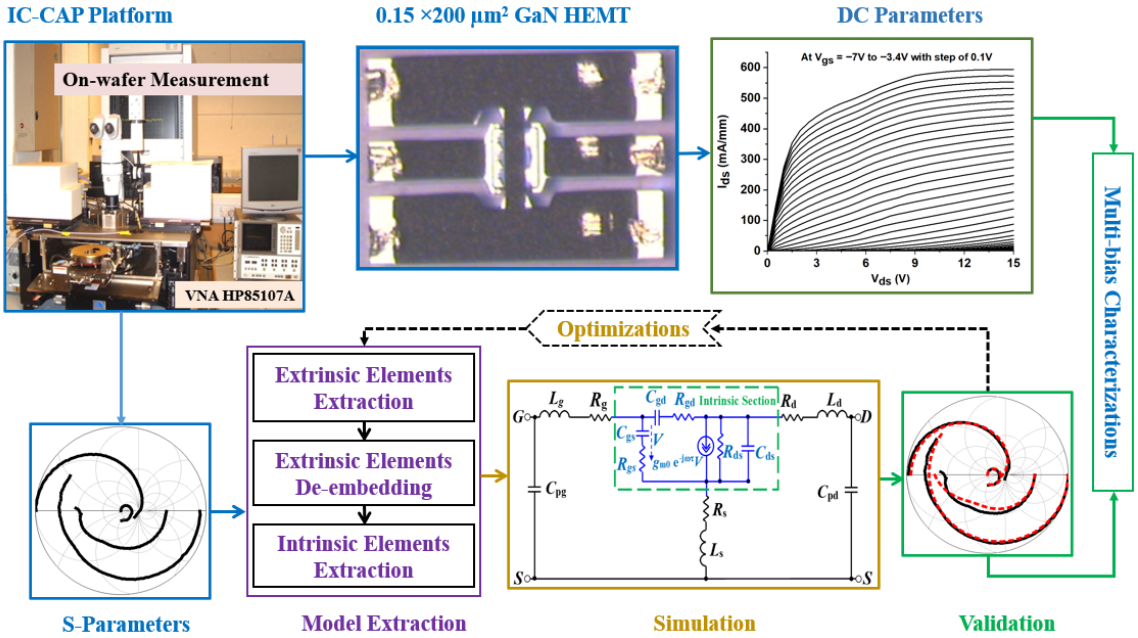

Figure 2. Diagram depicting the methodology for quantifying and assessing 150 nm GaN HEMT.

3. Results and Analysis

The operation of HEMTs can be described across different voltage regions. In the sub-threshold region, when V_{gs} is less than V_{th}, the current increases exponentially with V_{gs}, but is small enough, making it suitable for ultra-low-power device applications. When the dependence of V_{gs} surpasses Vth and V_{ds} is adequately elevated, the square law region fluctuates, yielding a current that is roughly equivalent to V_{gs} squared. This region is optimal for amplifiers due to the advantageous correlation between V_{gs} and current, making it a preferred choice in analog circuit designs. In this instance, the transconductance (g_m) increases with current. In contrast, elevated V_{gs} values lead to the saturation of carrier velocity within the velocity saturation region, maintaining constant transconductance and diminishing the increase in current, thereby affecting performance. When selecting V_{gs} = −3.0 V to −7.0 V and V_{ds} = 3 V to 15 V, it is recommended that V_{gs} be maintained above the threshold level for maximum amplification, and V_{gs} should not enter the velocity saturation region. Regarding the square-law region, its emphasis enables most of the HEMT's characteristics to be effectively exploited, which is why it is suitable for use in high-performance analog circuits.

3.1. DC Behavior with Biasing

Figure 3a illustrates the DC attributes of a GaN HEMT. Even with V_{ds} and V_{gs} equal to zero, there is practically no drain current (I_{ds}), which is usually less than the reverse leakage current [16]. As the gate voltage increases, the current through the drain also increases. The data can be divided into two main regions: the triode region, characterized by a linear increase in I_{ds} with rising V_{ds}, and the saturation region, where Ids becomes limited or

saturated once V_{ds} reaches a specific threshold due to channel constriction at the drain side [37]. From the I–V graph, two key metrics emerge: I_{dss}, the drain current when the transistor was saturated at V_{gs} = −3.0 V, measured at 109 mA, and $I_{dssm,}$ the maximum drain-source current at peak transconductance, recorded at 26 mA. Figure 3b,c show the transconductance (g_m) and transfer characteristics (g_m versus V_{gs} and I_{ds} versus V_{gs}). The maximum transconductance achieved was 62 mS at V_{gs} = −4.8 V and V_{ds} = 10 V, resulting in a ratio of 4.23 between I_{dss} and I_{dssm}, which indicates optimal small-signal gain [38]. The maximum transconductance values were determined at different combinations of V_{gs} and V_{ds}. The measurements revealed a transconductance of 46.23 mS with V_{gs} at −4.6 V and V_{ds} at 3 V. A transconductance of 54.48 mS was observed at a V_{gs} of −4.6 V and a V_{ds} of 6 V. The peak transconductance of 59.62 mS was attained at a V_{gs} of −4.7 V and a V_{ds} of 9 V. A value of 57 mS was recorded at V_{gs} of −4.8 V and V_{ds} of 12 V. A transconductance of 56.8 mS was observed at a V_{gs} of −4.9 V and a V_{ds} of 15 V. These values underscore the sensitivity of transconductance to variations in both V_{gs} and V_{ds} within the designated ranges. As V_{ds} increased from 3 V to 15 V, the peak transconductance (g_m) changed from −4.6 V to −4.9 V. This is because threshold voltage (Vth) varies with V_{ds}, a phenomenon known as "Vth roll-off" [39]. The roll-off has a significant impact on how well the device performs. As V_{ds} increases, Vth decreases, which means that V_{gs} must be adjusted to maintain the desired conduction levels. This behavior improves transconductance and overall efficiency between −4.6 V and −4.9 V. These differences demonstrate the importance of carefully managing circuit design to ensure that biasing, gain, and overall reliability are stable. Figure 3c shows that the threshold voltage (Vth) values had a consistent trend in the transfer characteristics (I_{ds} vs. V_{gs}). The Vth values were −5.06 V at V_{ds} = 3 V, −5.19 V at V_{ds} = 5 V, −5.32 V at V_{ds} = 7 V, −5.43 V at V_{ds} = 9 V, −5.50 V at V_{ds} = 11 V, −5.59 V at V_{ds} = 13 V, and −5.71 V at V_{ds} = 15 V. The decrease in Vth as V_{ds} rises suggests that higher drain-source voltages lower the threshold voltage, possibly because of short-channel effects like drain-induced barrier lowering (DIBL) [40]. This observation is essential for understanding device performance in low-voltage applications. V_{ds} and effective channel length influence Vth in short-channel HEMTs but remain unaffected by channel width [41]. The semi-log transfer curve in Figure 3d shows the drain-to-source dark current (I_{dso}) measurements, indicating a notable variation in current levels as V_{ds} increased. The dark currents observed were 1.66 pA, 0.27 pA, 8.85 nA, 4.42 nA, 0.78 nA, 2.38 µA, and 5.19 µA for V_{ds} values of 3 V, 5 V, 7 V, 9 V, 11 V, 13 V, and 15 V, respectively. This pattern suggests an exponential growth in dark current with increasing V_{ds}, possibly indicating enhanced carrier generation or reduced barrier potential at higher voltages [42,43].

3.2. Equivalent Circuit Parameters with Biasing

The equivalent-circuit approach [44], outlined in Figure 4, is employed to evaluate the S-parameters of the device. The equivalent-circuit parameters (ECPs) were determined using the "cold" pinch-off technique, a method that has been successfully used in GaN technology for many years. Our analysis focused on the extrinsic parameters of the semiconductor device, particularly the parasitic capacitances (C_{pg} and C_{pd}), parasitic inductances (L_g, L_d, and L_s), and terminal resistances (R_s, R_g, and R_d), among other factors. When the device was under pinch-off bias conditions (V_{ds} = 0, V_{gs} = −10 V), it was observed that the parasitic capacitances primarily affected the imaginary part of the Y parameters. We also examined the frequency dependence of these capacitances. Figure 5 depicts the behavior of Re (Zij) for the GaN device as a function of frequency under "unbiased" conditions. The device exhibited the PDRZ effect [45], with Re (Zij) starting to rise significantly for the GaN around 36 GHz. The values of Re (Zij) continued to rise with increasing frequency after this onset frequency. The PDRZ effect could be

removed from the de-embedded data by deducting the appropriate values of C_{pg} and C_{pd} from the measured data and gradually increasing them from zero until the effect was eliminated. To extract the extrinsic inductances, we used hypothetical Z parameters at OFF bias conditions (V_{ds} = 0, V_{gs} = 0 V) across a specific frequency range. The results showed that inductance L_g was significantly more prominent in devices with longer gate lengths. Additionally, it was found that the terminal resistances were heightened due to the influence of the contact metal in the semiconductor. Amongst the three terminal resistances, R_g was the smallest, reflecting the effects of metallization in this device. Table 1 presents all the extrinsic parameters of the device.

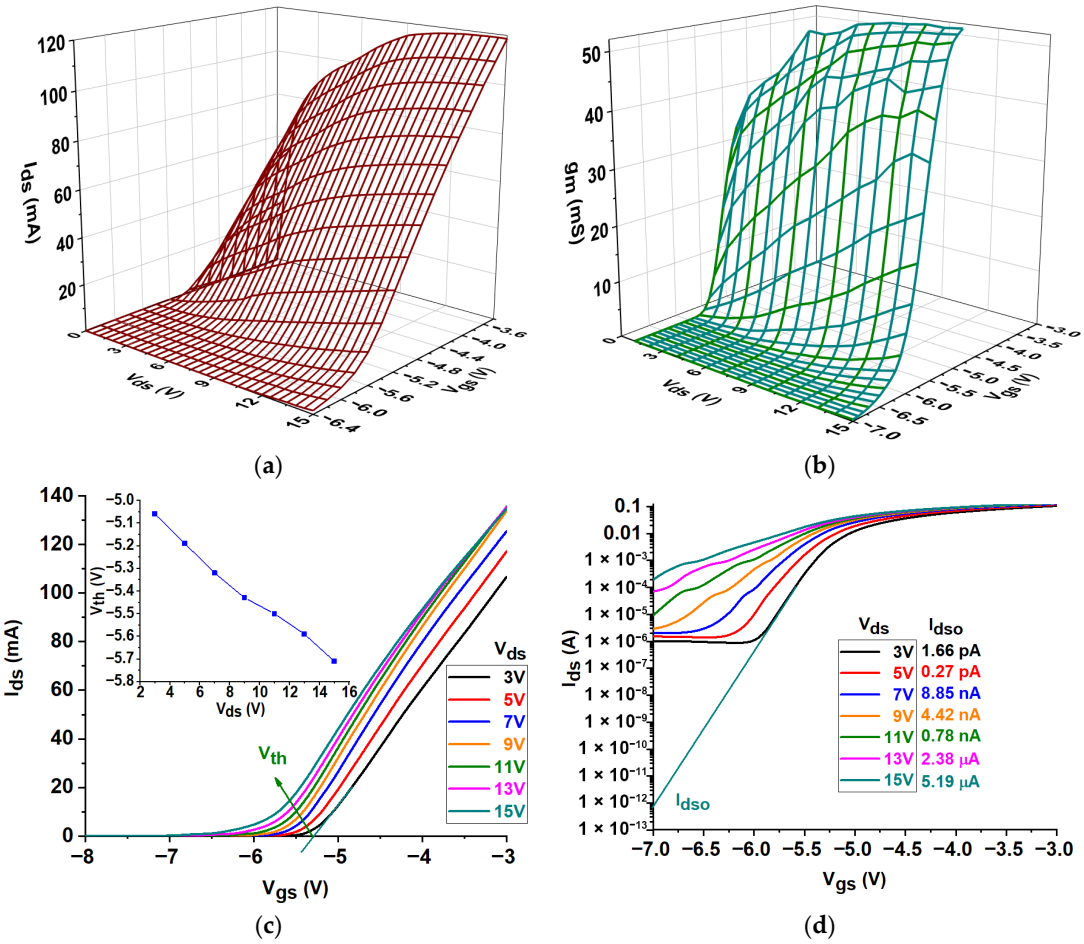

Figure 3. (**a**) DC characteristics, (**b**) transconductance characteristics, (**c**) transfer characteristics, and (**d**) semi-logarithmic transfer characteristics.

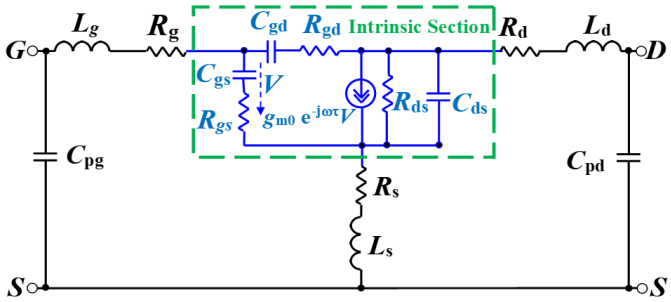

Figure 4. The equivalent circuit model for the investigated GaN HEMT.

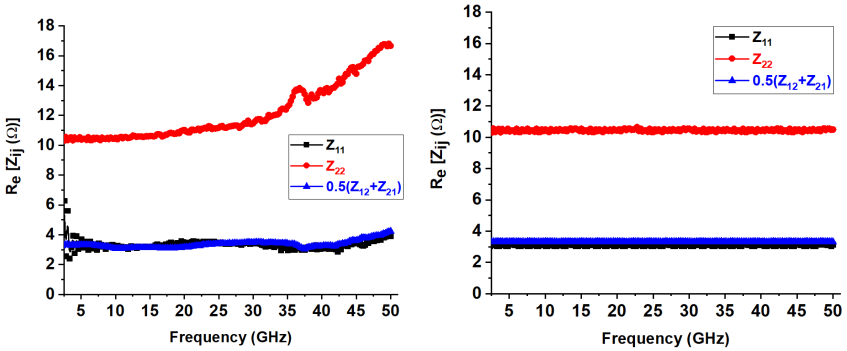

Figure 5. Re (Z_{ij}) against frequency under zero bias condition: (**a**) before and (**b**) after de-embedding of the extrinsic capacitances.

Table 1. Extrinsic parameter values of the GaN HEMT.

V_{gs} = 0 V and V_{ds} = 0 V (OFF Condition)	
Parameters	GaN HMET
L_g (pH)	142.0
L_s (pH)	1.80
L_d (pH)	64.0
R_g (Ω)	2.69
R_s (Ω)	3.10
R_d (Ω)	5.81
V_{gs} = −10.0 V and V_{ds} = 0 V (PINCH-OFF Condition)	
C_{pg} (fF)	51.0
C_{pd} (fF)	85.0

The initial phase of the extraction process is dedicated to identifying the extrinsic parameters. The intrinsic parameters can be established once these parameters are minimized. The applied bias ranged from V_{gs} = −6.0 V to −3.0 V and V_{ds} = 3 V to 15 V, with intrinsic parameters being extracted between 45 MHz and 50 GHz. Figure 6a shows that the gate-source capacitance, C_{gs}, went up when both V_{ds} and V_{gs} went up. C_{gs} stands for the capacitance between the gate electrode and the channel. It shows very non-linear behaviour. It includes both depletion and inversion charges, which are essential for determining the extrinsic cut-off frequency. C_{gs} decreases as V_{gs} decreases owing to the widening of the gate-source depletion region at higher negative voltages [46]. Furthermore, C_{gd} represents the feedback capacitance between the gate and drain, as shown in Figure 6b. Remarkably, this capacitance decreased at higher V_{ds}, contrasting with the lower C_{gd} values observed at high negative V_{gs} across varying V_{ds}. As V_{gs} increased at a constant V_{ds}, C_{gd} gradually rose. The subsequent capacitance analyzed is the drain-source capacitance, C_{ds}, depicted in Figure 6c with V_{gs} and V_{ds}. As V_{gs} rose from −6 V to −3 V, the C_{ds} values demonstrated a significant increase, especially at lower V_{ds} values. The capacitance substantially rose as V_{gs} transitioned from −6 V to −5.2 V, indicating a substantial effect of gate voltage on capacitance. The effect of changing V_{ds} is clear, especially in the middle range of V_{gs}. On the other hand, changing C_{ds} values has a bigger effect when V_{gs} changes. The series resistances, R_{gs} and R_{gd}, are derived from the real components of Y_{11} and Y_{12}, respectively. The charging delay resulting from non-quasi-static effects is depicted by the distributed channel resistances R_{gs} and R_{gd} [47] in Figure 7a,b. As V_{gs} went from −6 V to −3 V, the R_{gs} resistance values showed a clear downward trend. The resistance was relatively high when V_{gs} was low, such as around −6 V. However, it dropped significantly as V_{gs} increased, especially between −5.4 V and −4.8 V. This behavior indicates that within this

range, elevated gate voltages result in lower resistance. The overall trend suggests a more pronounced decline with increasing V_{gs}, even though variations in V_{ds} also affect the resistance values. As V_{gs} rose from −6 V to −3 V, the R_{gd} values typically exhibited a declining trend. At reduced V_{gs} values, especially at −6 V, the resistance was comparatively elevated, reaching its maximum at increased V_{ds} levels. As V_{gs} rose, particularly between −5.4 V and −4.8 V, R_{gd} declined considerably, indicating that elevated gate voltages result in reduced resistance. Although changes in V_{ds} affected R_{gs}, the main trend indicates that V_{gs} had the most significant impact on resistance characteristics. The "anomalous dip" in S-parameters is more pronounced in devices connected in series to gate-drain capacitance with higher effective gate-drain channel resistance (R_{gd}).

As the V_{gs} rose from −6 V to −3 V, the R_{ds} values usually showed a decreasing trend, as shown in Figure 7c. R_{ds} was relatively high at lower V_{gs} values (roughly −6 V), indicating that the device was less conductive. R_{ds} dramatically decreased as V_{gs} increased, particularly between −5.4 V and −4.8 V, suggesting that the device has better conductivity at higher gate voltages. The overall pattern indicates that higher V_{gs} values result in lower R_{ds}, underscoring the influence of gate control on the device's conductivity. In addition, the R_{ds} values vary with V_{ds}.

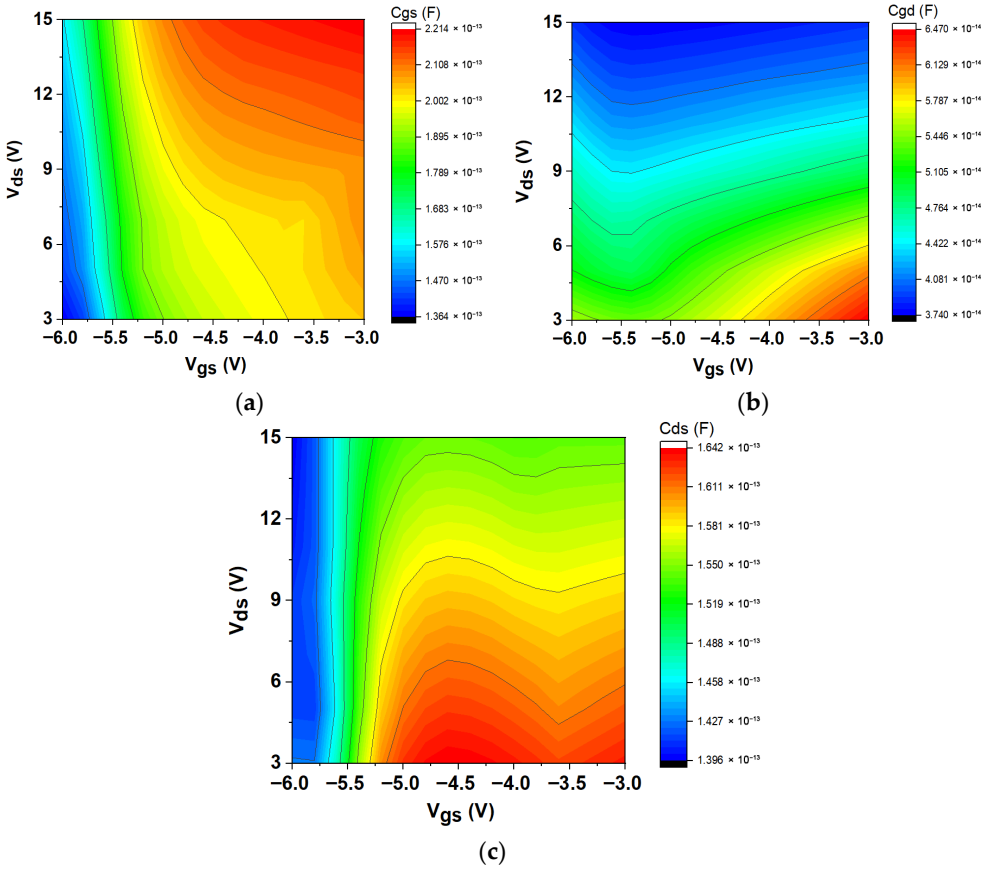

Figure 6. Variation in intrinsic capacitances plotted at different V_{ds} and V_{gs} for the AlGaN/GaN/SiC HEMT: (**a**) C_{gs}, (**b**) C_{gd}, and (**c**) C_{ds}.

Figure 8 illustrates the intrinsic transconductance (g_{mo}) alongside three intrinsic time constants (τ_{gm}, τ_{gs}, and τ_{gd}). The time constants arise from the transistor's inherent delay in reacting to rapid signal variations and represent the intrinsic non-quasi-static (NQS) effects that become increasingly pronounced at elevated frequencies. As V_{gs} transitioned from −6 V to −3 V, g_{mo} typically rose across all V_{ds} levels, signifying improved conductivity and the creation of channels within the transistor. The g_{mo} values were noticeably low

at V_{gs} = −6 V, suggesting that there was insufficient gate voltage for strong channel formation. On the other hand, g_{mo} attained significantly greater values at V_{gs} = −3 V, peaking at roughly 0.071 mS at V_{ds} = 11 V, suggesting adequate amplification. The data indicate that as V_{ds} increases, g_{mo} tends to stabilize, signifying that the transistor entered the saturation region where further increases in V_{ds} have a decreasing impact on g_{mo}. The time delay τ_{gm} in a transistor circuit indicates that as V_{gs} becomes less negative, τgm typically decreases. This means that charge carriers can move around more easily and respond faster. The time delay increased when Vgs was lower, such as when it was close to −6 V, because the conductivity was insufficient. On the other hand, values close to −3 V showed minimal delay, which is perfect for quick switching.

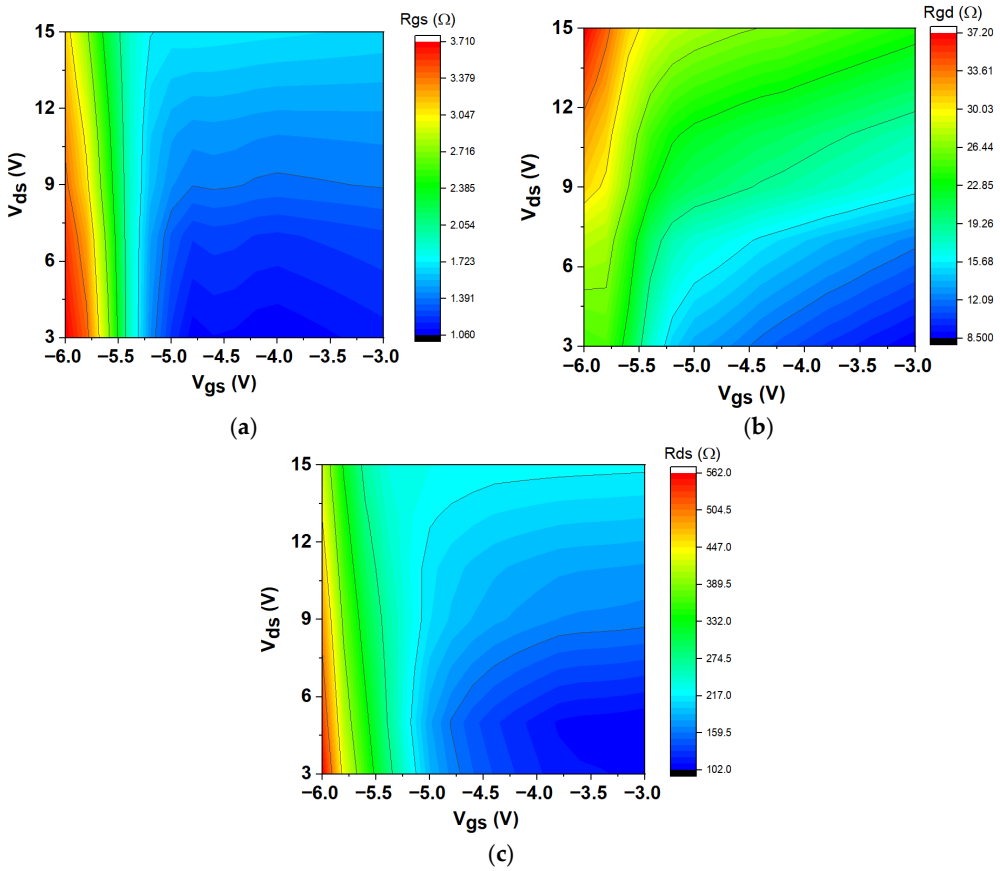

Figure 7. Variation in intrinsic resistances plotted at different V_{ds} and V_{gs}: (**a**) R_{gs}, (**b**) R_{gd}, and (**c**) R_{ds}.

Furthermore, increasing the V_{ds} can improve performance, although delays may stabilize at elevated levels due to saturation effects. This relationship is crucial for designing high-speed circuits. The intrinsic time delay values, τ_{gs}, ranged from approximately 3.18×10^{-12} s at V_{gs} = −6 V and V_{ds} = 3 V to about 1.29×10^{-12} s as V_{gs} approached −3 V with increasing V_{ds}. This pattern implies that lower τ_{gs} is linked to higher V_{gs}, suggesting a quicker transistor response, particularly at higher V_{ds} levels. The intrinsic time delay values τ_{gd} ranged from approximately 8.59×10^{-12} s at V_{gs}= − 6 V and V_{ds} = 3 V to about 3.47×10^{-12} s at V_{gs} = −3 V and V_{ds} = 3 V. A quicker gate-drain response was indicated by decreasing τ_{gd} values as the V_{gs} became less negative. According to this pattern, improved transistor switching speeds—which are essential for high-frequency applications—are a result of higher V_{gs}.

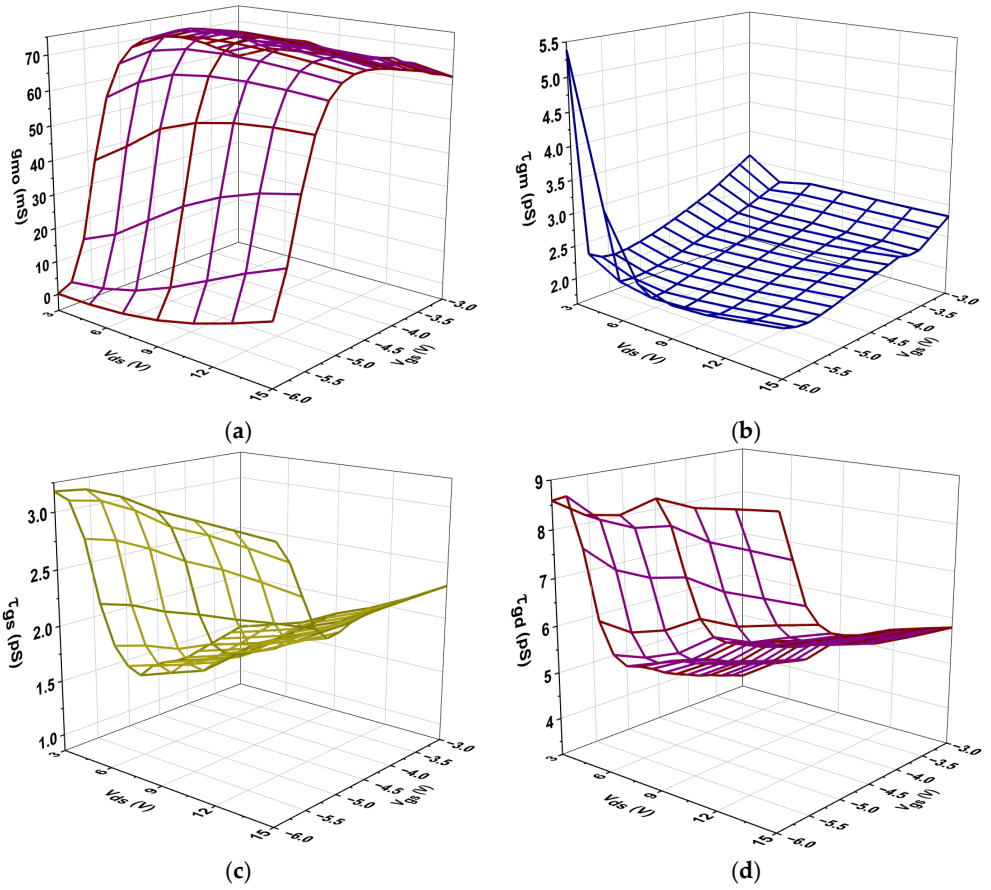

Figure 8. Variation in intrinsic parameters plotted at different V_{ds} and V_{gs} for the AlGaN/GaN/SiC HEMT: (**a**) g_{mo}, (**b**) τ_{gmo}, (**c**) τ_{gs}, and (**d**) τ_{gd}.

Even in the presence of parasitic effects, Figure 9 demonstrates that the measured h_{21} and MAG exhibited ideal behaviour, declining with frequency at a rate of −20 dB/decade. The f_t and f_{max} obtained from the data are displayed in the inset images in Figure 9c,d, which show an inversion at various V_{ds} values. When V_{ds} was higher and V_{gs} was less negative, the cutoff frequency (Figure 9a) typically increased, indicating improved device performance. The range of values was approximately 1.18×10^8 Hz to 5.16×10^{10} Hz. Better device performance under these bias conditions was indicated by the f_{max} (Figure 9b), which normally increases with increasing V_{ds} and decreasing negative V_{gs}. The range of the f_{max} values was approximately 5.23×10^8 Hz to 9.96×10^{10} Hz. The transistor's suitability for high-frequency applications, such as RF amplifiers and high-speed switching, is demonstrated by both f_t and f_{max} [48].

In Figure 10, the impact of biasing on the real part of Y_{21}, the magnitude of S_{21}, and the stability factor K, is illustrated. It is essential to note that the low-frequency values of both Y_{21} and S_{21} are specifically correlated with the intrinsic transconductance g_{mo}, as depicted below [49]:

$$Y_{21} = \frac{g_{mo}}{1 + g_{mo}R_s + g_{DS}(R_S + R_D)} \quad (1)$$

$$S_{21} = -2Y_{21}\left(Z_0 // Y_{22}^{-1}\right) \quad (2)$$

where Z_0 equals 50 ohms, which is generally much smaller than $1/Y_{22}$.

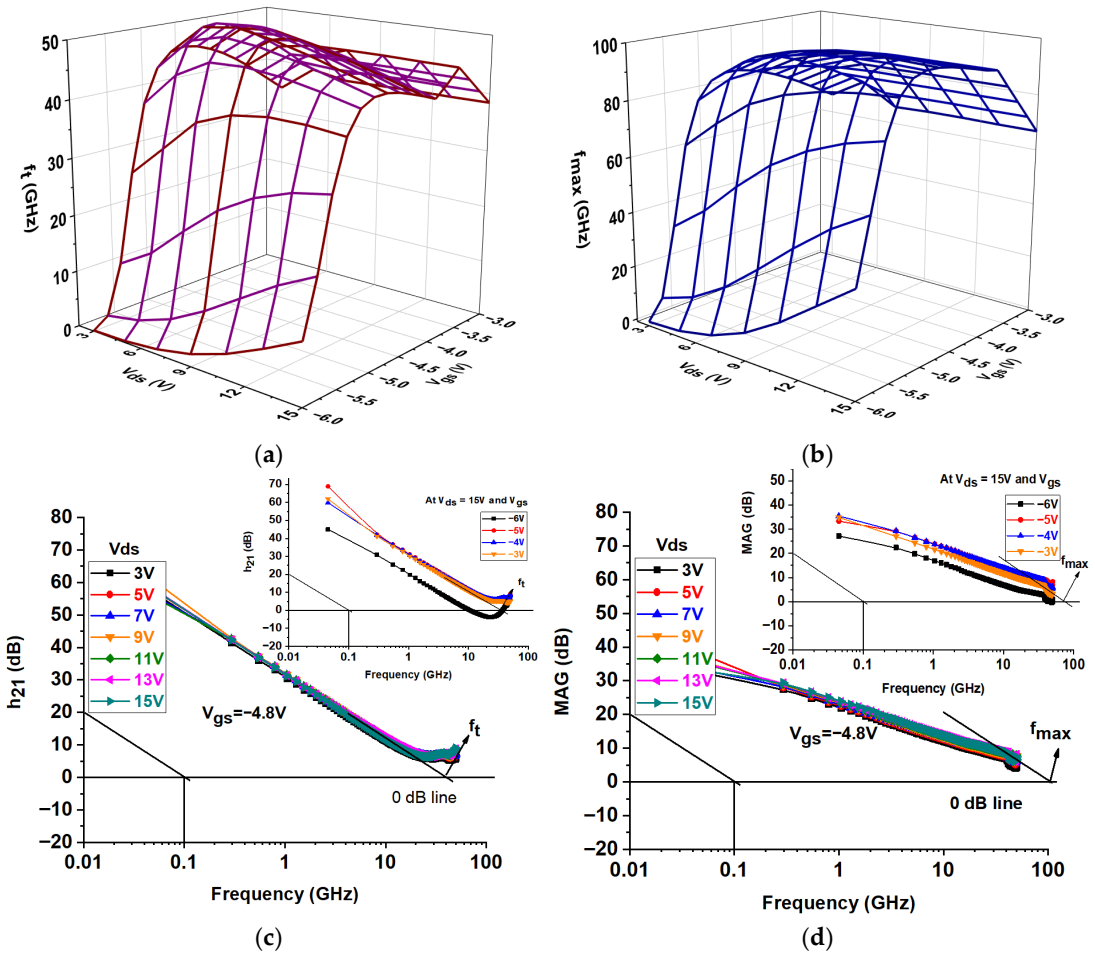

Figure 9. Variation in cut-off and maximum frequencies: (**a**) f_t, (**b**) f_{max}, (**c**) h_{21}, (**d**) MAG.

The S_{21} parameter indicates that the values were highly negative at lower V_{gs}, such as −6 V, but increased significantly as V_{gs} approached −3.0 V, reflecting improved signal transmission. The highest S_{21} values, approximately 11.2 dB, occurred when V_{gs} = −3.2 V and V_{ds} ranged from 11 to 15 V. Additionally, beyond a certain point, higher V_{ds} values resulted in smaller gains, indicating the transistor's limitations. As the drain-source voltage rose, the Y_{21} values typically increased with higher V_{ds} across the various V_{gs} values, indicating improved signal transmission. The Y_{21} values tended to rise as V_{gs} became less negative (going from −6 V to −3 V), suggesting improved conductivity and transmission properties of the transistor. The values, which fell between roughly 0.032 and 0.043, indicate that the transistor exhibits good signal amplification capabilities within the tested voltage range. As Vds rose, the stability factor K usually increased as well. This was especially noticeable at V_{gs} = −3 V, where K peaked at about 1.30. Conversely, lower V_{gs} values exhibited a decreasing trend in K for most V_{ds} levels, particularly at V_{gs} = −6 V, where K initially started at around 1.05 but increased slightly at higher V_{ds} values.

The equivalent-circuit model's precision in depicting the device's performance under these conditions is corroborated by the robust correlation between simulations and experimental data (Figure 11). Table 2 shows the coefficient of determination (R^2) and root mean square error (RMSE) values for each bias setting. This was to verify that the simulated and experimental results are in agreement. The model's accuracy was validated by the low RMSE and high R^2 values; the former indicates the magnitude of error between the simulated and observed S_{21} values, while the latter demonstrates the robustness of the linear

correlation. This validation is essential for assessing practical performance, optimizing design, and advancing complex RF integrated circuit designs.

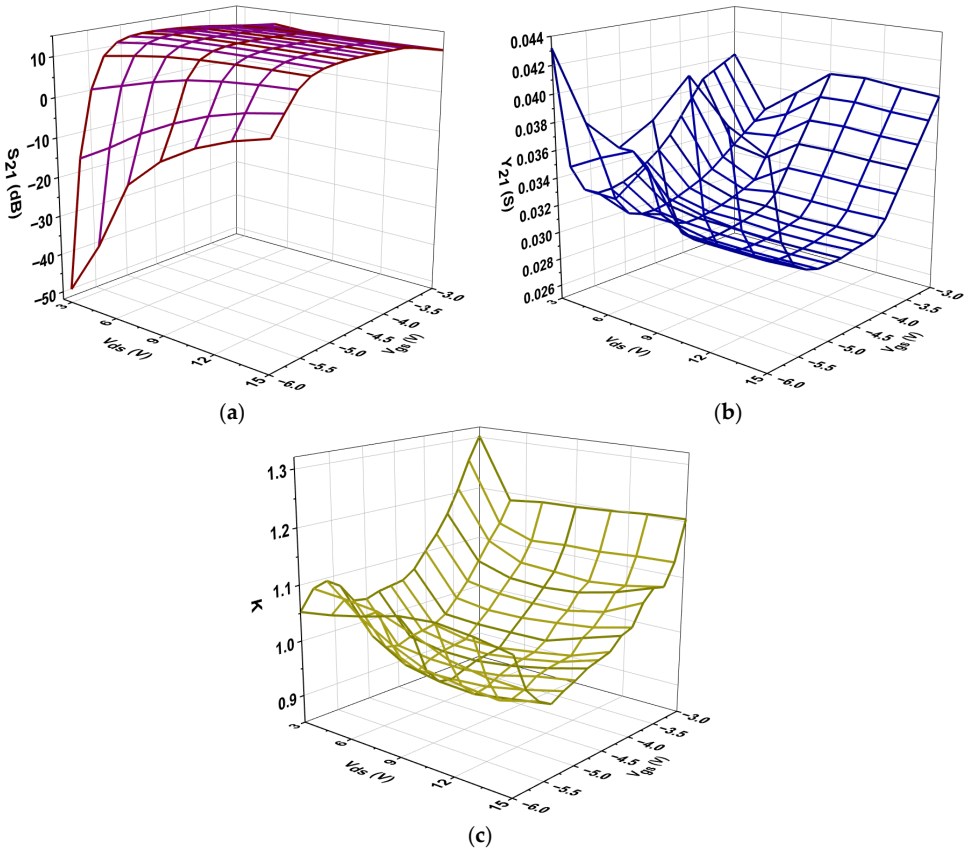

Figure 10. Variation in the intrinsic parameters: (**a**) S_{21}, (**b**) Y_{21}, and (**c**) K.

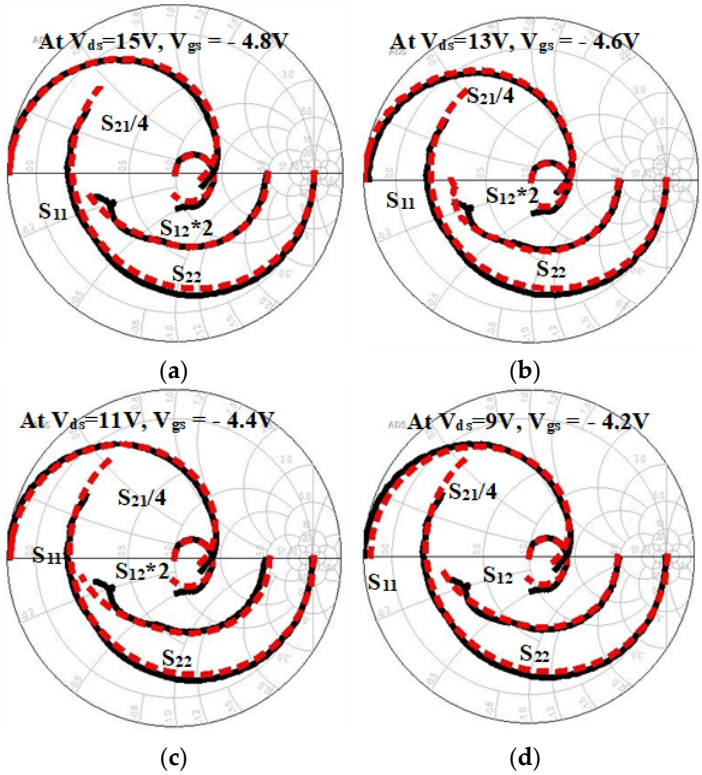

Figure 11. Verification of experimental (black) and modeled (red) data: (**a**) at V_{ds} = 15 V, V_{gs} = −4.8 V, (**b**) at V_{ds} = 13 V, V_{gs} = −4.6 V, (**c**) at V_{ds} = 11 V, V_{gs} = −4.4 V, and (**d**) at V_{ds} = 9 V, V_{gs} = −4.2 V.

Table 2. Quantitative comparison between simulated and experimental data (Figure 11).

Bias Condition (V_{ds}, V_{gs})	RMSE (dB)	R^2 Value
V_{ds} = 15 V, V_{gs} = −4.8 V	0.52	0.993
V_{ds} = 13 V, V_{gs} = −4.6 V	0.47	0.991
V_{ds} = 11 V, V_{gs} = −4.4 V	0.43	0.994
V_{ds} = 9 V, V_{gs} = −4.2 V	0.39	0.995

The data in Table 3 illustrate the performance of the GaN HEMT at varying V_{ds} with a constant V_{gs} of −4.8 V. The I_{ds} consistently rose from 21.81 mA to 54.71 mA as V_{ds} increased from 3 V to 15 V, suggesting better conduction and increased amplification potential. The transconductance (g_m) peaked at 61.25 mS at 7 V, and the intrinsic g_{mo} also peaked at 73.77 mS under the same conditions. This indicates that the output current control is functioning properly. The C_{gd} went down, which is good because it would reduce the Miller effect and make things more stable. However, the C_{gs} went up, which could mean that switching speeds would be slower. The resistances of R_{gs} and R_{gd} also increased, which could alter the input impedance and the amount of power used. Higher distributed resistance and a delayed charge response are likely causes of the increasing trend of R_{gd} with V_{ds}, resulting from non-quasi-static effects and increased voltage stress across the gate-drain region at higher drain biases.

Table 3. DC, RF, and intrinsic parameters for various drain biases at V_{gs} = −4.8 V.

V_{ds} (V)	I_{ds} (mA)	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_{gs} (Ω)	R_{gd} (Ω)	R_{ds} (Ω)	g_{mo} (mS)	τ_{gm} (ps)	τ_{gs} (ps)	τ_{gd} (ps)	f_t (GHz)	f_{max} (GHz)	S_{21} (dB)	Y_{21} (S)	K
3	21.81	45.45	192.51	55.62	163.79	1.08	13.04	166.01	67.96	2.27	1.31	4.55	45.81	84.72	12.70	0.0327	1.04
5	29.54	50.02	195.91	52.68	162.17	1.15	14.83	158.10	72.57	2.15	1.42	4.89	50.92	92.34	13.45	0.03093	0.97
7	37.73	61.25	197.27	49.16	160.65	1.23	16.63	177.12	73.77	2.17	1.52	5.13	51.62	96.01	13.63	0.03052	0.96
9	43.65	56.36	201.39	45.20	159.13	1.39	20.07	196.14	73.66	2.20	1.76	5.70	50.46	98.12	13.74	0.03049	0.96
11	47.75	56.88	205.21	42.21	157.56	1.46	21.87	201.70	72.90	2.24	1.89	5.79	48.80	98.90	13.75	0.03037	0.97
13	51.40	56.58	209.26	39.76	156.01	1.58	24.49	213.99	71.70	2.30	2.08	6.11	46.82	98.76	13.72	0.03041	0.99
15	54.71	55.83	212.77	37.65	154.46	1.70	27.11	226.28	70.26	2.35	2.27	6.41	44.83	98.16	13.66	0.03048	1.01

R_{ds} showed some fluctuation, which could affect efficiency and heat generation. Time constants (τ_{gm}, τ_{gs}, τ_{gd}) also increased with V_{ds}, resulting in longer response times and potentially limiting high-speed performance. f_t reached its highest point at 51.62 GHz at 7 V, and f_{max} rose to 98.90 GHz at 11 V. This means that the device can work at high frequencies. Overall, the forward gearbox gain, S_{21}, increased slightly, indicating that amplification remained stable. The forward transconductance parameter, Y_{21}, remained constant, indicating that the device remained stable. The stability factor K remained close to 1, indicating that the entire device operated effectively.

4. Discussions and Future Directions

This study thoroughly investigates the performance of the 150 nm AlGaN/GaN HEMT on a SiC substrate in the DC, RF, and small-signal regimes. Essential conclusions are emphasised, including the necessity for precise V_{ds} control in high-frequency applications and the threshold voltage's (Vth) susceptibility to the drain-source voltage (V_{ds}), which signifies short-channel phenomena such as DIBL. The study found that transconductance (g_m and g_{mo}) also changed with bias points, which suggests that charge transport is not linear. The highest intrinsic transconductance occurred at V_{gs} = −4.8 V and V_{ds} = 11 V, which was when the small-signal gain was at its highest. This highlights the importance of parasitic elements, such as capacitances (C_{pg}, C_{pd}) and resistances (R_g, R_s, R_d), and illustrates how they affect high-frequency performance and frequency-dependent behaviour. Capacitance trends also indicate that increasing V_{gs} and V_{ds} could enhance forward gain and mitigate

the Miller effect. This can improve high-frequency parameters, such as f_t and f_{max}. The research illustrates the influence of intrinsic resistances on conductivity and switching times, indicating that enhancements in resistance at reduced negative gate biases facilitated expedited carrier movement and diminished RC time delays. The S-parameter and Y-parameter responses confirm that signal transmission was improved and the RF amplifier performed well in various situations. Ultimately, the study offers essential insights for future RF circuit designs by validating the equivalent circuit model through substantial concordance with both measured and simulated results.

Future research must focus on several critical domains. To determine how GaN HEMTs will perform over time, they must undergo accelerated ageing tests, particularly under various biasing conditions. This will help us understand how the devices break down, how they fail, and how stable their performance is in high-power, high-frequency applications. A comparative analysis of GaN HEMT performance on various substrates, including SiC, Sapphire, and Si, could also shed light on the trade-offs between power handling, efficiency, cost, and scalability. Additionally, because non-linearities and parasitic effects become more pronounced at higher frequencies, future research should focus on enhancing thermal management, developing innovative packaging technologies, and optimizing device design to ensure that devices operate effectively in the mmWave and terahertz ranges. We also need better methods to address issues with device uniformity that arise due to fabrication tolerances. These tolerances are necessary to ensure that devices function consistently across a wide range of commercial applications. Ultimately, future research should incorporate noise figure measurements and power handling tests to gain a deeper understanding of how GaN HEMTs function. To further enhance the dependability and power handling capabilities of GaN HEMTs for high-frequency applications, effective thermal management techniques should be employed.

5. Conclusions

The detailed analysis reveals that the GaN HEMT device has considerable potential for high-frequency applications. It also illustrates the complexity of the relationship between performance metrics and biasing conditions. When there was no bias, the device had a low drain current. As the gate voltage (V_{gs}) increased, the drain current (I_{ds}) also increased. There were two distinct operating regions: the triode and saturation regions. Key metrics, such as Idss and maximum transconductance (g_m), show that the device could significantly amplify signals, especially when the bias levels are just right. The observed decrease in threshold voltage (Vth) as the drain-source voltage (V_{ds}) increased indicates that drain-induced barrier lowering (DIBL) and other important short-channel effects were occurring. To ensure the device works properly, these effects must be kept in check. Additionally, the dark current's exponential growth with higher V_{ds} suggests that more carriers were being generated, which could render high-voltage applications less reliable. Finding the equivalent circuit parameters reveals how parasitic components impact a device's operation. For example, capacitances and resistances are very sensitive to changes in V_{gs} and V_{ds}. Analysis of the intrinsic parameters shows that response times were faster and transconductance was better at lower negative gate voltages. These parameters are crucial for applications that require rapid switching. In the end, the equivalent-circuit model and the experimental data agreed very well with each other, indicating that the model is accurate in predicting the performance of a device. This study not only enhances our understanding of how GaN HEMTs function, but also provides valuable insights for developing more effective designs in cutting-edge RF integrated circuits.

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