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Physics-based reverse recovery modelling of ultrafast recovery diodes with carrier lifetime control

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Abstract: Ultrafast recovery diodes are often used in high frequency switching applications because of their ability to switch from the ON-state to OFF-state very quickly. However, ultrafast recovery diode switching performances are very difficult to predict using Technology Computer-Aided Design (TCAD) simulation tools, especially when carrier lifetime is adjusted. To model carrier lifetime, the Shockley-Read-Hall (SRH) recombination theory is used in TCAD tools as a standard simulation model. This model is not sufficient as it considers the presence of only one deep energy level located at the material mid-gap. Used as a carrier lifetime killer, platinum doping introduces several deep energy levels facilitating the minority carrier recombination. Thus, this paper presents a new approach based on trap physical modelling. Trap characteristics are determined using Deep Level Transient Spectroscopy (DLTS) measurement technique. This approach can significantly reduce the large mismatch observed between the ultrafast recovery diode turn-off measurements and the standard simulation model results.

Keywords: ultrafast PIN diode, Turn-off transient characteristics, platinum diffusion, minority carrier lifetime control, Deep Level Transient Spectroscopy (DLTS)

1 Introduction

Ultrafast recovery diodes are a key component in power electronic circuits when used as free-wheeling diodes. Power switches like IGBTs require very hard turn-off conditions on the diodes, by forcing fast current

decrease that can lead to high over-voltages. Thus, recovery diodes must exhibit a soft recovery behaviour to limit over-voltages and oscillations, a low reverse recovery current to enable high dI/dt diode capability at turn-off, and low energy losses during recovery which implies a very short reverse recovery time.

Various carrier lifetime control techniques are used in the industry in order to improve the electrical characteristics of power devices by reducing their switching time delay. The reduction of carrier lifetime can be made by the diffusion of metallic impurities such as gold and platinum, or by high energy electronic irradiation (Baliga & Sun, 1977).

Commonly used in industry, the metal doping lifetime control technique is based on the intentional introduction of metal atoms into the semiconductor devices in order to create deep energy levels in the material's band-gap. Those levels act as intermediate energy levels in the material band-gap and facilitate the carrier displacement between the conduction band and the valence band. As a result, carrier recombination is enhanced and the minority carrier lifetime is reduced, which can significantly reduce the switching time delay of power devices. Unfortunately, the carrier lifetime reduction generates an increase in the on-state voltage drop (VF). A trade-off between static and dynamic power device performance is therefore required (Baliga & Sun, 1977; Hauf, et al., 2018).

The location of defect energy levels in the material band-gap is important as it impacts the leakage current. Indeed, a defect energy level located at the material mid-gap generates a higher leakage current than energy level located far from the mid-gap. For this reason, platinum is used as an alternative to gold despite its efficiency in carrier lifetime control. Indeed, studies have shown that gold generates much higher leakage current than platinum (Baliga & Sun, 1977; Badr, 2017).

Simulation TCAD tools have always been essential in the field of research. Used to model and predict the real behaviour of new technologies, they offer industrial development at a lower cost. The predictive power of simulation TCAD tools is based on the models chosen to represent the real phenomena that occur in the device. In some cases, simulation models need to be calibrated to reduce prediction errors.

Platinum modelling is not available in the TCAD Sentaurus tools as it is for boron and phosphorus. The simulation model commonly used, to describe the deep level recombination, is the Shockley-Read-Hall (SRH)

recombination model. In fact, SRH takes into account the presence of only one deep level located at the centre of the material band-gap. (Hall, 1952).

This study uses ultrafast power diodes on silicon substrates doped with platinum atoms. Several deep levels platinum-related into the silicon bandgap are currently being measured using the Deep Level Transient Spectroscopy (DLTS) technique. To account for the presence of these energy levels in the simulation model, the SRH recombination model has been replaced by a new approach. This approach is based on data from DLTS measurements of trap characteristics. Traps are characterized by their energy levels E_T , trap capture cross-sections σ_T , and the trap concentrations N_T .

Finally, an advanced measurement technique is performed to determine the platinum concentration profile in the silicon bulk for each deep level. This method is based on both, DLTS measurements and current-capacitance measurements.

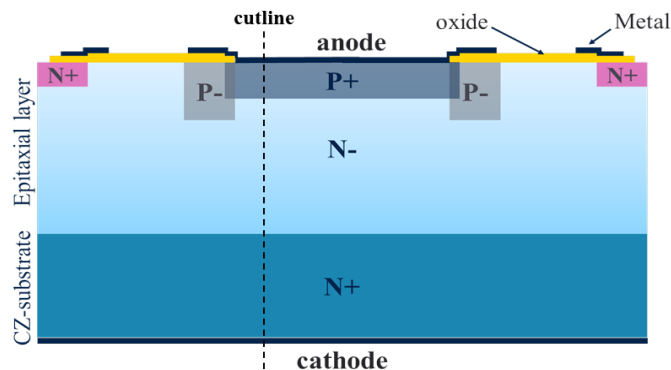
2 Experimental Results

2.1 Device properties

This section presents the ultrafast diode samples modelled with TCAD Sentaurus tools. The diode was designed and manufactured by STMicroelectronics. It consists of a $P^+N^-N^+$ structure of an epitaxial Czochralski grown N-type silicon substrate.

The diode structure is composed of a lightly N-doped layer (N^-) in between a heavily P-doped anode layer (P^+) and a heavily N-doped cathode layer (N^+) (Figure 1).

Figure 1 The $P^+N^-N^+$ diode cross section view



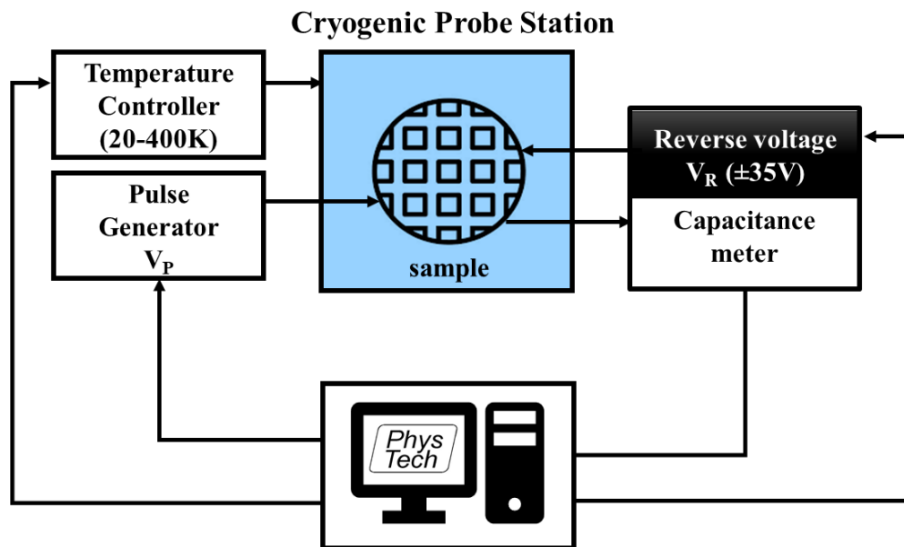
The central region of the diode has a doping concentration of approximately 10^{14} at.cm⁻³. Its thickness is designed in order to support a breakdown voltage of 750 V. The diode structure peripheries are composed of a P-doped guard rings and N⁺ regions. This design allows to protect the diode from a premature destruction which can occur when the diode is reverse-biased, by avoiding tightening of the equipotential bonding at the device edges.

to improve device switching performance, the diode is doped with platinum atoms at the end of the manufacturing process and prior to the metallization step. The platinum atoms diffuse from a Pt-silicide layer formed on the front surface of the device. platinum is then thermally annealed for hours at over 800 °C.

2.2 Deep Level transient Spectroscopy measurements

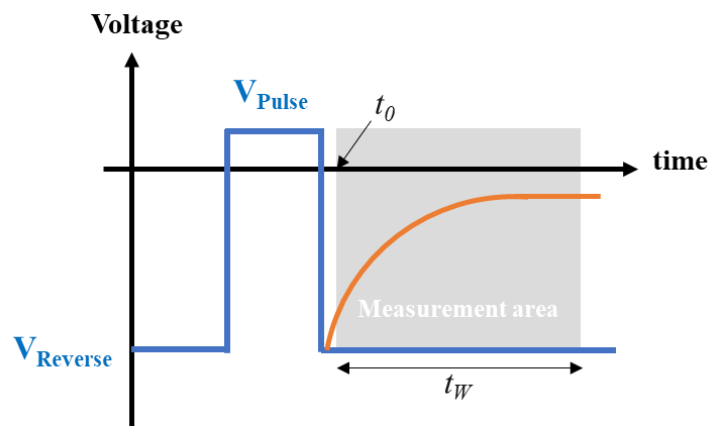
This section describes the physical measurements used to characterize platinum-related defects in ultrafast recovery diodes. The DLTS is a non-destructive measurement technique, proposed by Lang in 1974 (Lang, 1974), to characterize traps (defects) in semiconductors. It is based on measurement of the emission rate of trapped charge carriers as a function of temperature. A temperature scan ranging from 20 K up to 400 K is needed in order to activate all the traps present in the silicon band-gap. The sample is therefore placed under a computer controlled cryogenic probe station (nitrogen ambient) (Figure 2).

Figure 2 The DLTS measurement workbench



A reverse voltage V_R of -10 V is first applied to the diode, in order to empty all present traps from charge carriers. The diode is then supplied with a filling pulse (V_P) of +1 V. The pulse voltage is maintained during 0.1 ms to fill all the traps present in the silicon band-gap. The diode is then reverse biased again in order to emit (reject) all carriers captured by traps during the previous phase. At t_0 the capacitance transient is recorded till t_W (Figure 3).

Figure 3 The DLTS measurement applied voltage

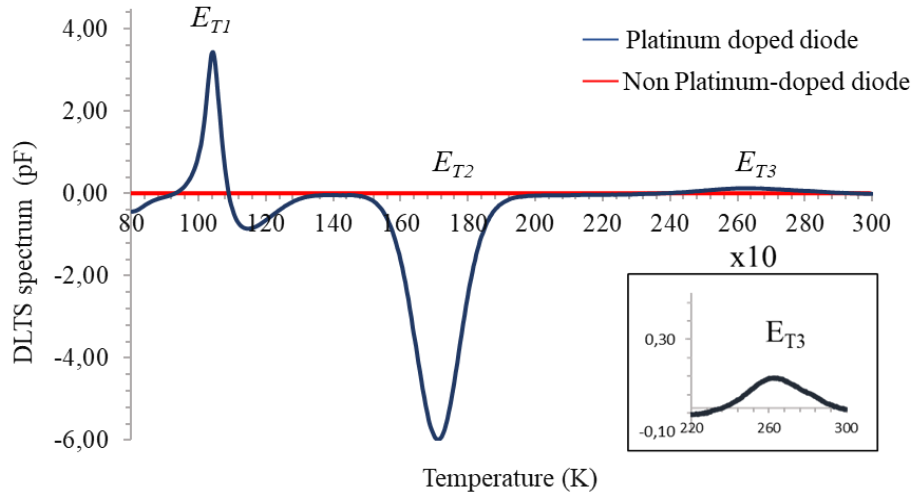


DLTS measurements was first performed on power diodes without platinum and then compared with measurements performed on platinum-doped diodes in order to detect any non-platinum contaminations.

DLTS measurements performed on the platinum-doped diodes show the presence of three different deep levels in the silicon band-gap. In contrast, no defects are observed in DLTS measurements performed on non-platinum doped samples. This confirms that all the defects detected are platinum-related (Figure 4).

Note that the DLTS software is configured to give positive peaks for majority carriers and negative peaks for minority carriers (PhysTech, 2012). Thus, the two positive peaks detected at 105 K and 265 K are identified as electron traps. The negative peak detected at 170 K is identified as a hole trap.

Figure 4 DLTS measurement on the P⁺N⁻N⁺ ultrafast recovery diode



The first trap E_{T1} (at 105 K) is an electron level located at 0.22 eV from the conduction band. The second trap E_{T2} (at 170 K) is a hole level located at 0.32 eV from the valence band. The third trap E_{T3} (at 265 K) is an electron level located at 0.50 eV from the conduction band.

Based on the literature, E_{T1} and E_{T2} are identified as substitutional platinum defect (Pt_s), and the E_{T3} is identified as a defect complex Pt-X. Due to its very low amplitude at the sample surface compared to the other two defects, this mid-gap defect (E_{T3}) is not systematically detected and not considered in all defect studies. In some studies, it is considered as a platinum-hydrogen (Pt-H) defect complex (Prohinig, et al., 2018; Badr, et al., 2014), while others consider that it is platinum-oxygen (Pt-O) defect complex (Kwon, et al., 1987). As the Pt-H complexes can be dissociated at an annealing temperature above 450 °C (Badr, 2017), the E_{T3} level is probably a platinum-oxygen defect complex, which is due to the CZ diode substrate. The CZ substrate is known to have a higher oxygen content than the FZ substrate (Vervisch, 2005).

Our experimental results obtained by DLTS measurements are in a good agreement with at least three studies. (Prohinig, et al., 2018) present three energy levels located at $E_C-0.23$ eV, $E_V+0.36$ eV, and $E_C-0.50$ eV. (Kwon, et al., 1987) present three energy levels located at $E_C-0.23$ eV, $E_V+0.36$ eV, and $E_C-0.52$ eV. (Gill, et al., 1990) present three energy levels located at $E_C-0.23$ eV, $E_V+0.32$ eV, and $E_C-0.55$ eV.

The DLTS measurement technique allows to determine the physical characteristics of traps. It gives information about the trap type, the trap energy levels, the trap concentration, and the trap capture cross section. All

of these parameters are integrated into the trap simulation model in the Sentaurus TCAD tools (Table 1).

Table 1 Trap physical properties obtained with DLTS measurements

	<i>Energy level (E_T)</i> [eV]	<i>Concentration (N_T)</i> [at.cm ⁻³]	<i>Capture cross section (σ_T)</i> [cm ²]
E_{T1}	E _C -0.22	$1.14 \times 10^{+14}$	5.38×10^{-14}
E_{T2}	E _V +0.32	$4.34 \times 10^{+12}$	2.69×10^{-12}
E_{T3}	E _C -0.50	$3.89 \times 10^{+10}$	1.00×10^{-15}

The trap energy levels are determined from the Arrhenius plot of the emission rate as a function of temperature T. The following expression denotes the Arrhenius-equation in the case of an N type region (PhysTech, 2012).

$$\ln(\tau_e V_{th,n} N_C) = \frac{E_C - E_T}{k} \frac{1}{T} - \ln(\chi_n \sigma_n) \quad (1)$$

τ_e denotes the emission time constant, $V_{th,n}$ the electron thermal velocity and N_C the state density. χ_n is the enthalpy factor, σ_n is the electron capture cross section and k is Boltzmann constant.

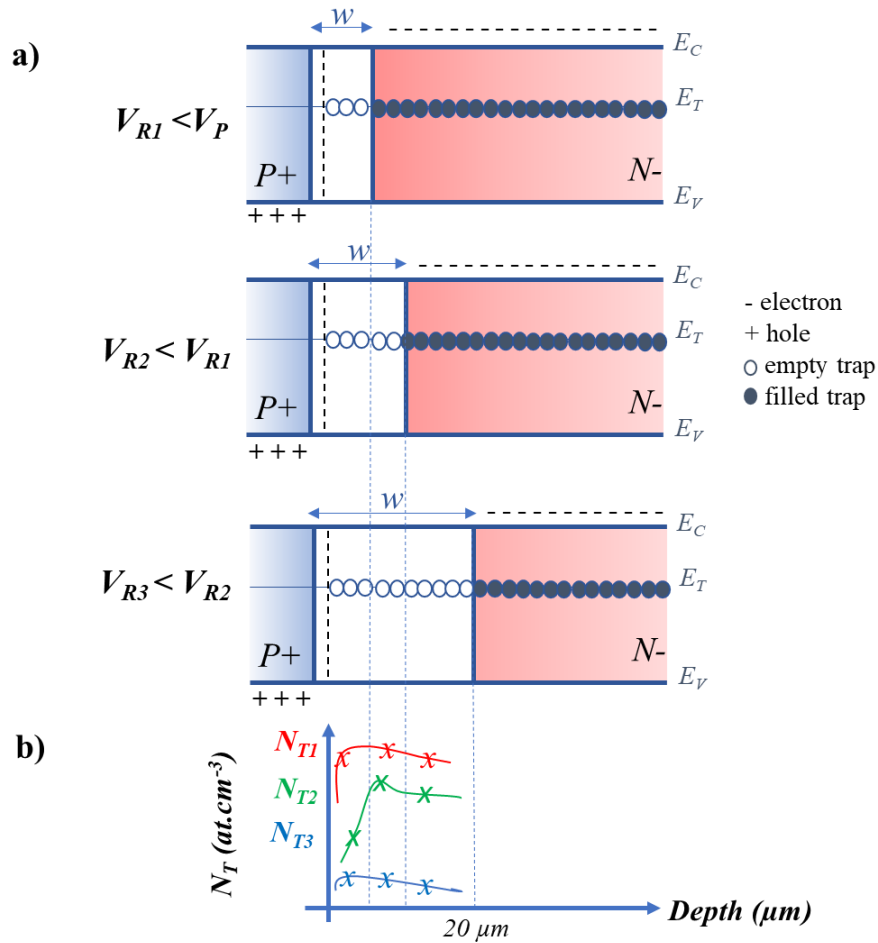
The capture cross section of the trap is the intersection of the Arrhenius plot of equation (1) with the y-axis giving the product $\chi_n \sigma_n$.

The DLTS measurements provide a single value of the trap concentration measured near the diode junction. Typically, the trap simulation model assumes a constant trap concentration throughout the device structure, which is not the case in reality. In fact, several studies show that platinum concentration has a symmetrical distribution (Kwon, et al., 1987; Vervisch, 2005; Jacob, et al., 1997; BALIGA, 2008; Hazdra, et al., 1999). It increases near the wafer surface, decreases in the middle of the wafer volume and then increases to reach the wafer backside surface. Then, it forms a symmetrical U-shape through the center of the wafer. A half profile is sufficient in our case to cover the entire intrinsic zone of the diode, allowing a shorter time simulation.

In this work, the platinum concentration profile of each trap level is considered in the trap simulation model. The platinum concentration profile is determined by varying the reverse voltage V_R applied to the PIN diode from -1 V to -35 V (equipment limitation). In fact, the thickness of the probed area is dependent on the reverse voltage that is applied. It

increases as the reverse voltage increases. With a maximum of -35 V, the probed area is about 20 μm from the diode junction. This allows to determine the trap concentration profile near the surface (Figure 5).

Figure 5 a) Measurement approach based on reverse voltage variation. b) Trap concentration depth profile.



The obtained platinum depth profiles of E_{T1} and E_{T2} traps are not sufficient as they stop at 20 μm in the diode bulk. Their depth profiles are mathematically extrapolated as a function of the depth.

The concentration of the third trap (E_{T3}) is very low and difficult to measure. For that reason, some authors neglect it (Kwon, et al., 1987; Gill, et al., 1990; Vervisch, 2005). Close to the silicon mid-gap, it is known as a carrier generation center. It was shown by (Hazdra, et al., 1999) that the concentration profile of a trap near the midgap is proportional to the

generation current. Thus, a method based on reverse current-voltage (I-V) and capacitance-voltage (C-V) characteristics allowed to determine the third trap concentration profile.

The depth profile is then calculated from the generation current density (J_{gen}) as a function of the depletion width (w), as expressed in equation (2).

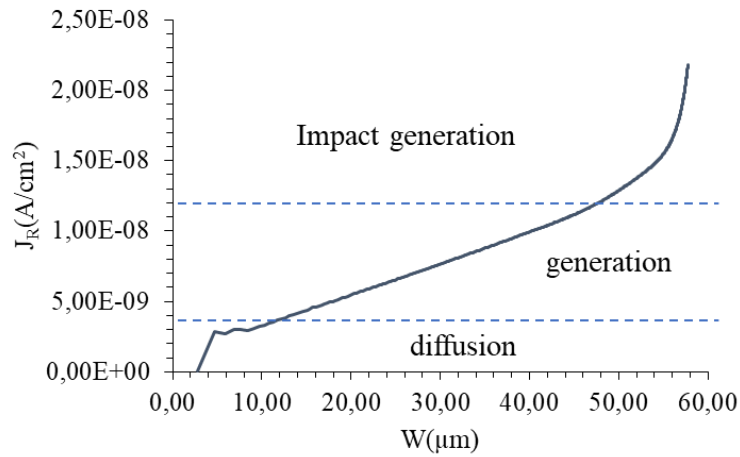
$$N_T(w) = \frac{1}{q\xi} \frac{dJ_{gen}}{dw} \quad (2)$$

Where q is the elementary charge and ξ is the trap emissivity.

The generation current density is obtained from the reverse current density (J_R), as it is the sum of the generation current density (J_{gen}) and the diffusion current density (J_{diff}).

Currents are then separated by the method proposed by (Murakami and T.Shingyouji, 1994). This method consists of plotting the reverse current density (J_R) as a function of the depletion width (w) calculated from the C-V characteristics (Figure 6). This leads to a linear dependence of the reverse current density on the depletion width.

Figure 6 The reverse current density as a function of the depletion region depth



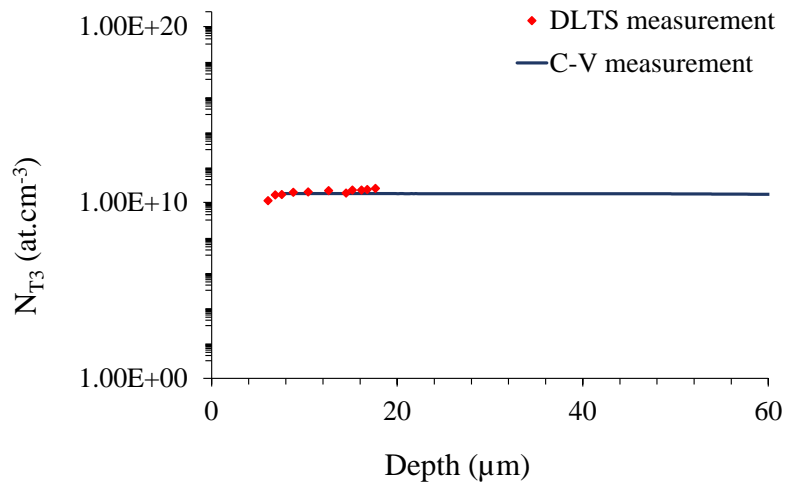
The linear part of the reverse current density is the generation current density. The current diffusion (J_{diff}) is given by the y-intercept.

The trap emissivity ξ can be determined from equation (2) using E_{T3} concentration measured by DLTS near the junction. With the E_{T3} trap concentration measured by DLTS near the diode junction, the emissivity calculated is 394 s^{-1} . This value is consistent with the trap emissivity

calculated previously by (Prohinig, et al., 2018) and (Rasinger, et al., 2019) respectively 470 s^{-1} et 450 s^{-1} .

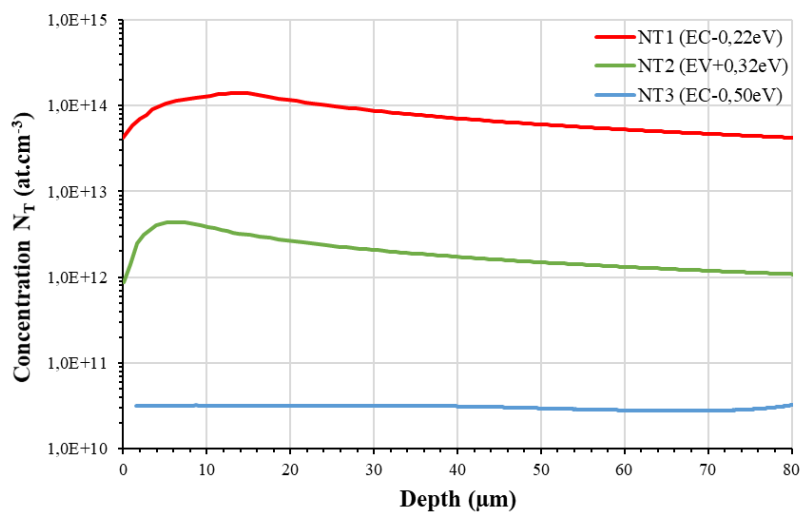
The obtained E_{T3} trap concentration depth profile from C-V measurements and the depth profile obtained from DLTS measurements are in a good agreement (Figure 7).

Figure 7 E_{T3} trap concentration depth profile obtained by DLTS and C-V measurements



The concentration depth profile of each trap is presented in Figure 8, and then implemented in trap model in the simulation tools.

Figure 8 The concentration depth profile of each trap obtained by DLTS and C-V measurements



3 Results and discussions

3.1 Simulation model methodology

As mentioned earlier, the Shockley-Read-Hall recombination model consider a single deep level located near the silicon mid-gap in addition to the dopant energy levels. It is based on the value of electrons and holes lifetime which is used as a calibration parameter to control the switching rate. Thus, the new approach based on DLTS measurements describes more precisely the physical phenomena involved.

To overcome the SRH recombination model limitations, the SRH model is disabled in the simulation and a trap model is introduced. The DLTS measurements performed on the ultrafast recovery diode are used in the new model, such as the trap type, the energy level, the capture cross section (Table 1), and the concentration depth profile of each trap.

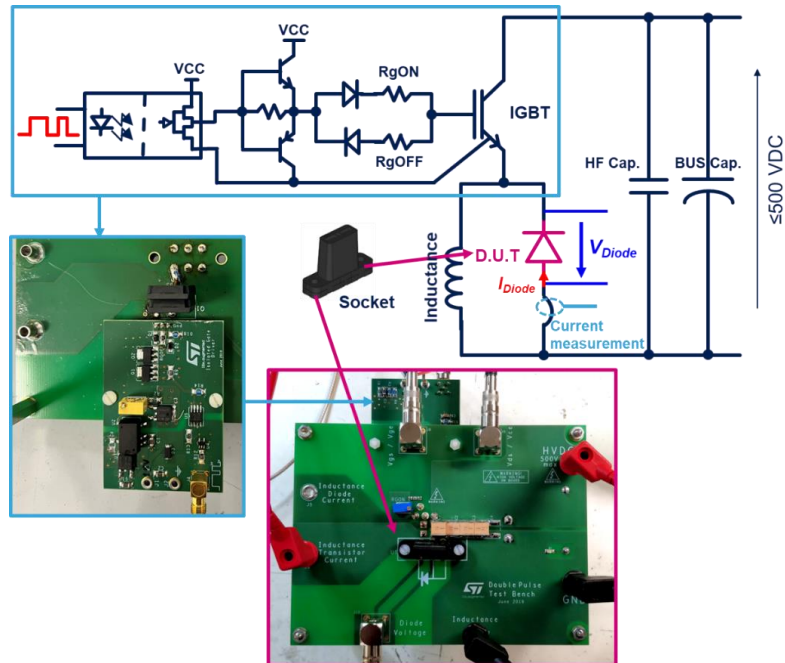
To validate the new diode simulation model, the electrical behavior of the ultrafast recovery diode is investigated under the switching mode. The key parameters which allow to evaluate the carrier lifetime model are the reverse recovery time delay (t_{rr}), the maximum reverse current (I_{RM}), and the reverse recovery charges (Q_{rr}). For this purpose, simulations are performed with the new trap-based model, but also with the standard SRH recombination. The SRH recombination model is used with its default parameters. The simulation results are then compared with the electrical measurement results performed on the ultrafast recovery diode in the switching mode at room temperature. The experimental workbench that is used for the reverse blocking measurements is simulated in the TCAD tools.

Figure 9 presents the experimental workbench and its electrical circuit schematic used in simulation to operate the ultrafast recovery diode in the switching mode. The ultrafast recovery diode acts as a freewheeling diode controlled by an IGBT (Insulator Gate Bipolar Transistor) in a dual pulse measurement circuit. When the IGBT is in the "OFF" state, the current from the inductive load is transferred to the freewheeling diode. when the IGBT switch to the "ON" state, the diode is switched. The current delay dI/dt is controlled by the gate resistors R_{gON} and R_{gOFF} of the IGBT.

For the simulation, parasitic inductors are considered in the electric circuit in order to include the IGBT and the diode packaging losses.

The "BUS cap." capacitors are used to keep the VDC voltage constant during current draw. However, these capacitors generate a lot of parasitic inductance. Thus, "HF cap" capacitors are used in order to counteract the effects of these parasitic inductances generated during current transients.

Figure 9 The experimental workbench and its schematic used to operate the diode in the switching mode

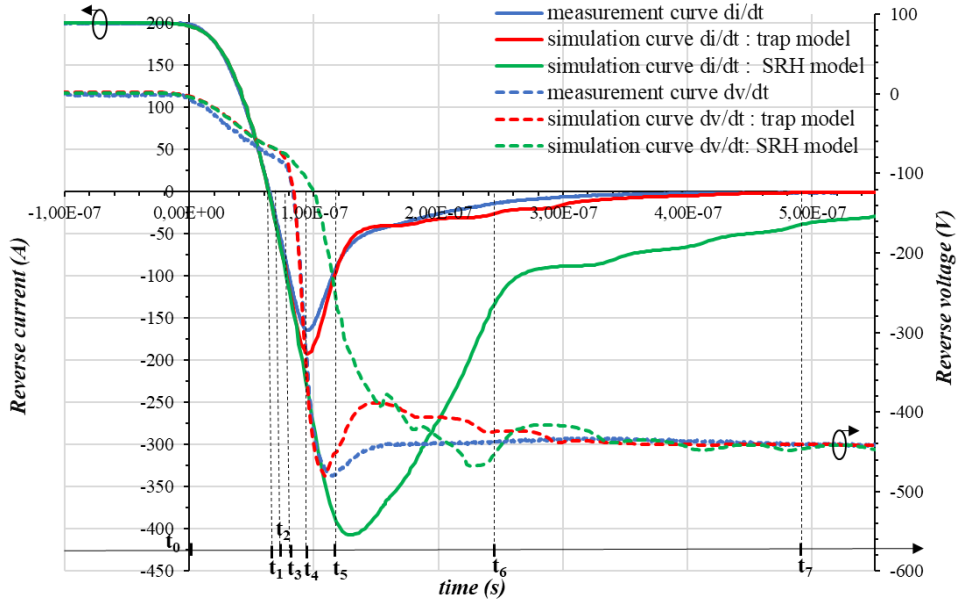


The measurements of the reverse current and the reverse voltage as time function are performed at an initial current level of 200 A and a high current delay dI/dt . The reverse voltage V_R is set to -500 V (VDC in Figure 9).

3.2 Reverse recovery characteristic analysis

The measured and simulated recovery waveforms (reverse current dI/dt and reverse voltage dV/dt) are superimposed on the same graph. The simulated recovery waveforms are first carried out with the standard simulation model SRH (green curves), then with the new based-trap model (red curves) (Figure 10). The comparison leads to a large gap between simulation results performed with SRH model and measurement results. The simulation results performed with our new recombination model based on trap description shows a small gap with measurements compared to SRH model.

Figure 10 Simulated curves with both recombination models compared to the measurements performed in the switching mode



The results are also compared by calculating the percentage deviation between the measurement and simulation results.

Table 2 contains the simulation results at room temperature performed with the standard SRH model and the new approach based on the trap description. The simulation results performed with the SRH model show a significant gap between the simulation and the experimental results. The percentage deviation on simulated I_{RM} is about +148 %, and on simulated t_{RR} about 128 %. The simulation results performed with the trap model significantly improve the simulation performance. In terms of I_{RM} , the simulation results performed with the new approach are in good agreement with the measurements with a percentage deviation around 17.0 %. The t_{rr} and Q_{rr} show a good agreement with measurements with a percentage deviation of 22.5 % which is acceptable compared to the initial gap obtained with SRH recombination model.

Table 2 Percentage deviation of simulation results from measurements in the dynamic mode at room temperature

$25^{\circ}\text{C}, 5000\text{A}/\mu\text{s}$	$I_{RM} [A]$	$Q_{RR} [\mu C]$	$t_{RR} [ns]$	$t_a [ns]$	$t_b [ns]$
<i>SRH model</i>	148,1%	544,2%	127,9%	111,99%	131,5%
<i>Trap model</i>	17.3%	22.5%	22.3%	3.04%	26.38%

The t_{RR} is divided into two parts, “ t_a ” and “ t_b ”. The parameter t_a corresponds to the time when the reverse current decreases and reach I_{RM} . In this case, the evacuation depends not only on the carrier lifetime but also on the current decay di/dt . The parameter t_b corresponds to the time when the reverse current increase from the I_{RM} to zero. The simulated t_a with trap model is coherent with the measurements (3% of deviation). At t_b , the carrier evacuation depends mostly on the minority carrier lifetime. The IGBT can also impact the tail current delay (di/dt) by the nonlinear change of its parasitic capacitance C_{gc} , known by Miller effect, which can justify a considerable part of the gap obtained on simulated t_b with the trap model. The hole density distribution, simulated with the trap model at different time during the switching allows to observe the displacement of the excess carriers in the diode bulk (Figure 11). At different switching times indicated on Figure 10, a cut line is made on the device structure (Figure 1). At t_0 , when the current is equal to the initial current level (when the diode is conducting), the injected carriers (holes) are uniformly distributed in the hole N^- region. From t_1 , when the current is decreasing, the excess carriers begin to be removed from the P^+N^- junction by diffusion and recombination, and the depletion region begins to expand in the central region. This can be visualized by plotting the electric field evolution as a function of the switching time (Figure 12). At t_4 , the current is equal to the I_{RM} and the reverse voltage increase to reach the applied value of V_R . From t_4 to t_7 , the reverse current grows up to zero with a slope determined by the diode characteristics. When there is remaining charge at the cathode side (N^+), as in our case, it means that recombination dominates the carrier evacuation resulting a slow tail current (Cappelluti, et al., 2006).

Figure 11 The hole density distribution during reverse recovery in ultrafast recovery diode at room temperature

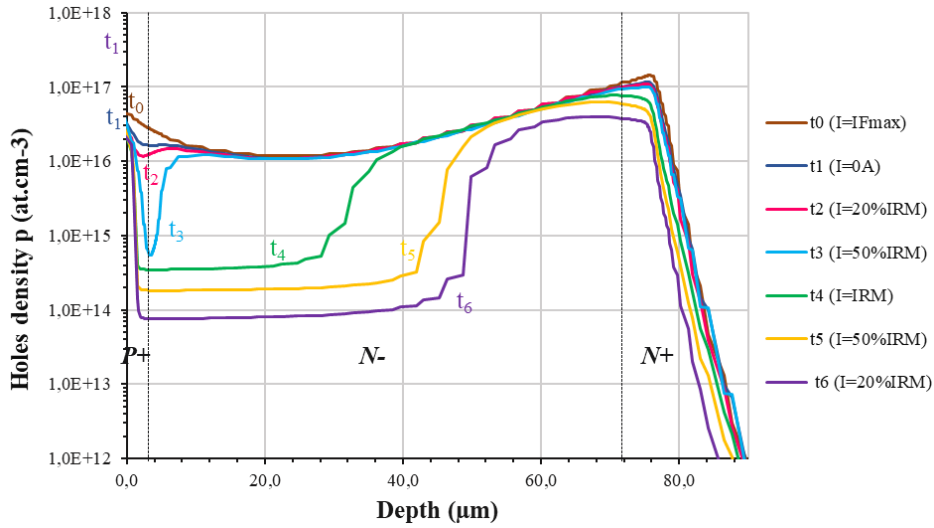
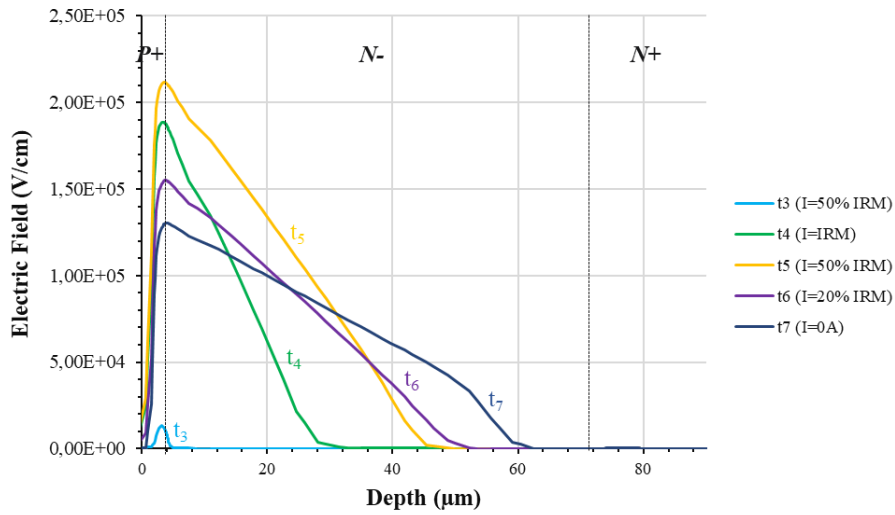


Figure 12 The Electric Field evolution during reverse recovery in ultrafast recovery diode at room temperature



5 Conclusion

Electrical simulation results of the ultrafast recovery diode performed with the standard SRH recombination model showed a big difference with the measurements in the switching mode. To improve the obtained results, a

new approach based on trap description is performed and gives a better agreement with the measurements. Traps induced by platinum doping were characterized using DLTS measurements, which identified three different level in the silicon band-gap. An electron trap is located at 0.23 eV from the conduction band, a hole trap is located at 0,32 eV from the valance band and another electron trap which is located at the mid-gap. Platinum concentration depth profile is determined for each trap by varying the reverse voltage applied to the PIN diode. Due to the equipment limitations, capacitance and reverse current measurements were performed in order to determine the mid-gap level concentration depth profile. Thus, the new simulation model allows not only to predict the electrical behavior of platinum doped diodes in the dynamic mode, but also to investigate the phenomena occurring during the diode Turn-off such as the minority carrier displacement for different switching times.

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Physics-based reverse recovery modelling of ultrafast recovery diodes with carrier lifetime control

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