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# Low-Latency Software Polar Encoders and Decoders for Short Blocklengths

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**Abstract**—This paper presents our low-latency Polar code encoders and decoders developed for the 2025 International Symposium on Topics in Coding (ISTC 2025) contest, which challenges participants to implement the fastest possible channel code encoders and decoders in terms of average and maximum latency on a CPU target. Our solution is based on Polar codes with an Adaptive Successive Cancellation List (ASCL) decoder.

We introduce a novel ASCL unrolled decoder generator. We conduct an extensive exploration of the design space, including code construction, CRC selection, and list size, to identify optimal trade-offs between signal-to-noise ratio and decoding time across various operating points. The considered operating points are frame error rates of  $10^{-3}$  and  $10^{-5}$ , information bit lengths of 64, 128, 256, and 512, and code rates of  $1/4$ ,  $1/2$ , and  $4/5$ . We also propose an optimized bit-packed encoder.

All implementations of the encoders and decoders, along with the code construction and the unrolled decoders generator, are released as open source in the AFF3CT toolbox.

## I. INTRODUCTION & RELATED-WORKS

The ISTC 2025 Challenge advances the emerging field of software-defined channel decoding by tasking participants with developing low-latency, high-performance C++ encoders and decoders for short blocklength codes on single-core CPUs, evaluated across various code rates and block sizes.

In our submission<sup>1</sup>, we focus on Polar codes [1] concatenated with a CRC. For decoding, we employ an Adaptive Successive Cancellation List (ASCL) decoder, which first attempts low-latency SC decoding and only falls back to SCL decoding if necessary [2], [3]. This approach achieves the error-correction performance of SCL decoding while significantly reducing average latency.

While Polar decoder optimization typically receives the most attention, we also propose a bit-packed encoder in Section II. On the decoder side, we leverage and refine FAST-SSC-List decoding, unrolling, and vectorization techniques (Section III) to reduce latency. These optimizations enable high-throughput software decoding on general-purpose CPUs. A comprehensive design space exploration in Section IV identifies optimal SNR/latency trade-offs. All source code and tools are released in the open source AFF3CT toolbox [4].

## II. BIT-PACKED ENCODER

The encoder implementation relies on bit-packing and proceeds in four stages. First, the input vector  $U_N$ , containing

both frozen and information bits, is generated. This is done by statically identifying constituent nodes at compile time: rate-0 nodes are skipped, and large rate-1 nodes can be vectorized during memory copy. Second,  $U_N$  is bit-packed using SIMD instructions, specifically `_mm256_cmpgt_epi8` followed by `_mm256_movemask_epi8`, which extracts the MSBs of each 8-bit element to form packed output. Third, systematic Polar encoding is performed using vectorized XOR and shift operations, applied intra- or inter-register depending on the node position in the encoding graph. Finally, unpacking is achieved using a 256-entry lookup table of 256-bit values.

## III. UNROLLED ASCL DECODER

The decoder implemented in this work follows the ASCL decoding principle. This approach aims to reduce the average latency of Polar decoders without compromising error-correction performance. Decoding begins with a fast SC decoder. If the decoded codeword passes the CRC check, it is accepted immediately. Otherwise, the decoder falls back to more powerful SCL decoders with increasing list sizes  $L$ . This adaptive strategy significantly lowers the average decoding time in high-SNR regimes, where SC decoding is often sufficient, while preserving the robustness of SCL decoding in more challenging conditions. The ASCL mechanism is well suited for short blocklength codes, where latency is critical.

To achieve low latency, we adopt a fully unrolled decoder generation strategy. For each Polar code configuration used in the contest, a dedicated and specialized C++ source file is generated. This eliminates control-flow overhead such as loops and recursive function calls, making the approach particularly effective for short blocklengths where latency is critical. We provide an open source decoder generator tool<sup>2</sup>, which supports SC, SCL, and ASCL decoding modes. The tool produces optimized C++ code tailored to each frozen set, enabling reproducibility and integration into larger systems.

## IV. SEARCH SPACE AND EXPLORATION

To identify optimal trade-offs for the ISTC 2025 contest, we explored various code and decoder configurations, including different code constructions (GA, 5G) [5], [6], CRC lengths and polynomials – including some polynomials that do not correspond to standard CRCs – and list sizes  $L$ . This search

<sup>1</sup>Contest code and materials: [https://github.com/aff3ct/istc25\\_contest](https://github.com/aff3ct/istc25_contest).

<sup>2</sup>Polar decoder generator: [https://github.com/aff3ct/polar\\_decoder\\_gen](https://github.com/aff3ct/polar_decoder_gen)

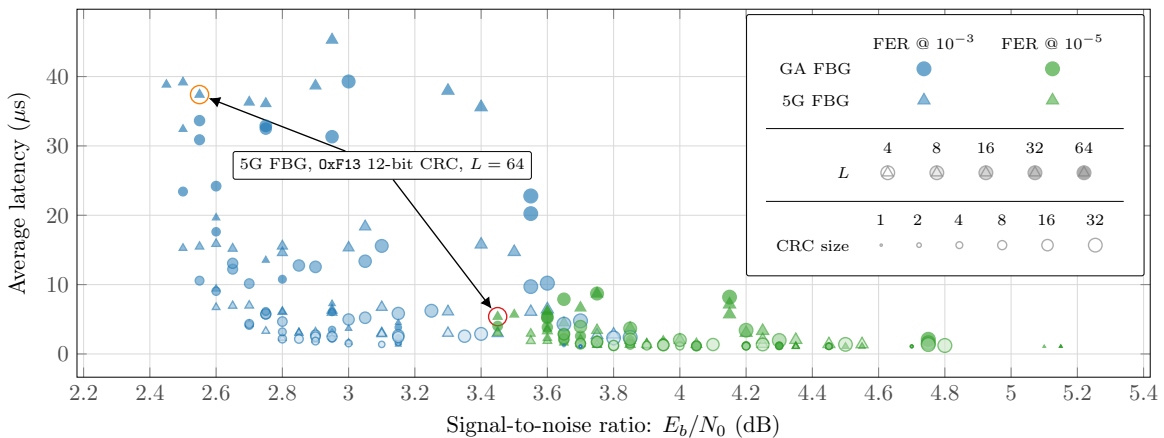


Fig. 1. Space exploration of the ASCL decoder performance for  $K = 128$  and  $R = 1/2$ . Measured latencies from the AFF3CT generic ASCL decoder running on one core of an Intel Xeon Gold 6140 CPU. The selected code is highlighted in orange for FER @  $10^{-3}$  and in red for FER @  $10^{-5}$ .

TABLE I  
PROPOSED CODES FOR THE CONTEST WITH THE CORRESPONDING ACHIEVED PERFORMANCE (FULLY UNROLLED ASCL DECODERS).

Rate	$K$	Code specifications			Encoder $\mathcal{L}_{\text{worst}}$ ( $\mu\text{s}$ )	Decoder				
		CRC size	CRC poly.	Fb. gen.		FER @ $10^{-3}$		FER @ $10^{-5}$		$\mathcal{L}_{\text{avg}}$ ( $\mu\text{s}$ )
						$L$	$E_b/N_0$	$E_b/N_0$	$\mathcal{L}_{\text{avg}}$ ( $\mu\text{s}$ )	
1/4	64	11	0x385	5G	0.20	64	2.15 dB	2.53	3.35 dB	0.55
	128	12	0xF13	5G	0.28	64	1.60 dB	6.44	2.60 dB	1.07
	256	12	0xF13	5G	0.60	64	1.25 dB	10.58	2.25 dB	1.66
	512	12	0xF13	GA	1.01	32	1.10 dB	14.92	1.85 dB	3.53
1/2	64	7	0x65	5G	0.14	32	3.15 dB	0.70	4.60 dB	0.33
	128	12	0xF13	5G	0.21	64	2.55 dB	3.31	3.45 dB	0.69
	256	12	0xF13	5G	0.34	64	2.15 dB	6.55	3.10 dB	1.18
	512	16	0x8005	5G	0.68	64	1.90 dB	11.95	2.70 dB	2.12
4/5	64	8	0x9B	GA	0.15	32	5.05 dB	0.48	6.45 dB	0.16
	128	10	0x3D9	5G	0.20	32	4.40 dB	1.21	5.35 dB	0.41
	256	10	0x3D9	5G	0.34	32	4.10 dB	2.20	5.00 dB	0.67
	512	12	0xF13	5G	0.66	32	3.75 dB	4.92	4.55 dB	1.36

helped uncover “sweet spots” balancing latency and error-correction performance. An example of the results obtained for  $K = 128$  and  $N = 256$  is shown in Figure 1.

## V. PERFORMANCE RESULTS

*a) Testbed:* A Minisforum AtomMan X7 Ti PC (Intel Ultra 9 185H, 16 x86-64 cores with 6 p-cores @ 5.1 GHz (one core used), 8 e-cores @ 3.8 GHz (unused), and 2 LPe-cores (unused), 32 GB DDR5 @ 5600 MT/s) running Linux (Ubuntu 25.04 kernel 6.14, g++ 14.2.0) has been used.

*b) Results:* Table I summarizes the proposed Polar code configurations submitted for the contest, along with their measured performance metrics. The table provides details on the code rate, information block length  $K$ , CRC size and polynomial, code construction method, worst-case encoder latency, list size  $L$ , and decoder performance in terms of Frame Error Rate (FER) at  $10^{-3}$  and  $10^{-5}$  thresholds, together with corresponding average decoding latencies.

## VI. CONCLUSION

This work was conducted in the context of the ISTC 2025 low-latency software coding challenge, targeting high-

performance implementations of channel encoders and decoders for short blocklengths on general-purpose CPUs. We presented a complete open source toolchain based on Polar codes, including a bit-packed encoder and a fully unrolled ASCL decoder generator. Design space exploration revealed competitive configurations balancing latency and error performance. All implementations are available within the AFF3CT framework to foster reproducibility and further research.

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