Preliminary 2D elastoplastic modeling of gate cracking in SiC MOSFETs under short-circuit conditions across a wide temperature-range using rankine's damage energetic approach. (Selected – Extended Full Paper from ESREF'24)

Mustafa Shqair, Emmanuel Sarraute, Frédéric Richardeau

Preliminary 2D Elastoplastic Modeling of Gate Cracking in SiC MOSFETs Under Short-Circuit Conditions Across a Wide Temperature-Range Using Rankine's Damage Energetic Approach

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Mustafa Shqair*, Emmanuel Sarraute, Frédéric Richardeau

LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France

Abstract

For the first time in SiC MOSFETs, structural and physical modeling of the Intermediate-Layer-Dielectric (ILD) cracking in a planar gate under short-pulse short-circuit conditions is proposed. This approach employs an energy-based Rankine damage model, relying on the SiO_2 mechanical properties. The Rankine model has been effectively integrated into a comprehensive 2D electrothermal-metallurgical and elastoplastic-mechanical model across a wide range of temperatures. Initial results enable the extraction of crack penetration depth from a single pulse, paving the way for estimating the average number of critical cycles leading to a potentially complete destructive ILD fracture.

Keywords: SiC MOSFET; Short-Circuit (SC); High-Temperature; Gate-Crack Modeling; Damage Modeling; 2D Finite Elements Modeling; Elastoplastic Modeling.

1. Background, Methodology, and Targets

SiC MOSFET technology stands out among power devices for its high efficiency and high switching frequency, making it ideal for on-board power inverters. Short-circuit (SC) withstanding time (t_{scw}) and maximal number of cycles (N_{cycles}) are critical for achieving operational certifications. While substantial research has been focused on standard t_{scw} [1], N_{cycles} and SC life capabilities have received significantly less attention. To date, only classical, time-consuming and costly experimental approaches have been attempted [2]. There is also a lack of a comprehensive physical model that addresses Intermediate Layer Dielectric cracking (ILD), identified as the weak position in the gate region during short-pulse or medium-pulse periods in SiC MOSFETs [3]. To address this gap, this article presents, for the first time in SiC MOSFET, a novel preliminary approach based on a complete 2D structural and physical modeling of the ILD gate-corner damage. Modeling the crack of SiO_2-type ILD is challenging due to its rigid and brittle nature, as noted in [4] for GaN HEMT applications. This damage behavior is confirmed in SC experiments by the occurrence of a distinct abrupt failure mode, where cracks accumulate and lead to fracture damage. As a result, a permanent offset in gate leakage occurs after a threshold number of cycles (cycle #291), as illustrated in Fig.1 and Fig.2, signifying the initiation of soft crack formation.

The crack modeling in SiO_2-type ILD also requires accurate Finite Element Modeling (FEM) of local stress-strain distributions at gate positions with geometric singularities. The Cohesive Zone Modeling (CZM) approach was previously introduced and applied to analyze the crack formation and evolution at the topside wire-metallization contact, influenced by grain boundary reconstructions in Al that cause wire lifting-off [5,6]. While CZM is suitable for interfacial damage modeling, it may not be appropriate for cracking problems within an isotropic and homogeneous brittle material such as a SiO_2-ILD. Therefore, a new approach is proposed in this paper based on Rankine's model. This model allows calculating the progressive partial damage quantity that reflects the locations of effective local cracks in the SiO_2 material, typically near the ILD's corner during SC operation, based on an energy-based deformation model.

The paper is organized as follows: Section 2 provides an overview and an update of our previous Multiphysics modeling; Section 3 details the implementation of the Rankine sub-model in COMSOL Multiphysics software and its verification; finally, Section 4 presents the initial results of crack penetration at the ILD corner during a single short-pulse SC.

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
Corresponding author: mustafa.shqair@laplace.univ-tlse.fr
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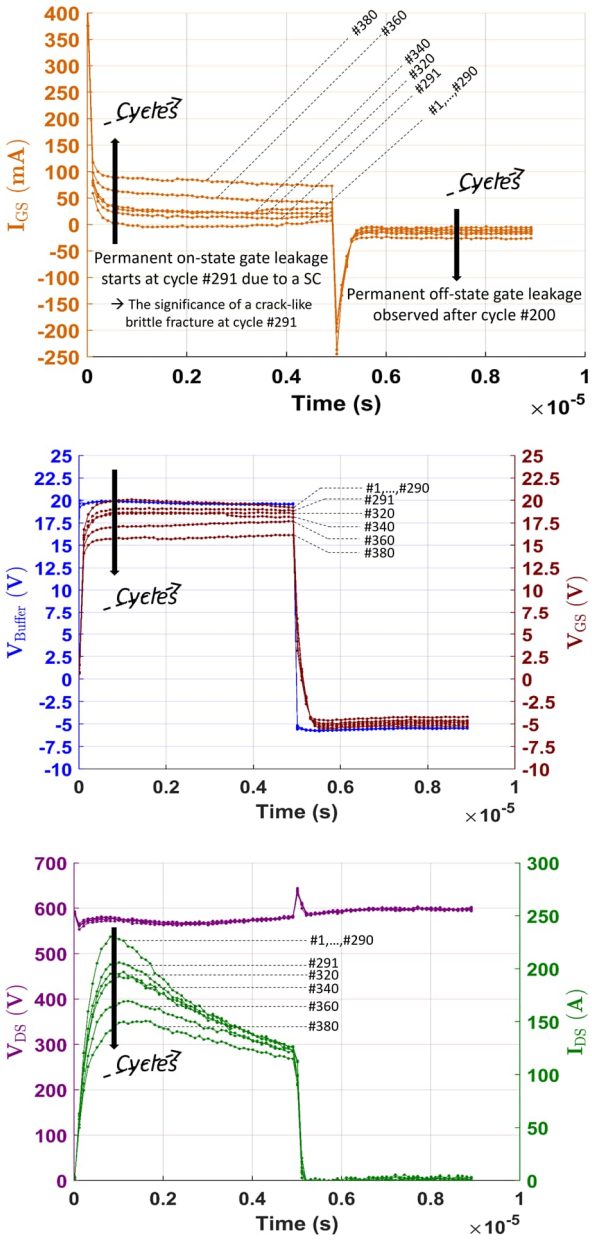

Fig.1 Transient waveforms during SC cycling of a 3-lead TO-247 package with a planar gate Gen. II device (80mΩ-1.2kV) under V_{DS}=600V, V_{Buffer}=$V_{GS\ init}$=20V, $R_{Gate(on/off)}$=47Ω, T_{case}=T_{Room}=25°C, t_{SC}=5µs, and t_{scw}=8µs from cycle #1 to the cycle #380

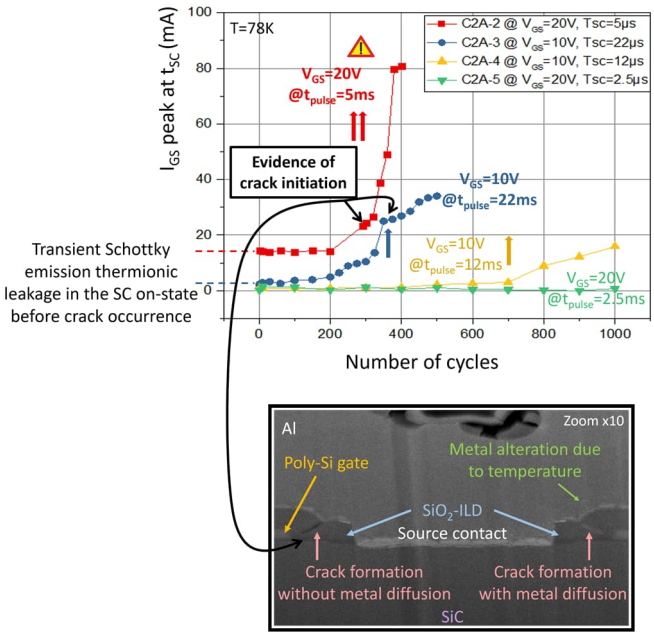

Fig.2 Parametric analysis of the maximum gate current (I_{GS} peak at t_{SC}) for V_{Buffer} (10V and 20V) and t_{SC} (2.5µs, 5µs, 12µs and 22µs), extracted at the end of each pulse. Up to cycle #200, the offset gate current is governed by transient Schottky emission thermionic leakage. An important permanent offset in gate leakage through the ILD corner appears at cycle #291, as shown in the SEM image, marking the onset of the first soft crack-like brittle fracture

2. Advanced Multiphysics Model for Wide-Range Temperature Dynamics in SiC MOSFETs during SC Operation

A static and transient electrothermal 2D model of 4H-SiC MOSFETs, including SiO_2-gate/SiC-channel fixed-charge and charge trapping/de-trapping effect, was previously developed by authors [7] using the semiconductor and heat transfer modules in COMSOL Multiphysics. The model accounted for the thermal dependency of the gate-source threshold voltage $V_{GS(th)}$, while an additional mobility coefficient to Arora's model refined the transient response under extreme SC conditions. This model enabled temperature extraction and oxide health monitoring, paving the way for studying metallurgical phase transitions and thermo-mechanical stress localization. The dimensions of the model are presented in Tab.1. Fig.3 depicts the initial 2D symmetric geometry of the half-cell device and the applied doping.

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
Corresponding author: mustafa.shqair@laplace.univ-tlse.fr
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Tab.1. Geometric dimensions [9]

t_{drift}	14µm	t_{ox}	50nm	t_{poly}	185nm
t_{ild}	416nm	t_{ti}	45nm	t_{al}	4µm
w_{drif}	8.7µm	w_{ox}	2µm	w_{poly}	1.77µm
w_{ild}	2.33µm	w_{al}	8.7µm		

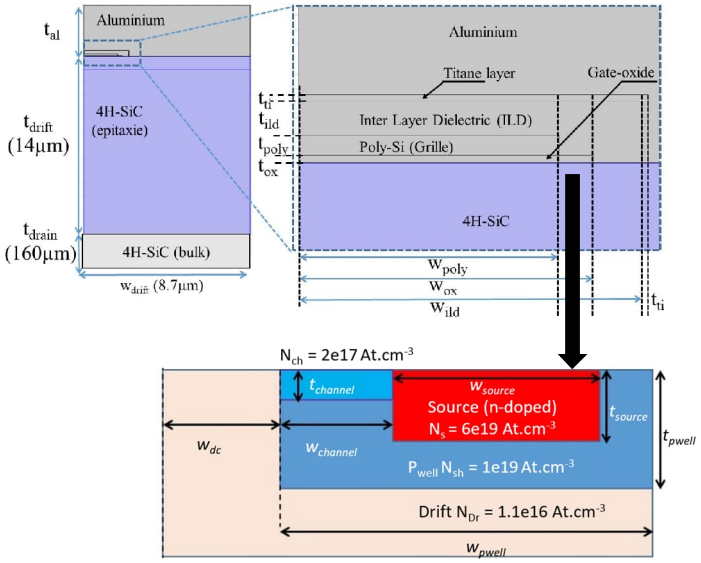

Fig.3 Parametric details of the modeled half-cell planar gate SiC MOSFET (1.2kV, 80mΩ, and an active area ≈ 6mm^2) [7,8]

The model was then extended to include dynamic Al source melting [8]. Compared to existing 1D models, it offers improved geometric accuracy and accounts for temperature-dependent electrothermal material properties of all involved materials, making the model particularly relevant for high temperatures in SCs and a valuable tool for understanding failure mechanisms. The main material properties considered are shown in Fig.4. In this study, the impact of Al phase change on current density, temperature evolution, and melting dynamics was highlighted. The critical time and energy to reach the melting temperature ($T_{melting}$) of Al were identified as well as highlighting the high thermal stress regions in the transistor. These insights can help optimize chip design and refine gate driver protection timing to prevent catastrophic failure. Fig.5 highlights the main SC simulation results based on channel-mobility fitting, an extension of Arora's model [7,8]. Fig.6 illustrates the progression of the melting process within the Al metallic source electrode.

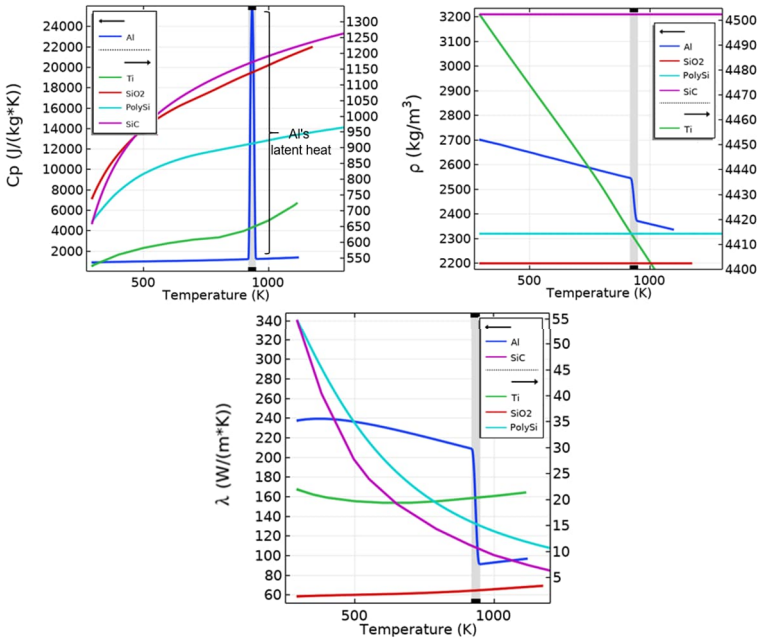

Fig.4 The evolution of heat capacity, thermal conductivity, and density as a function of temperature for aluminum (Al), silicon dioxide (SiO_2), titanium (Ti), silicon carbide (SiC), and polysilicon (poly-Si) [8]

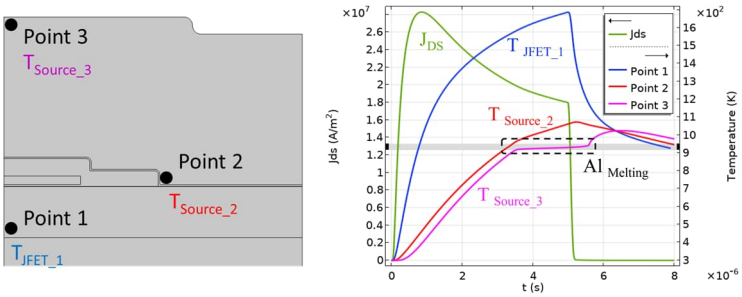

Fig.5 Thermal evolution in materials (Points 1, 2 and 3) resulting from the electrothermal simulation integrated with Al phase-change modeling for (V_{DS}=600V, V_{GS}=20V, and T_{CASE}=T_{ROOM}=25°C) [7,8]

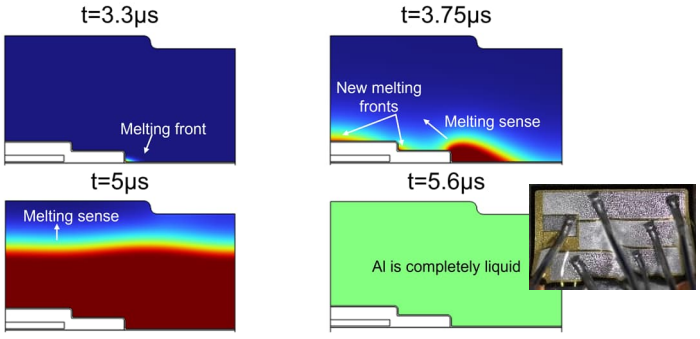

Fig.6 2D maps illustrating the dynamic visualization of the melting front and progression of Al over time. During the phase change, the blue zone indicates the solid phase, while the red zone represents the liquid phase [8]

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Starting here, the paper delves into its central focus by addressing thermomechanical modeling. The electrothermal model [8] was expanded to include thermomechanical simulations (using only linear elastic laws, without plasticity) to capture deformations across a broad temperature range within the ILD-Ti-Al region [10]. This updated model accounts for temperature-dependent mechanical properties, as shown in Fig.7. The modeling yielded promising preliminary results, indicating stress concentration near the ILD-Ti barrier, the same region where cracks are observed experimentally, as illustrated in Fig.8.

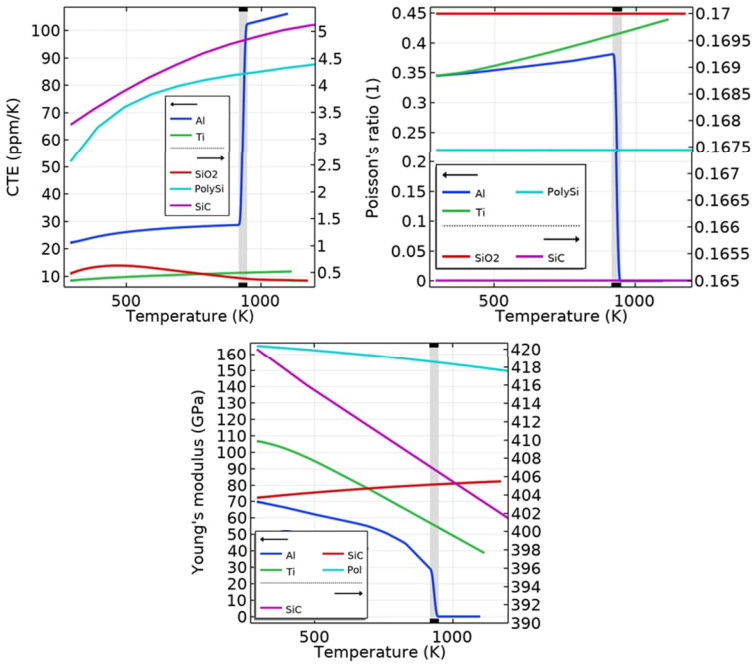

Fig.7 The evolution of CTE, Young's modulus, and poisson ratio as a function of temperature for aluminum (Al), silicon dioxide (SiO_2), titanium (Ti), silicon carbide (SiC), and polysilicon (poly-Si) [10]

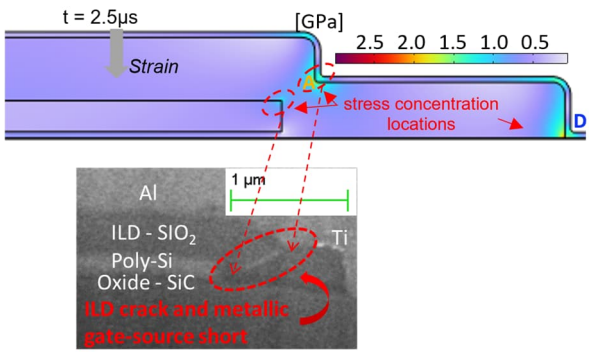

Fig.8 Surface stress distribution during SC operation near the ILD-Ti barrier, the same region where cracks form

However, the previous model did not account for the elastoplastic behavior of the thick Al-source layer and the Ti barrier surrounding the ILD, especially since large thermal stresses and strains are likely to occur under high-amplitude SC conditions. To achieve a more accurate model and precisely predict the crack-path progression, new deformation laws for Ti and Al were proposed. Extensive literature research enabled the extension of a previously published model, now including elastoplastic stress-strain laws for Al and Ti as defined in Fig.9 [11].

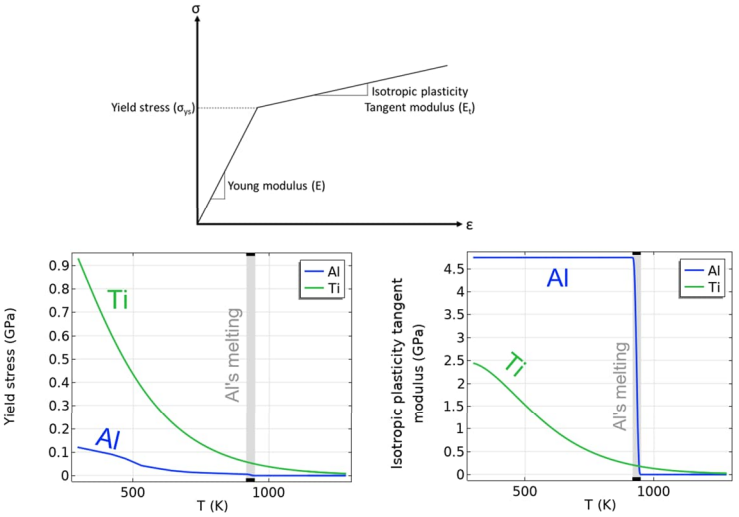

Fig.9 Temperature-dependent bilinear kinematic elastoplastic behavior of the Ti barrier around the SiO_2-ILD region and the thick Al-source layer [12-14]

So, a bilinear kinematic elastoplastic model is used for Al and Ti. The parameters of such an elastoplastic law are Young's modulus (E), representing the initial linear elastic behavior as shown in Fig.7; the isotropic plasticity tangent modulus (E_t), reflecting the subsequent plastic behavior; and the yield stress (σ_{ys}), which is the stress threshold separating the two behaviors.

As one can see in Fig.9, it is crucial to consider the wide temperature range dependency of these parameters, particularly up to $T_{melting}$ of Al. The newly introduced material laws for both Al and Ti exhibit high-temperature sensitivity (except for the E_t of Al). Notably, Ti exhibits significantly greater sensitivity than Al, especially at temperatures below the $T_{melting}$ of Al [300K-600K].

Compared to earlier models, this model offered significant improvements, with plasticity limiting the stress field in the gate region. A key outcome of this model was its ability to track the chronological

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
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evolution of thermal and mechanical stresses in the gate region during an SC. Specific points of interest in the geometry were selected for analysis, focusing on thermal and mechanical aspects. Thermal points include the first and last melted positions in Al, while mechanical points correspond to the ILD-Ti-Al edge region, where crack formation is expected. The temperature and stress evolution were tracked at these points. The selected positions, shown in Fig.10, are as follows: A in the SiO_2 domain, B in the Ti domain, and C, D, and E in the Al domain. This enabled the extraction of more precise critical time values for the initiation of the two primary degradation forms discussed: Al melting, based on the thermal modeling, and SiO_2 cracking, based on the elastoplastic modeling (Fig.10). This model confirmed the stress concentration near the ILD-Ti-Al barrier (Fig.11), which had been observed in the previous model (Fig.8).

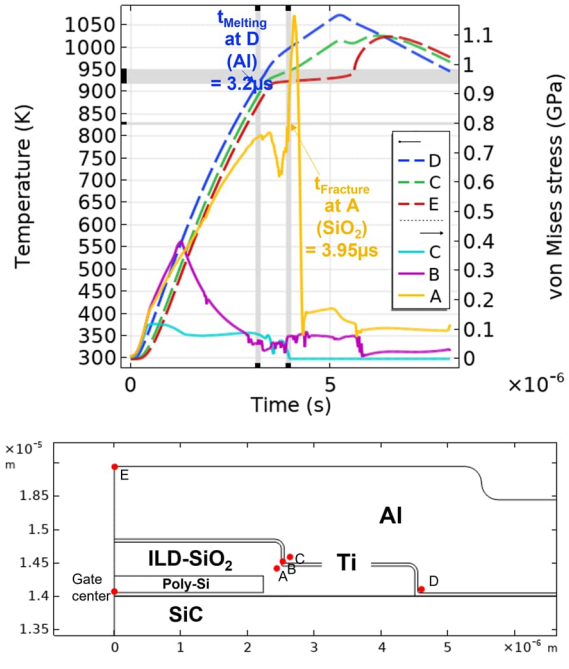

Fig.10 Temperature and stress evolutions at critical points in the geometry, at which Al melting begins and cracks are expected to initiate, are shown in the thermomechanical (elastoplastic) simulation under SC operation conditions (V_{DS}=600V, V_{GS}=20V, T_{CASE}=25°C)

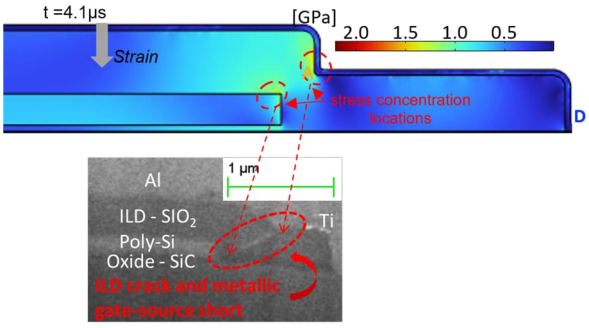

Fig.11 2D stress distribution in the transient elastoplastic thermomechanical simulation with temperature-dependent material laws

Starting from the fact that this modeling provides valuable insights for designers to optimize gate-driver protection and enhance device robustness, such as refining chip design and protection timing to prevent catastrophic failure, the SiO_2-ILD damage model was introduced. This approach helps validate the model by observing the damage evolution and comparing the modeled damage location with experimental observations. Additionally, it can be used in future studies to predict the number of cycles required for a complete crack along the ILD-Poly-Si region through repeated mechanical cycles. Given the brittle nature of the damage, the Rankine model was adopted to predict damage evolution. The next section describes the model's implementation.

3. Description and Implementation of Rankine's Damage Model in COMSOL Multiphysics for Predicting Fracture in the Gate Region

The foundation of Rankine's theory for modeling damage in brittle materials such as SiO_2 at the gate region is illustrated in Fig.12 [15, 16]. The mechanical behavior is physically and locally modeled using a stress (σ) - crack opening displacement (δ) law. Rankine's theory proposes an energetic criterion called the fracture energy (G_f), which represents the energy density of the material up to fracture. The fracture stress (σ_f) indicates the maximum stress the material can sustain before fracturing [17]. In Fig.12, state "1" corresponds to reversible elastic deformations, reflecting the material's stiffness. Upon reaching σ_f, state "2" begins, marked by irreversible deformations ($\delta>\delta_s$), resulting in a sharp stress reduction in the softening region. State "3" is attained when δ reaches δ_f, indicating the formation of a crack. The proportional damage variable (D) indicates the damage status: D=0% for $\sigma\leq\sigma_f$ and $\delta\leq\delta_s$, whereas D=100% for σ=0 and $\delta=\delta_f$. Rankine's law is defined as shown in Equation (1):

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
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$$G_f = \frac{\sigma_f . \delta_f}{2} \quad (1)$$

Where G_f=4.5J/m^2 for SiO_2 [18], σ_f=0.8GPa for SiO_2 [19, 20], and δ_f is derived from G_f and σ_f [16, 17]. Assuming linear softening in the "2" interval, the crack opening displacement (δ_f) for SiO_2 measures 11.25nm. This value is crucial for determining the appropriate mesh size in the SiO_2-ILD region during damage modeling.

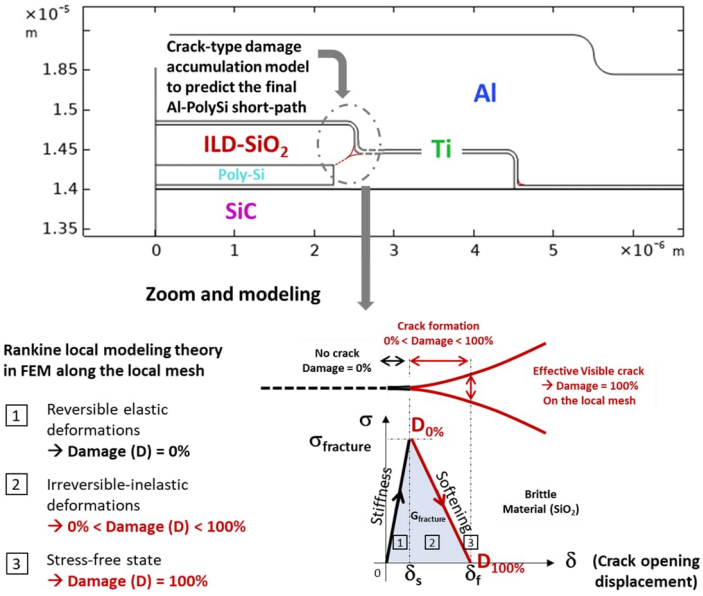

Fig.12 Rankine's theory is employed to model the formation and evolution of corner cracks in SiO_2-ILD. This includes an introduction to local damage initiation (D<100%) and complete damage formation (D=100%), defined by $D(\delta)=(\delta_f/\delta).(\delta-\delta_s)/(\delta_f-\delta_s)$ [17]

Fig.13 illustrates an extended representation of possible Rankine cycle modes, ranging from the simplest (Fig.13a) to the most advanced (Fig.13c) model, accounting for the permanent fatigue effect by maintaining the damage factor (D) across cycles. Since only the model shown in Fig.13a is implemented and parametrized in COMSOL Multiphysics software, this Rankine cycle mode was adopted in this paper to investigate the SiO_2-ILD damage.

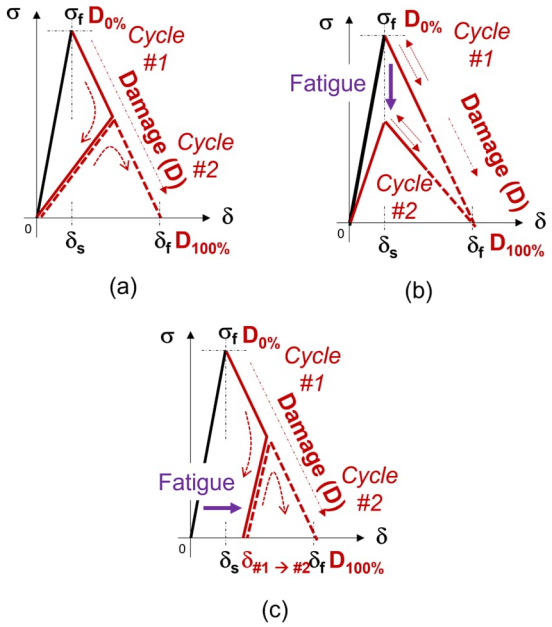

Fig.13 Summary of possible Rankine cycle modes derived from [16]: (a) basic fatigue modeling, (b) fatigue modeling based on σ(δ) softening within cycling, and (c) fatigue modeling that considers changes in δ_s within cycling

Fig.14 validates the proposed Rankine model using a simple case within COMSOL Multiphysics involving a virtual brittle material subjected to two cyclic loadings. This figure demonstrates that the implemented model reveals a more physically realistic exponential stress-displacement behavior in the softening-unloading interval "2", as defined in Equation (2). Equation (3) provides the expression for the global energy G_f (covering intervals "1" and "2"). Equation (4) shows the formula for the analytical damage progression D_δ. The parameters described in these equations are clearly illustrated in Fig.13. These relationships, available in COMSOL Multiphysics [17], are considered when modeling SiO_2 damage in SiC MOSFET and will be detailed in the following section.

$$\sigma = \sigma_f \, e^{-\frac{\delta-\delta_s}{\delta_f-\delta_s}} \quad (2)$$

$$G_f = \sigma_f \left(\delta_f - \frac{\delta_s}{2}\right) \quad (3)$$

$$D_\delta = 1 - \frac{\delta_s}{\delta} e^{-\frac{\delta-\delta_s}{\delta_f-\delta_s}} \quad (4)$$

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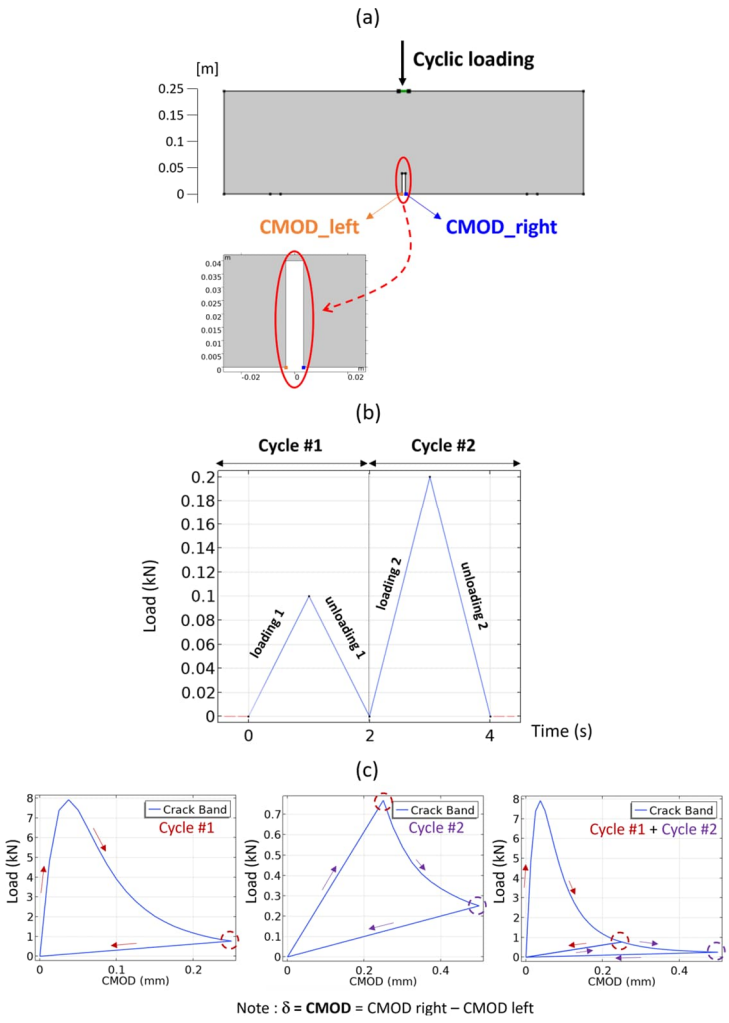

Fig.14 Rankine's model validation in COMSOL Multiphysics when considered in the (a) notched beam model [21] while applying (b) a temporal cyclic loading definition. The results in (c) show the load vs crack opening mouth displacement (CMOD) progress in the first and second cycle sequences. The material properties in this model are assigned as follows: (G_f=85J/m^2, σ_f=3.9MPa, E=37GPa, ν=0.21 and ρ=2400 kg/m^3)

4. Analysis of Initial Results: Crack Penetration Path, Critical Times & Energies, and Cycle Endurance Capability

Rankine's model, introduced in the previous section (Fig.12) and validated in its physical form (Fig.14), is now implemented for the SiO_2-ILD material within the comprehensive 2D Multiphysics SiC MOSFET model described in Section 2. As a reminder, the damage parameters introduced for the SiO_2 domain are G_f=4.5J/m^2 for SiO_2 [18] and σ_f=0.8GPa [19, 20].

This model offers several advantages over our previous ones [10,11]. In our prior mechanical models, a point near the ILD-Ti corner was selected to estimate the time required to reach the fracture stress, thereby predicting the critical time for crack initiation. However, the current model provides a 2D visualization of damage evolution over time. This allows us to track crack progression and validate that the damage location matches experimental observations, confirming that failure occurs in regions of maximum stress, as shown in Fig.8 and Fig.11. Additionally, this serves as the foundation for our future work, which involves applying repetitive mechanical cycles to analyze damage progression. It may also pave the way for developing a predictive law to estimate the number of cycles required for a complete crack along the ILD-Poly-Si region.

Consistent with our previous models, specific points of interest in the geometry were selected for analysis, including thermal points (first and last melted positions in Al) and mechanical points (ILD-Ti-Al edge region at which the crack is expected). Temperature and stress evolution were traced at these points, and the resulting damage was interpreted. The selected points are the same as those shown in Fig.10, with an additional point, A2, illustrated in Fig.15.

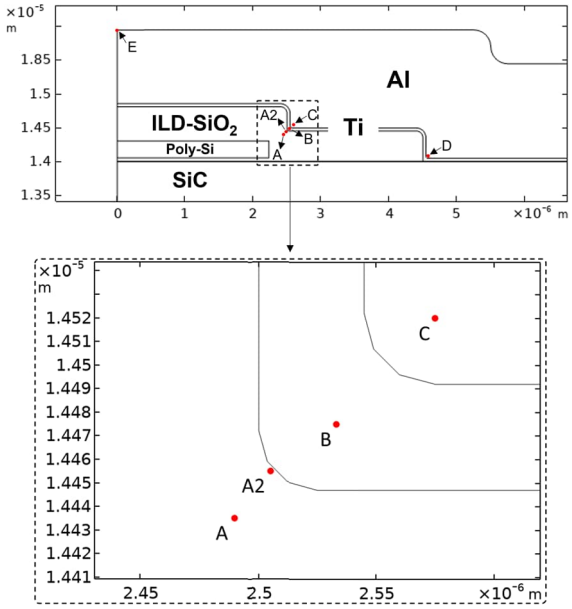

Fig.15 Selected points for analyzing stress, temperature, and damage evolution (Compared to Fig.10, an additional point A2 inside SiO_2 has been added for this analysis)

The damage model was validated at point A2 within the SiO_2 domain by plotting the first principal stress (σ_1) and the damage parameter (d), as shown in Fig.16. Once the σ_f was reached, the damage

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
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parameter began to increase, indicating the onset of damage.

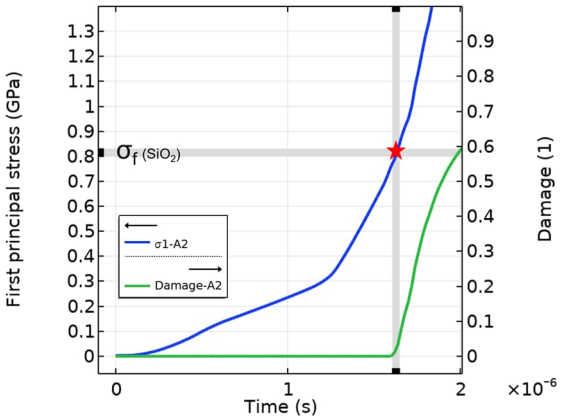

Fig.16 Validation of the damage model at point A2 in the SiO_2 domain: Damage parameter increase upon reaching σ_f

A topside-constrained surface above the Al metallization is used as a boundary condition, reflecting the presence of a thermal-resistant epoxy resin, along with polyimide and silicon nitride layers, compensating for their absence in the model. According to Equation (4), the simulations use deformation-adaptive meshing, which adjusts based on the progression of displacement and damage at the SiO_2-ILD corner. An overview of the new results is presented in Fig.17, similar to our previous models [10,11], where both von Mises stress and temperature are plotted versus time. This time, the evolution of σ_1 is also displayed, as the model now incorporates the Rankine criterion. Fig.18 shows the progression of damage over time.

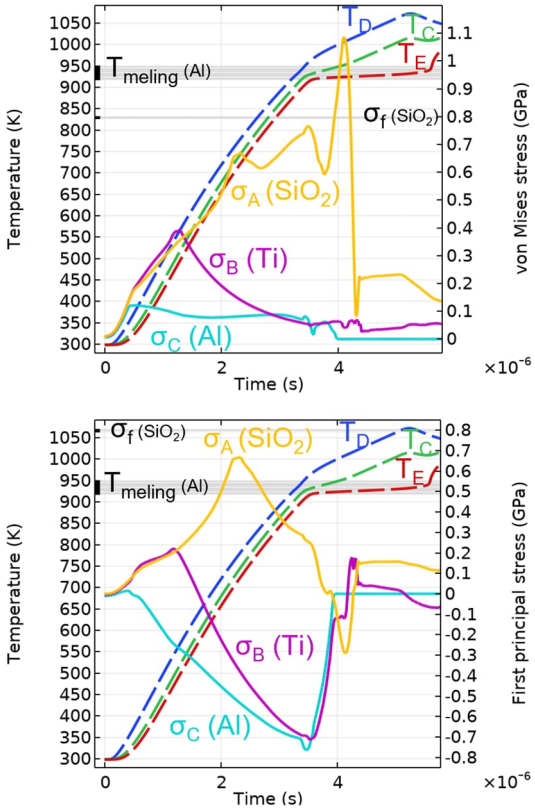

Fig.17 Temperature and stress evolutions at critical points in the geometry, at which Al melting begins and cracks are expected to initiate, are shown in the thermomechanical (elastoplastic) simulation under SC operation conditions (V_{DS}=600V, V_{GS}=20V, T_{CASE}=25°C). This simulation incorporates the SiO_2-ILD crack damage modelling based on Rankine's theory (G_f=4.5J/m² and σ_f=0.8GPa)

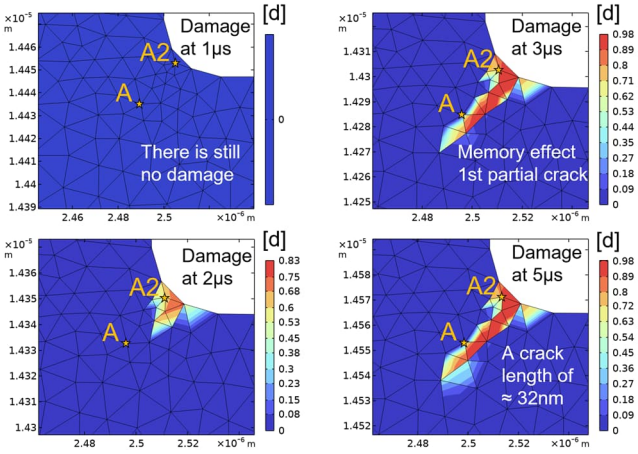

Fig.18 2D damage maps plotted in the SiO_2-ILD domain, based on Rankine's theory (G_f=4.5J/m² and σ_f=0.8GPa). Mesh size range: For SiO_2, 8nm<$Size_{Mesh}$<30nm and for Ti, 5nm< $Size_{Mesh}$<15nm. The crack opening displacement is approximately 10nm, as calculated by Equation (3)

M. Shqair, E. Sarraute, F. Richardeau - LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France.
Corresponding author: mustafa.shqair@laplace.univ-tlse.fr
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The stress evolution depicted in Fig.17 closely aligns with that in Fig.10. According to the 2D damage maps shown in Fig.18, the initial damage becomes clearly visible at approximately 3µs, which corresponds to 37.5% of t_{scw}. The critical time for the initiation of Al melting is 3.2 µs, based on thermal results [8], when the temperature at point D reaches the Al melting temperature. This critical time corresponds to 40% of t_{scw}, as shown in Fig. 17.

Experimentally, the critical energy values at which the initial damage in the SiO_2-ILD region becomes apparent and Al melting begins are calculated using Equation (5). Since the moments of Al melting and the initial damage occurrence are approximately simultaneous (3.2µs and 3µs respectively), the energy value at the initiation of both phenomena is around 4.46J/cm^2.

$$E_{SC} = V_{DS} \int J_{SC_{channel}}(t).dt \quad (5)$$

Based on Fig.18, when examining point A2 situated at the ILD-Ti interface, no damage is present for t<2µs because $\sigma_1<\sigma_f$, as shown in Fig.16. However, at t=2µs, when σ_1 in the vicinity of point A2 reaches σ_f, a crack clearly propagates through point A2, governed by the damage equations (Equations 2-4). Notably, the damage mapping reveals a visible crack opening displacement, consistent with the prediction based on Equation (3). Beyond t>5µs, the shape of the cracking stabilizes due to stress collapse caused by the melting of the Al layer. The results in Fig.18 show a concentration of damage (D=100%) at the ILD-Ti corner region, near points A and A2, where maximal stresses are concentrated along a quasi-linear preferred damage pathway, aligning with the cross-sectional SEM analysis shown in Fig.2.

In this simulation when considering a topside-constrained boundary condition at the upper part of the Al layer, a total crack depth of 32nm is resulted. This value must be related to the straight-line distance between the corners of the SiO_2-ILD and poly-Si gate (315nm), representing 10% of the total crack length. Assuming the hypothesis of linear accumulation of damage is accepted as with Miner's rule, in that case, the critical number of cycles required to crack the entire distance between the corners of SiO_2-ILD and the poly-Si gate will be 315/32≅10 cycles. However, this estimation is clearly the simplest, with maximum yielding damage imposed by the choice of the topside-constrained boundary condition. Certainly, a higher number of cycles is required for complete crack formation, allowing the Al-source metal to penetrate through the SiO_2 material, as observed in Fig.2. This will be discussed more thoroughly in our upcoming works.

5. Conclusion and Future Work

A new extended 2D Multiphysics model for SiC MOSFETs, incorporating Rankine's damage theory applied to the SiO_2-ILD layer under harsh SC operation has been introduced, implemented, and analyzed. The simulated damage localization and crack-path direction align with the transient 2D stress maps and the SEM cross-sections. The critical time and energy for crack formation in SC operations can also be determined, revealing that a margin of at least 37.5% below the t_{scw} must be maintained to prevent the initiation of SiO_2-ILD cracks and Al melting. *Future research will focus on exploring the impact of varying topside boundary conditions and investigating in detail the effect of pulse duration on damage progress. Additionally, the next phase will involve subjecting the system to repetitive mechanical cycles to gain deeper insights into damage evolution, potentially leading to the estimation of the critical cycle range for complete ILD fracture.*

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