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Giovani Crasby Britton Orozco, Salvador Mir, Estelle Lauga-Larroze, Benjamin Dormieu, José Lugo-Alvarez, et al.. 28 nm FD-SOI 4 K RF LNA design using DC transistor characterization measurements. LATS 2025 - IEEE 26th Latin American Test Symposium, Mar 2025, San Andres, Colombia. ⟨10.1109/LATS65346.2025.10963946⟩. ⟨hal-05042856⟩

HAL Id: hal-05042856

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28 nm FD-SOI 4 K RF LNA design using DC transistor characterization measurements

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***Abstract*—The design of cryogenic silicon circuits has gained much importance in recent years, in particular for applications such as quantum computers that require interface electronics with ultra-low levels of power consumption at temperatures as low as 4 K. The design of these circuits is complicated due to the lack of standard design kits for their simulation at these temperatures. Alternative approaches to avoid costly design and fabrication cycles are possible, in particular the use of Look-Up-Table (LUT)-based techniques that exploit the characterization of components at cryogenic temperature. In this paper, we illustrate this approach for the design of an RF Low Noise Amplifier (LNA) using a 28 nm FD-SOI technology that has been characterized at cryogenic temperatures.**

***Index Terms*—Cryo-CMOS, LNA, Qubit, Look-Up Table, Fano factor.**

I. Introduction

Cryogenic low-noise amplification originates in the need of radio astronomy and space exploration for the detection of the radio waves emitted by celestial objects [1]. Recently, a growing interest in quantum computers has boosted the research into cryogenic circuits [2] that must be sized considering power, gain and noise trade-offs. Current efforts are aimed at using silicon technologies, granting the possibility of large scale qubit integration and energy efficient systems [3]. FD-SOI is a promising CMOS technology with a demonstrated improvement in RF performance for silicon cryogenic circuits. In addition, it allows the possibility to counteract the increase of the threshold voltage for diminishing temperatures using the back-gate node, mitigating many of the cryogenic negative effects [4]. A current difficulty for the design of cryogenic circuits lies in the lack of design kits working at these temperatures. In this paper, we propose a LUT-based design environment running in Matlab that uses 4 K characterization measurements of a 28 nm FD-SOI technology to overcome the lack of a design kit [5]. A 4 K RF LNA is designed. The LUT-based approach is also demonstrated at room temperature and compared with standard circuit simulation. Ultimately, screening tests for fabricated LNAs defined by means of the LUTs can be performed at room temperature before validation at cryogenic conditions. Section II describes the characterization of the 28 nm FD-SOI technology from room to cryogenic temperatures. Section III briefly introduces the procedure for the construction of the LUT and the design approach. Section IV shows the use of the LUT environment for sizing a cascode LNA at 4 K using the DC measurements in the LUT. Finally, Section V validates the approach and describes the performances of the LNA at room temperature for a screening test, before giving some conclusions.

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II. Transistor temperature characterization

The LUT-based design approach requires the characterization of the transistor and passive components of the technology at cryogenic temperature. The temperature profile of characteristic parameters is extracted and stored in the LUT. In this Section, we illustrate the characterization of 28 nm FD-SOI transistors. The measurement setup consists of a Lakeshore CPX prober for placing the dies and operating the temperature regulation, a device analyzer B1500 for DC bias from Agilent Technologies and a PNA-X for RF measurements from Keysight Technologies. The measurements were conducted from 300 K to 4 K on a thin oxide transistor of L=28 nm and W=18 $\mu\mathrm{m}$, biased with V_{ds}=0.5 V, and a back-gate bias at 0 V. The LUT-tool emphasizes on the relationship between the DC small-signal parameters and the normalized g_m/I_d, a figure of merit that is used for amplifier design [6] and that is roughly temperature independent. We characterize next the most important transistor parameters that are required for high-frequency amplifier design at low temperatures.

A. Subthreshold swing and slope factor

The DC $\log(I_d)$-V_{gs} characteristic of the transistor varies with temperature as shown in Fig. 1. This characteristic serves for inferring the electrical behavior of the device and for modeling purposes, giving the necessary information of how the temperature profile of the technology will affect analog design. For values below room temperature, the efficiency of the device improves. This is seen in weak inversion regime where the steepness of the I-V characteristic is increased, implying a higher increase in current for the same voltage change when compared to room temperature [4]. However, the values of the I-V curve are almost identical below a certain critical

temperature T_c. This critical temperature usually occurs at around 46 K for advanced technologies [7].

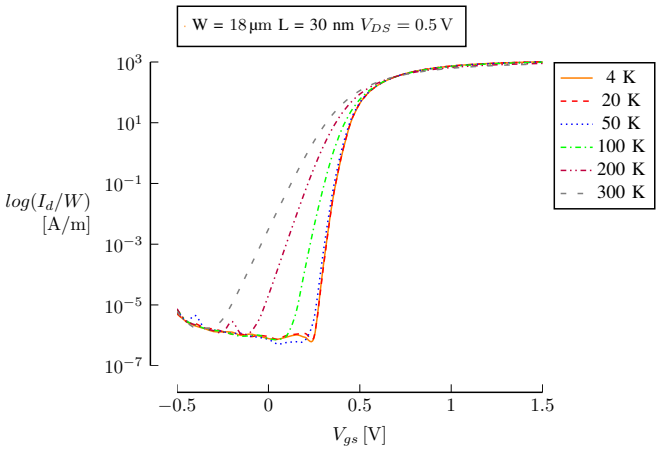

Figure 1: Measured $log(I_d)$ versus V_{gs} from room temperature to 4 K of the 28 nm FD-SOI technology.

The saturation of this temperature effect is better visualized in Fig. 2 using the Sub-threshold Swing (SS), a parameter that evaluates the slope $dV_{gs}/dlogI_d$ of the characteristic in its linear part. The theoretical limit of the subthreshold swing is given by the Boltzmann limit $ln(10)U_T$ [8], where $U_T = KT/q$ is the thermal voltage, with K the Boltzmann constant and q the elementary charge. The Boltzmann limit at 4 K would give a slope of 0.8 mV/dec, instead of the measured subthreshold swing of 23.6 mV/dec in Fig. 2 for the 28 nm FD-SOI technology. This difference is attributed to the imperfections in the channel leading to an overlapping of the conduction band into the bandgap [7]. The SS excess impacts the power consumption as temperature scales down, and is modeled by the slope factor given by

$$n = \frac{SS(T)}{U_T ln(10)} \tag{1}$$

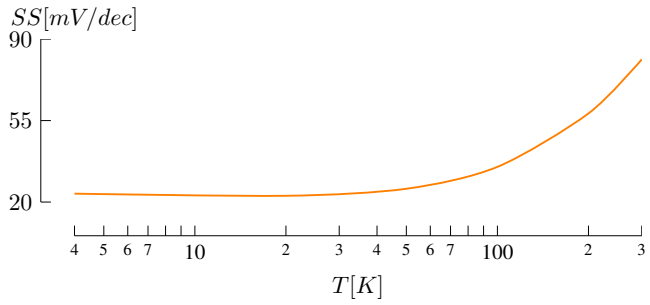

Figure 2: Measured subthreshold swing of the 28 nm FD-SOI technology from room temperature to 4 K.

The transconductance of the transistor $g_m = \partial I_d/\partial V_{gs}$ for a fixed V_{ds} is shown in Fig. 3. It increases for diminishing temperature, reaching also a saturation point for the same critical temperature Tc. The increase in g_m results in transistors with higher gain and power efficiency, and cryogenic conditions are optimal for amplifier performance.

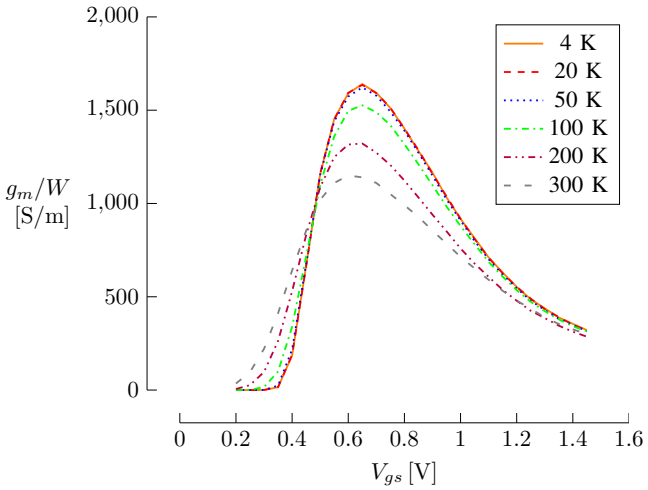

Figure 3: Measured transconductance g_m of the 28 nm FD-SOI technology from room temperature to 4 K.

B. Threshold voltage

Devices with low threshold voltage V_{th} are preferred given their improved performance for high frequency applications and lower power consumption. However, as the temperature of the transistor is decreased its threshold voltage increases (Fig. 4). The increase in V_{th} limits many of the electrical improvements of the transistor at low temperatures. The V_{th} increase is attributed to the temperature dependency of the interface-trap occupations and, to a lesser degree, incomplete ionization [9].

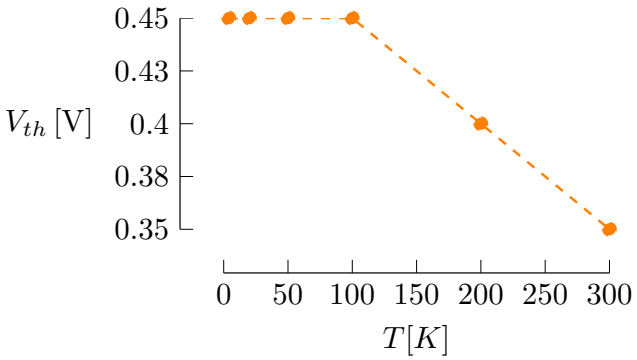

Figure 4: Measured threshold voltage V_{th} of the 28 nm FD-SOI technology from room temperature to 4 K.

When temperature decreases, while the bias conditions are kept as at room temperature, the overdrive voltage of the transistor reduces due to the increase in V_{th}. The drain to source current also reduces as shown in Fig. 5 since it is directly dependent on the overdrive voltage. Thus, for keeping a similar bias condition as at room temperature with the transistor in the same operation region, the value of V_{gs}

should be increased proportionally to the change of V_{th} with temperature. Fortunately, FD-SOI technologies have the additional advantage of the back-gate biasing, counteracting the increase of V_{th}, and as a consequence optimizing power consumption.

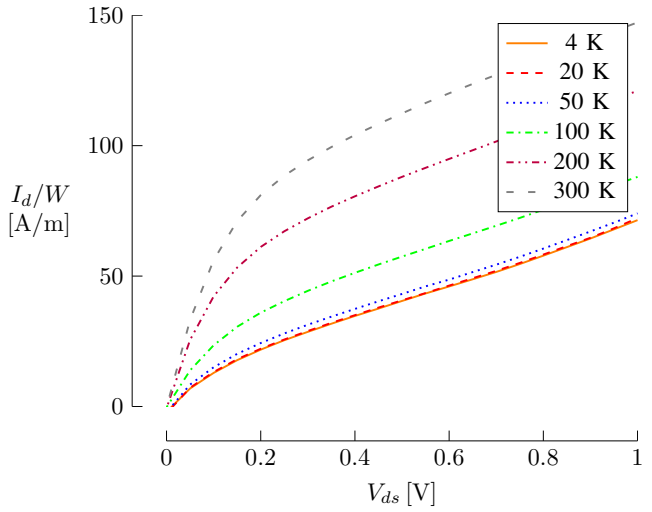

Figure 5: Measured I_d versus V_{ds} of the 28 nm FD-SOI technology from room temperature to 4 K for V_{gs}=0.5 V.

C. Normalized transconductance efficiency

For cryogenic design we consider the normalized g_m/I_d, a figure of merit that is roughly independent of temperature [7] and that can be used to determine the required biasing and sizing of a transistor at any temperature. The normalized g_m/I_d is obtained by dividing the nominal g_m/I_d over its theoretical maximum value (similarly as done for the SS), which gives

$$\left.\frac{g_m}{I_d}\right|_{norm} = n_{eq}U_T \cdot \frac{g_m}{I_d} \tag{2}$$

where n_{eq} is the equivalent slope factor. This factor captures the temperature changes of the transistor as shown in Fig. 6. Using a normalized g_m/I_d design approach it is possible to consider temperature independent design figures of merit, which can be later denormalized using the term $n_{eq}U_T$ for the sizing and bias at any temperature.

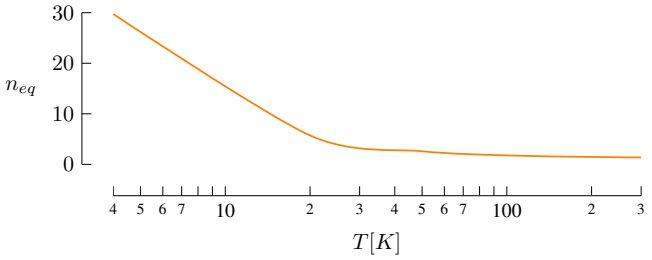

Figure 6: Measurement of the equivalent slope factor n_{eq} versus temperature of the 28 nm FD-SOI technology.

D. Parasitic capacitances

With respect to the transistor parasitic capacitances, their temperature dependency varies with the region of operation of the transistor. Considering the total gate capacitance C_{gg} when biased at weak and moderate inversion, its value changes due to the freezout of the dopants in the back gate N/P-well, increasing the backgate N-well resistance and ultimately the capacitors value [10]. Yet, when the transistor is biased at strong inversion, the value of C_{gg} remains almost constant with temperature as shown in Fig. 7.

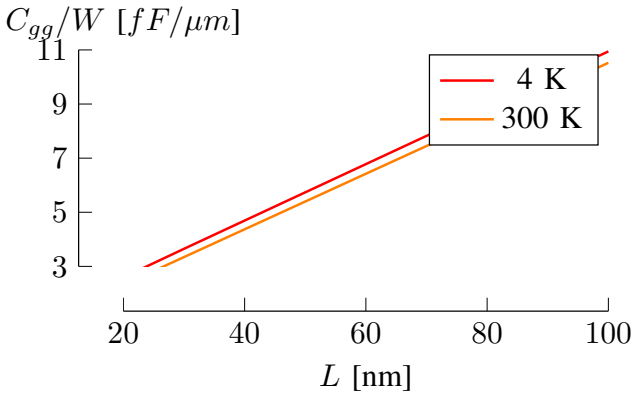

Figure 7: Measured total gate capacitance C_{gg} at 300 K and 4 K for the 28 nm FD-SOI technology at strong inversion (V_{gs} = 1 V, V_{ds} = 0.5 V) versus length.

For practical purposes, and as a first approximation in the case when there are no available cryogenic measurements of the transistor capacitor values, the transistor parasitic capacitances can be assumed equal to the values obtained at room temperature.

E. Noise and the Fano factor

In the standard transistor white noise model, the two major noise sources are the gate ($\overline{v_{ng}^2}$) and channel ($\overline{i_{nd}^2}$) noises. They are modeled as thermal noise as shown in Fig. 8. We neglect noise sources due to drain and source resistances since these are much smaller, and 1/f noise for high frequency design.

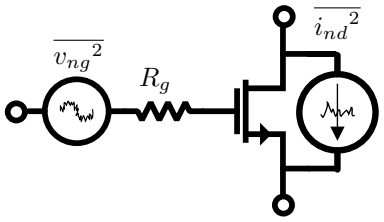

Figure 8: Transistor noise sources.

Recent works have shown that the standard noise model overestimates the noise improvement seen at cryogenic temperatures. This is due to the channel noise estimation since the shot noise, which basically depends on the bias condition of the transistor ($\overline{i_{nds}^2} = 2qI_d\Delta f$), does not scale with

temperature as thermal noise does [11]. The gate thermal noise ($\overline{v_{ng}}^2 = 4kT\Delta f R_g$) decreases linearly with temperature until 50 K, remaining constant or with a slight increase for values below. These temperature effects are attributed to the mobility increase of charges and the carrier freezout [12]. In the case of the 28 nm FD-SOI, we thus assume a linear decrease for R_g until 50 K, extrapolating the values from the compact model in the standard temperature range. For temperatures below 50 K, the value of R_g is assumed constant (Fig. 9).

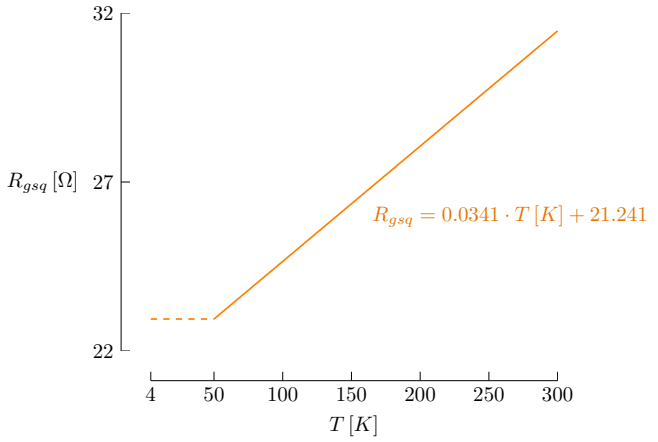

Figure 9: Temperature profile for the resistivity per area of one gate finger for the 28 nm FD-SOI node extracted from an extrapolation of the compact model.

The modeling of the channel white noise using the Fano factor F_a is useful to consider the temperature dependency. The channel white noise is represented as

$$\overline{i_{nd}}^2 = 2qI_d\Delta f F_a \tag{3}$$

where q is the elementary charge, I_d the drain current and Δf is the bandwidth in which the noise is integrated. The Fano factor takes values in the range]0,1[and expresses the suppression of shot noise [13]. The Fano factor can be written in terms of the normalized g_m/I_d as

$$F_a = \frac{2\gamma_n}{n_{eq}} \cdot \frac{g_m}{I_d}\bigg|_{norm} \tag{4}$$

where γ_n is the excess noise factor. It turns out that $\frac{2\gamma_n}{n_{eq}}$ is roughly constant with temperature, and thus the Fano factor is independent of temperature. There is then a linear dependency between the Fano factor and the normalized g_m/I_d. Fig. 10 shows the Fano factor versus the normalized g_m/I_d for different temperatures in the standard range simulated with a compact model. For a given normalized $\frac{g_m}{I_d}$, the Fano factor only varies slightly for this large temperature range.

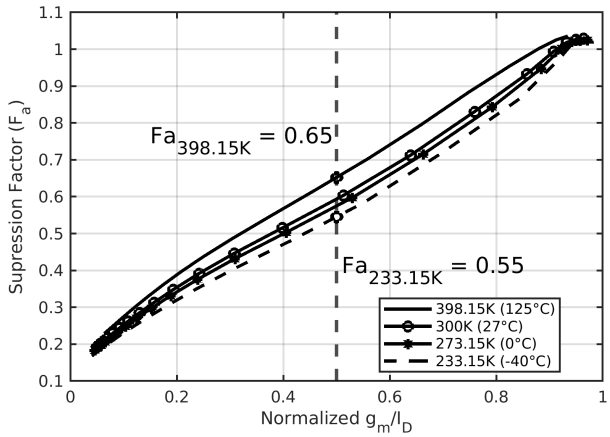

Figure 10: Compact model simulation of the Fano factor F_a versus normalized $\frac{G_m}{I_D}$ for different temperatures in the standard range.

Using this transistor white noise model, it is then straigthforward to obtain the noise parameters of a transistor in a given configuration. For example, the noise parameters of a common source transistor are given by [2]

$$F_{min} = 1 + \frac{I_d F_a}{U_{T_o}}\left(\frac{f}{f_t}\right)^2 R_g + \frac{f}{f_t}\sqrt{\left(\frac{I_d F_a}{U_{T_o}}\right)^2\left(\frac{f}{f_t}\right)^2 R_g^2 + 2R_g\frac{I_d F_a}{U_{T_o}}\frac{T}{T_o}} \tag{5}$$

$$Z_{sopt} = \sqrt{R_g^2 + 2R_g\left(\frac{f_t}{f}\right)^2\frac{U_T}{I_d F_a}} + \frac{j}{\omega C_{gg}} \tag{6}$$

$$G'_n = \frac{I_d F_a}{2U_{T_o}}\left(\frac{f}{f_t}\right)^2 \tag{7}$$

where f is the working frequency, f_t the transit frequency, T_o the reference temperature for noise figure measurement, T the operating temperature in Kelvin and U_{T_o} the thermal voltage at the reference temperature T_o. Using the *noise impedance formalism*, the noise factor F is given by $F = F_{min} + \frac{G'_n}{R_s}|Z_s - Z_{sopt}|^2$).

Noise measurements at 4 K have been conducted on a single 28 nm FD-SOI LVT transistor with L=30 nm, W=20 µm, and a frequency range from 500 MHz to 26 GHz. Figure 11 shows the NF values measured and compared with the calculated one for a transistor biased at $V_{gs} = 1\,\mathrm{V}$, $V_{ds} = 0.5\,\mathrm{V}$ and $V_{sb} = 0\,\mathrm{V}$. These results show that the Fano factor can predict the noise figure of a transistor at 4 K, and this is valid for all temperatures. Considering the steadiness of the channel noise at deep cryogenic temperatures, and the saturation of transistor gate noise, subthreshold swing and transconductance around 46 K, it could be argued that an RF amplifier could be designed at 46 K without significant performance degradation when compared to a 4 K design.

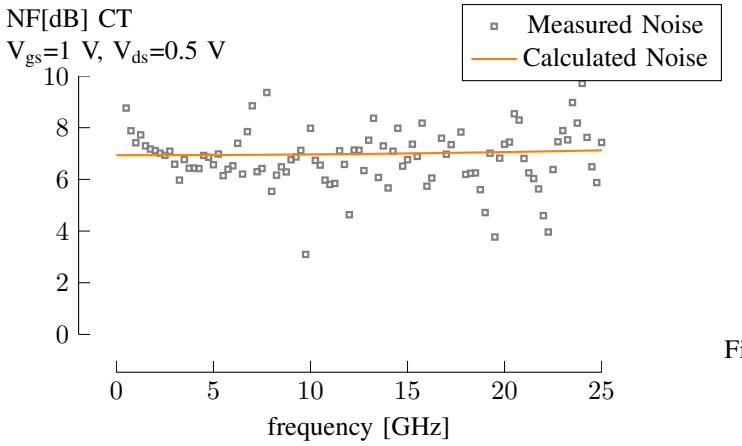

Figure 11: Measured and calculated noise figure (NF) as a function of frequency at cryogenic temperatures for V_{gs}=1 V, V_{ds}=0.5 V.

III. LUT CONSTRUCTION AND DESIGN

The LUT-based design tool illustrated in Fig. 12 is used as an alternative design environment, in particular when there is a lack of a compact model. The LUT database is constructed from experimental measurements at each temperature. A 4 dimensional sweep of the terminal voltages (V_{GS}, V_{DS}, V_{SB}) of transistors of the same width and varied lengths is performed. The small signal parameters of the transistors are retrieved from the measurements and stored in the LUT. Small signal parameters at standard temperatures can of course be obtained from simplified transistor models such as EKV or ACM or from a simulation with the technology design-kit. By using the LUT tool that runs in Matlab at a given temperature, the designer can perform a set of operations upon the LUT and follow a design methodology such as g_m/I_d [6].

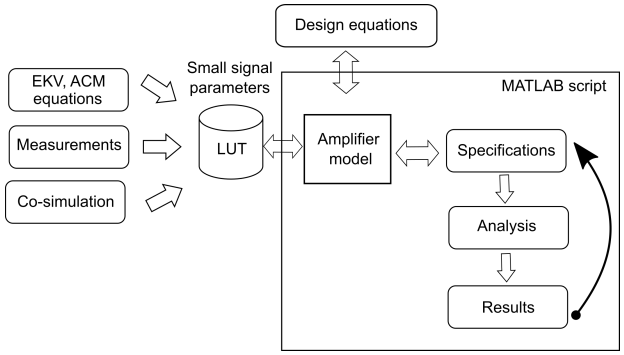

Figure 12: LUT-based design environment.

For the simulation of a circuit network, our LUT-based Matlab environment considers each component as a two-port network represented by 2x2 matrices for small signal power and noise analysis. Matrix operations are then performed for power and noise analysis of a circuit network. For example, the cascode amplifier in Fig. 13 is seen in Fig. 14 as a cascaded interconnection of a common-source transistor, a common-gate transistor and a load resistance, together with the feedback mechanism.

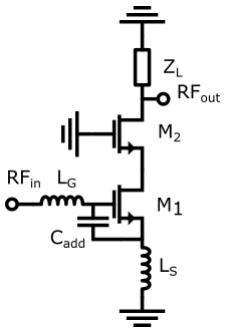

Figure 13: Schematic of cascode LNA (bias not shown).

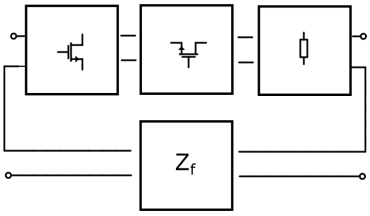

Figure 14: Cascode LNA as an interconnection of two-port subcircuits for MATLAB analysis.

IV. DESIGN OF A RF 4K CASCODE LNA INPUT STAGE FROM DC MEASUREMENTS

We describe next the design procedure for the RF cascode amplifier of Fig. 13 using the LUT environment. We target simultaneous noise and power matching so that the amplifier will have the lowest possible noise figure while having a maximum power transfer. The LNA must operate at 4 K with a power supply of 1 V, and it must show a central frequency of 7 GHz, bandwidth of 2 GHz, noise figure below 60 mdB, and a power consumption lower than 10 mW to serve in a readout stage for the simultaneous reading of multiple quantum bits.

The amplifier gain, assuming that both transistors are identical, is obtained from a schematic simulation of the circuit with the small signal parameters extracted from the LUT. The input impedance, on the other hand, is given by

$$Z_{in} = s\left(L_S + L_G\right) + \frac{1}{s\left(C_{gg} + C_{add}\right)} + 2\pi f_t^{'} L_s \qquad (8)$$

This formula defines the matching condition by sizing inductors L_S and L_G at the central frequency. We consider that the noise is largely dominated by transistor M1. With regard to noise matching, the optimum noise impedance is given by Eq. 6. We take advantage of the fact that the minimum noise factor F_{min} remains constant for each added finger in transistor M1. On the contrary, the total optimum noise impedance $Z_{sopt,tot}$ diminishes when N_f fingers are considered as given by $Z_{sopt,tot} = \frac{Z_{sopt}}{N_f}$, where Z_{sopt} is the optimum noise impedance of a single finger.

The sizing procedure can be resumed in a series of steps:

- Set the finger length that will give the lowest possible F_{min} of the technology.
- Set the inversion region using normalized g_m/I_d based on power and noise constraints.
- Set the transistor width and size of the added capacitor C_{add} to achieve $Z_{sopt} = 50\,\Omega$ and control the size of L_G.
- Size L_G and L_S for input power matching.

We sized three different amplifiers with the LUT at 4 K for strong inversion (SI), moderate inversion (MI), and weak inversion (WI). Table I shows the results for amplifier gain, noise, and power consumption. We used the available gain (G_A) to overcome the differences in matching between the simplified and PdK models. The closest performances to the target specifications are obtained with strong inversion.

IR	$\left.\frac{g_m}{I_d}\right\|_{norm}$	W/L [μm]/[nm]	G_A [dB]	NF [mdB]	L_g [nH]	L_s [pH]	C_{add} [fF]	I_d [mA]
SI	0.2	125/30	29.5	47.1	2.6	79.1	112	7.3
MI	0.5	99/30	19	102.5	2.6	266.6	122	0.874
WI	0.7	79/30	14.5	201.4	2.6	457.2	124	0.456

Table I: Cryogenic cascode LNAs designed for 4 K operation in the three different inversion regions.

V. Validation and perspectives for circuit testing

For the validation of this approach, we simulate the LNA performance at room temperature using the standard design-kit (PdK) for 28 nm FD-SOI technology. These results are compared with those of the LUT-based approach, considering that the LUT database is fed with transistor data obtained with the standard PdK simulation environment. Table II compares the results obtained in both cases, where differences are due to the use of simplified circuit network models for the LUT-based calculation instead of accurate 2-port matrices of the different components that are not yet available.

IR	A_v PdK [dB]	NF PdK [mdB]	I_d PdK [mA]	A_v LUT [dB]	NF LUT [mdB]	I_d LUT [mA]
SI	26.6	346.1	28.7	30.8	286.3	30.5
MI	20	413.9	4.6	21.13	397.5	4.6
WI	14.1	778.9	1.1	14.6	797.3	1.1

Table II: Simulation of cascode LNAs using a standard PdK and LUT-based approach at room temperature.

Finally, the test of the circuits at 4 K is specially costly due to the need of cooling. Screening faulty devices is of course possible by measuring the performances of the device at room temperature. These performances can already be predicted using the data in the LUT characterized at room temperature. Tolerance ranges can be defined by considering LUTs characterized with corner conditions.

VI. Conclusions and future work

The LUT-based approach is today already in use to accelerate design cycles at standard temperatures, often in combination with a gm/Id design methodology. This approach is specially important at cryogenic conditions given the current lack of design kits for simulation. This paper has illustrated this approach by using a LUT that has been constructed using 4 K DC characterization data. The design of the input stage of a 4 K RF cascode LNA for quantum applications has been carried out using the LUT data and simplified small signal networks. Future work will be aimed at obtaining accurate parameterized two-port power and noise correlation matrices for the different components using machine-learning to enhance accuracy. Interestingly, the LUT-based approach starts with a characterization step to build the necessary database that is further exploited for the design, and screening testing at room temperature of fabricated devices can also take advantage of this approach by extracting the required test performances directly from the LUT.

Acknowledgements

This work was supported by the French CIFRE program and the Labex MINOS of French program ANR-10-LABX-55-01.

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