A high voltage, high current transmission-line-pulse testbench for the reliability investigation of deep depletion, metal-insulator-semiconductor trench capacitors

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Keywords

«Capacitors», «Dielectric tests», «Test bench», «Snubber», « Pulsed current».

Abstract

This paper presents a work-in-progress design of a transmission-line-pulse testbench (TLPTB) for the investigation of the reliability of deep depletion, on-metal insulator semiconductor (MIS) capacitor at wafer level scale.
Firstly, we describe the capacitor (DUT) and the targeted application requiring the investigation of reliability: a snubber for wide-band gap (WBG) transistor. Then we explain the capacitor ageing mechanism induced specifically in the snubber application. We need to stress the capacitor repeatedly under high voltage (1000 V) and high current (100 A). The TLPTB is suitable for such stress pattern. The design is based on SPICE simulation prior to a board layout design. The theoretical subsection describes the expected stress sequence. The physical implementation is discussed along with a measurement setup.

1. Introduction

Since the beginning of power electronics, converter designers are trying to minimize overvoltage and ringing during switch transients. Indeed, overvoltage can damage the device and ringing generates Electro Magnetic Interference (EMI). These issues are more problematic with wide bandgap (WBG) transistors as the turn-off transient is very short.
Controlling the transistor switching trajectory during turn-off may require an RC snubber across the switch to reduce overvoltage and ringing as described by [1] on SiC components. GaN high electron mobility transistors (HEMT) may also benefit from a snubber, protecting against self-oscillating behavior as shown in [2]. Moreover, adding a snubber may enlarge the field of application of HEMT as explained in [3]. In the last two cases, the snubber protects the device during turn-off. A penalty comes with extra turn-off losses and the RC-snubber design is based on a tradeoff. The RC-snubber design is out of the scope of this paper. The snubber is implemented using discrete RC components connected as close as possible to the transistor. Stray inductances are inevitably introduced that reduce the efficiency of the snubber. As mentioned in [4], the stray inductance is roughly 3 nH for a D-PAK package. In order to reduce the parasitic inductance between snubber and power switch, an integrated solution is possible [5].
Prior to integration, there is a need for an assessment of the reliability of the RC device connected intimately to the GaN transistor. 3D Silicon trench capacitors are considered here. The state-of-the-art of reliability estimation is detailed in [6] and the particular case of a snubber is described in [5]. In the latter work, the lifetime estimation is based solely on the degradation due

to static biasing of the capacitor, using time dependent dielectric breakdown (TDDB).
However, the voltage and current waveforms across an RC snubber are far from the static biasing. A dynamic accelerated stress test should be considered. Multilayers ceramic capacitors (MLCC) ageing is investigated in [7] and [8]. Literature does not mention a similar approach regarding high voltage silicon capacitors. Failures mechanisms mentioned for silicon capacitors [9] include top-to-bottom metal short-circuit, electromigration, intermetallic compound formation and dielectric static degradation but in the scope of AEC-Q100 standard under low voltage. We have to note the work of [10] who investigate p-Si capacitor degradation under 150V and 200V voltage pulses stress in the scope of ElectroStatic Discharge (ESD).

2. Capacitor description

The intended reliability study concerns a Metal Insulator Semiconductor (MIS) deep trench capacitor. As explain in [11], when positively biasing the metal relative to the p-semiconductor substrate, a total capacitance C is obtained in a series combination of the insulator capacitance Ci and the semiconductor depletion layer capacitance Cd.

$$C = \frac{Ci \cdot Cd}{Ci + Cd} \quad (1).$$

The Murata technology is an improved version of the work described in [12]. The improvements offer a higher breakdown voltage, which is now 1500 V and the addition of an equivalent series resistor (5Ω) on the top capacitor layer to create a snubber.
This work is focused on the capacitor only. Indeed, on the snubber design, the resistor and the capacitor are intimately combined, and they will present separate failure mechanisms over time. For instance, the current flowing into the snubber generates power losses in the resistor. In turn, the resistor heats up the dielectric and may affect the capacitor lifetime. Considering non-correlated failure mechanisms, the study first concerns the capacitor. Fig. 1 and Fig. 2 show the capacitor under test. Fig. 3 and Fig. 4 describe how the capacitor is manufactured.

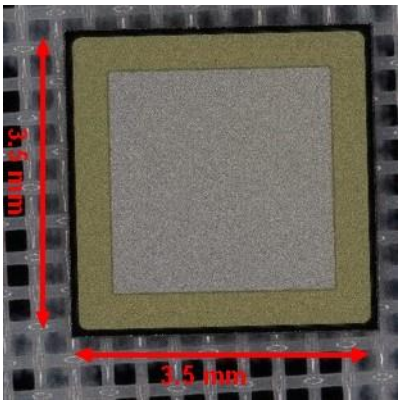

Fig. 1: Top view of studied silicon capacitors

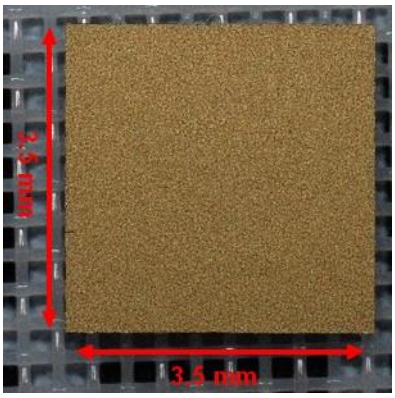

Fig. 2: Bottom view of studied silicon capacitors

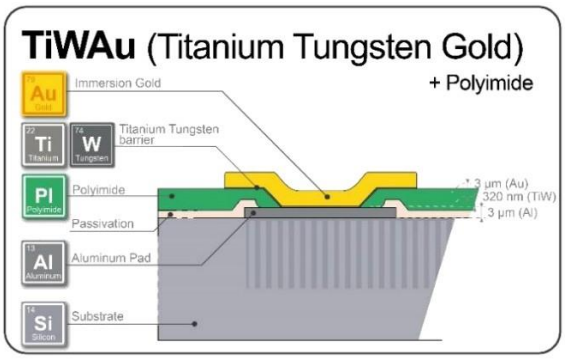

Fig. 3: Top layer cross section [13]

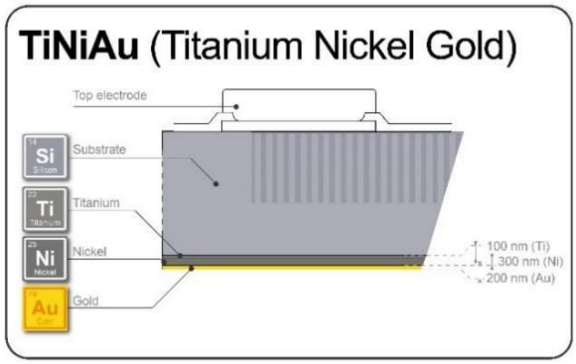

Fig. 4: Bottom layer cross section [13]

3. Snubber application

The typical snubber implementation is represented in Fig. 5 in a double pulse test bench (DPT) where R2 and C1 form the snubber.

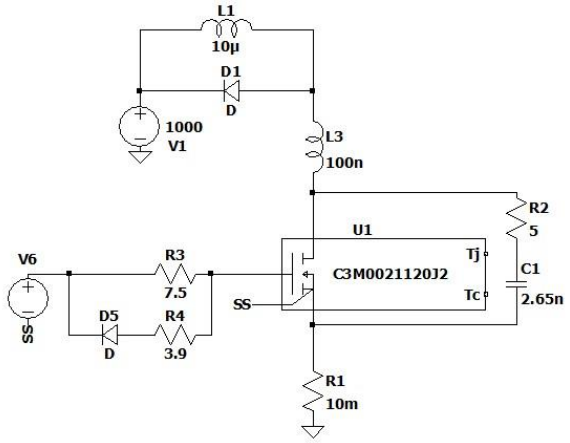

Fig. 5: Double pulse test bench with a GaN transistor connected to a snubber.

The schematic in Fig. 5 has been simulated using LTSpice to produce the waveforms in Fig. 6 to Fig. 8. The transistor has been selected with a Coss roughly ten times smaller than the snubber capacitor and rating voltage compatible with the snubber one. The transistor model comes from the manufacturer website. The other components are considered as ideal.

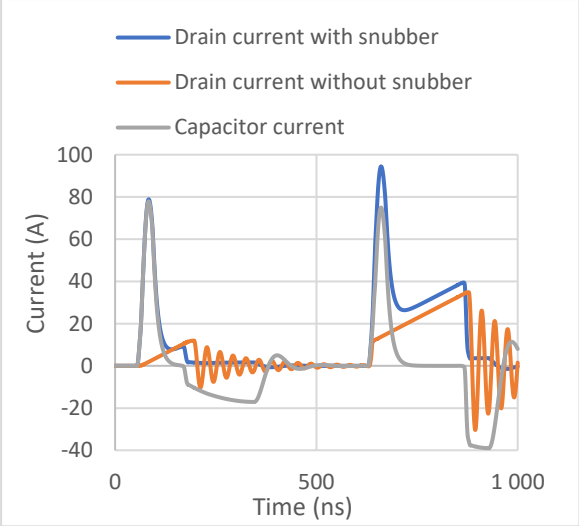

Fig. 6: Simulated currents in DPT.

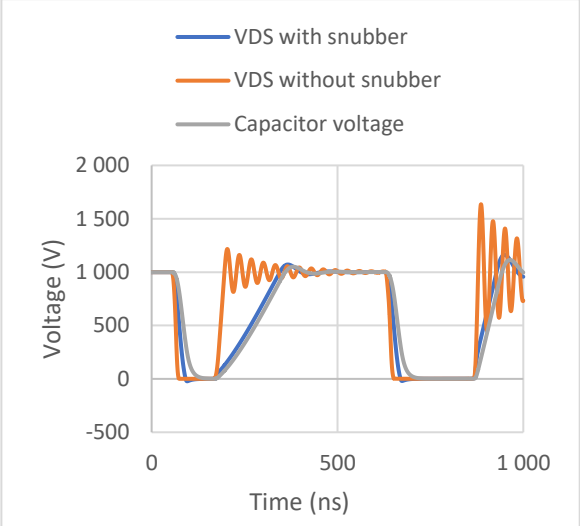

Fig. 7: Simulated drain source voltages in DPT.

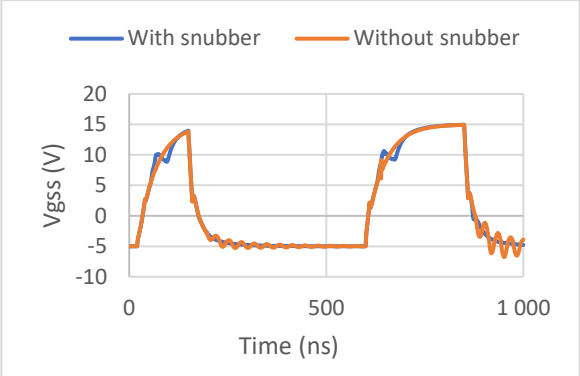

Fig. 8: Simulated gate source voltage in DPT application

Fig. 6 and Fig. 7 give an indication of the voltage and current waveforms to be applied to the capacitor to introduce an accelerated stress.

4. Ageing mechanism

Fig. 6 shows an asymmetrical capacitor current. According to [11], negative biasing voltage (relative to the p-semiconductor) is not detrimental as the structure enters an accumulation mode. Positive voltage during high frequency switching causes a deep depletion mode in the MIS capacitor as described in Fig. 9. It the field of metal-SO2-Si structures, high frequency means more than 1 kHz.

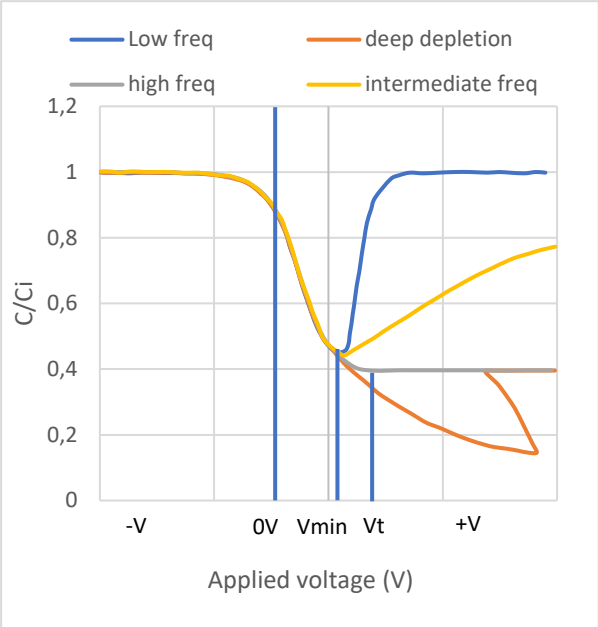

Fig. 9: MIS C-V characteristics. Voltage is applied to the metal relative to the p-semiconductor. Flat-band voltage of V - 0 is assumed [11]. Deep depletion occur with high frequency and fast sweep.

As a result, during deep depletion mode, the MIS capacitance is varying. The latter modifies the capacitance distribution over Ci and Cd. During transients, the electric field is no longer concentrated in the insulator but expands into the silicon bulk. The variation of C is due to the lack of minority carriers (here electrons) at the insulator/semiconductor interface. Under high electric field, electrons are accelerated, and become hot carriers entering the dielectric causing damages. For now, the main failure mechanism detected is dielectric breakdown appearing earlier than in TDDB conditions.

A reliability study aims at short term to give answers to questions like:

- How long can the dielectric withstand that kind a stress?
- What are the critical operating conditions?

A reliability study aims at long term to extract a lifetime prediction model separating wear-out mechanisms induced by the different biasing conditions, comprising the deep depletion and the silicon breakdown regimes that are not properly accounted with classical DC TDDB approach.

5. Test method

TLPTB has been studied regarding varactor for voltage-controlled oscillators in [14] and [15]. However, the rating voltage and the targeted application is far from the snubber specifications. As described in [11], negative voltage biasing ensure safe operating condition of the MIS capacitor even in high frequency pulse mode. Nevertheless, the snubber capacitor may need to act in both polarization in some applications like in solid-state circuit breaker presented in [16]

As a result, we need to stress the capacitor under test (CUT) with high di/dt pulse to charge the capacitor in positive biasing. To avoid useless self-heating and induce a parasitic ageing phenomenon, the device may be discharged slowly (few mA). Indeed, the RMS discharge current is negligible compared with the charging one. Obviously, ringing has to be avoided that excludes inductive charging. In addition, TDDB induced ageing must be avoided.

With a DPT test bench, the capacitor is always biased that induce undesirable TDDB ageing. Moreover, Fig. 6 shows negative current in the capacitor during turn-off transient state. This negative current may induce detrapping into the insulator and introduce another unwanted ageing mechanism.

An ESD test bench as used by [10] makes the pulse thanks to a capacitor greatly higher than the CUT. However, this approach needs to find a capacitor with a parasitic impedance largely inferior to the CUT one to be able to control the current pulse. In the proposed test bench, the transmission line solve this problem.

The TLPTB enables to control di(t)/dt at charging, maximal voltage and low discharging current (few mA) without ringing. Therefore, the pulse requirements are 1000 V maximum with pulsed current of 100 A. A Transmission Line Pulse Test Bench (TLPTB) [17] is so far the ideal candidate to perform accelerated ageing test on the capacitor at hand.

5.1 Theoretical study

In order to evaluate the reliability of silicon capacitors under deep depletion stress, we need to test numerous devices to evaluate snubber fabrication process. Thus, we choose to design TLPTB for wafer-level measurements. The

adapted design is presented in Fig. 10 and typical waveforms in Fig. 11.

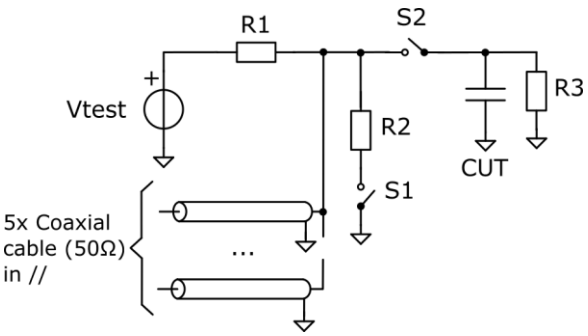

Fig. 10: Principle of the TLPTB.

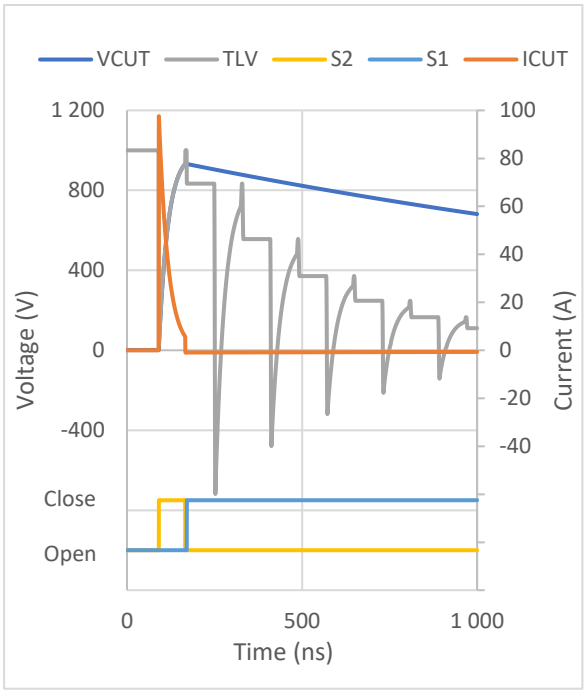

Fig. 11: TLPTB theoretical waveforms (VCUT: Voltage across the Capacitor-Under-Test; TLV: Transmission Line Voltage; ICUT: Capacitor-Under-Test current)

The stress sequence is composed of four steps:

1. Transmission line charging through R1
2. CUT charging when S2 is closed
3. Transmission line damping when S1 is closed
4. CUT discharging through R3 after S1 opening (not represented in Fig. 11)

During the first step, the transmission line is charged in quasi-static mode. Therefore, the line behaves like a large ideal capacitor. R1 is sized to ensure acceptable charging time and low power dissipation when S1 is closed. The arbitrary value of 1 MΩ. is selected.

The second step is CUT charging. In this case, the transmission line acts as a voltage source of initial voltage Vtest with a resistive impedance equal to its characteristic impedance (Zc). Thus, the peak current into CUT is given by:

$$ICUTpeak = \frac{Vtest}{Zc} \quad (2).$$

CUT charging time (CUTcht) is then:

$$CUTcht = 3 \cdot CUT \cdot Zc \quad (3).$$

The required transmission line length (TLlen) is estimated as:

$$TLlen = CUTcht \cdot c \cdot \rho \quad (4).$$

Where c is the light speed (m/s) and ρ the transmission line velocity factor

General-purpose coaxial cables have a characteristic impedance between 50 Ω and 75 Ω. Five 50 Ω cables of 20m long are wired in parallel to reach 10 Ω over 100 ns charging of the CUT.

A damping step has been added compared with the proposal in [17] to ensure good repeatability. The damping resistor (R2) has to match Zc. Finally, CUT is discharging through R3, which is selected arbitrarily as 100 kΩ.

5.2 Practical study

Due to practical considerations, the TLPTB scheme in Fig. 10 yields the schematic presented in Fig. 12 and the circuit simulation gives waveforms in Fig. 13.

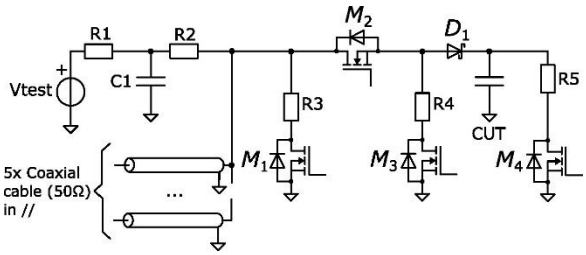

Fig. 12: Circuit schematic of TLPTB.

R1 and C1 are added to mask parasitic impedance of the voltage source, Vtest. M2, M3, R4 and D1 form the switch S2. Indeed, theoretical study considers a perfect switch but the real one does not switch instantaneously and has parasitic capacitance. SiC MOSFETs are selected as they

withstand voltage and peak current with minimum switching time and parasitic Coss. Three commercial devices will be evaluated: NVBG080N120SC1 (Onsemi), E3M0040120J2 (Wolfspeed) and IMBG120R045M1H (Infineon). M1 to M3 are identical because they have to operate under Vtest and potentially 100 A. M2 and M3 operate in opposition and D1 (SiC diode IDM02G120C5) blocks any reverse current from CUT. M2 lets the impulse flow from the line to CUT. M3 is here to discharge the parasitic capacitances of D1 and M2. Moreover, M3 and R4 also damp any current flowing through M2 parasitic Coss to limit glitches on CUT current as shown in Fig. 13. R4 is a damping resistor like R3, so it has to match also Zc. M4 is added to drive the discharge current and avoid matching issues.

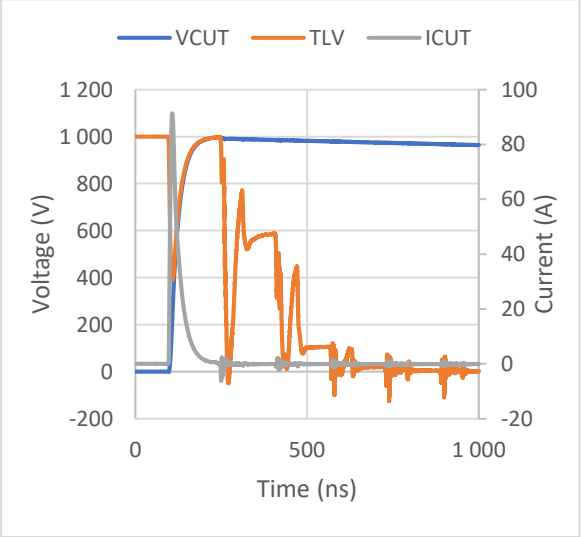

Fig. 13: Practical design simulation results

Two isolated standalone gate drivers IC are needed to source and sink 6.5A gate current to drive M1 and M4 respectively. An inductively isolated half-bridge gate driver IC is selected to source 4.5A and sink 9A gate current to drive M2 and M3 respectively. The device NCP51563CADWR2G is considered also for consideration of dead time to avoid cross conduction between MOSFETs. To manage gate voltage rise time, an adjustable low dropout regulator supplies the positive rail of each SiC gate driver from 14 V to 20 V. The gate driver negative rail is fixed at -5V.
The finite state machine made of high-speed logic gates delivers control signals for gate drivers.

6. Measurement setup

In order to follow stress cycle after cycle, we need to evaluate power losses in the CUT, hence the measurement of current and voltage.

6.1 Current sensing

Due to high di/dt pulse, the current flowing in the CUT during charging contains significant high frequency harmonics as shown in Fig. 14. Only the charging pulse is considered because discharging currently is negligible. To bring calculations closer to reality we consider 50 nH of stray inductance due to the current sensing implementation.

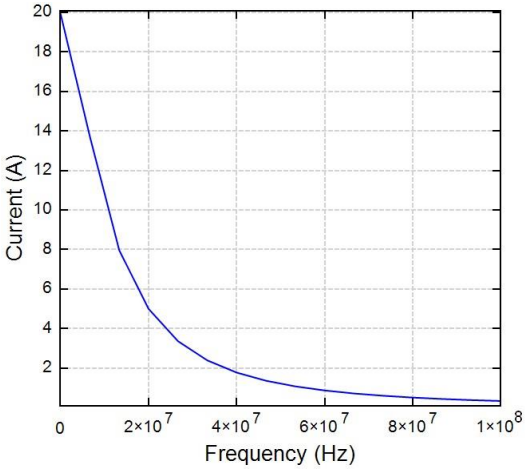

Fig. 14: Fast Fourier Transform of CUT current.

A Rogowski current probe CWT06 with 8 kA/µs and 30 MHz at -3dB bandwidth is selected. On the one hand, we lose only 3% of whole spectrum energy. On the other hand, the maximum theoretical di(t)/dt = 200 kA/µs out of reach of the probe.
However, measuring this level of transient current without 50Ω matching seems difficult. However power loss remains maximum when di(t)/dt is the largest, i.e. at VCUT = 0 V.

6.2 Voltage sensing

Voltage measurement is easier because dV/dt is reasonable. The voltage waveform is very close to an RC step response. As a result, the -3dB cutoff frequency is roughly:

$$fc = \frac{1}{2\pi \cdot CUT \cdot Zc} \approx 6\ MHz \quad (5).$$

Commercial high-voltage passive probes satisfy this condition. In order to simplify wafer level testing, the voltage probe is integrated on the TLPTB board (150x110mm) as presented in Fig. 15.

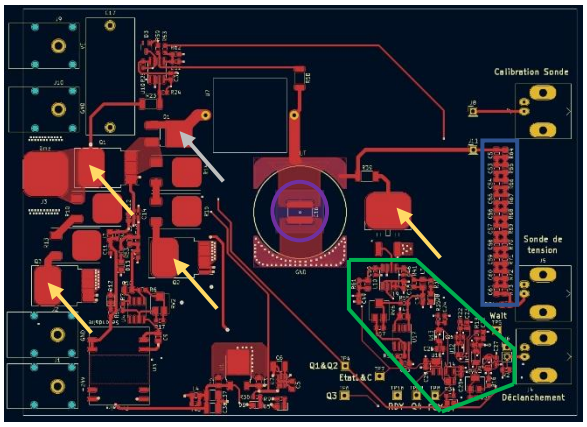

Fig. 15: top side of TLPTB board
Blue: voltage probe
Green: finite state machine
Purple: CUT (wafer probes will be replace discrete device)
Yellow: Power MOSFET
Grey: Power diode

6.3 Capacitor ageing monitoring

In [10] it is also investigated the effect of repetitive voltage pulses stress on p-Si MOS capacitor. This study confirm ageing polarity dependence, and early dielectric degradation under voltage pulses stress. To evaluate capacitor ageing, [10] selected capacitance and resistance measurements made with LCR meter.

In our case, hot carrier trapping results in poor dielectric characteristics that may increase the leakage current. Moreover, the peak current will damage the capacitor electrodes that may increase the equivalent series resistor (ESR). Therefore, in a first time we will measure ESR, capacitance and leakage current in quasi-static condition. Measurements will be done a long time (several µs) after stress to be sure that the capacitor is in a stable state. Indeed, we expect detrapping in a short time after stress that might affect measurements. The selected biasing voltage is 400V because it is close to the static condition of the targeted application.

7. Conclusion

The reliability study of capacitor under the stress generated in the snubber application is a work in progress. Main failure mechanism has been identified. The scheme for accelerated stress test has been selected and a TLPTB has been designed and simulated. The measurement protocol is not optimal to follow precisely current, but it might be acceptable for power loss evaluation. A printed circuit board has been designed with short-term delivery for experimental verification.

Compared with other dynamic stress methods presented in [7] and [8], TLPTB has nothing in common with the targeted application but realizes the stress protocol focused on the ageing mechanism of interest. Indeed, semiconductor physic has been more studied than ceramic capacitor physics. TLPTB should allow predicting accurately capacitor lifetime under the particular type of stress installed in a snubber and let us verify if the capacitor manufacturing technology is well qualified for the application.

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