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Performance evaluation of a versatile and low-jitter White Rabbit board

Daniel Charlet, Paul-Éric Pottie, Antoine Back, Monique Taurigna-Quéré, Cédric Esnault, Chafik Cheikali, Cedric Dumez-Viou, Christelle Soulet, Michel Lours

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HAL Authorization



Low jitter WhiteRabbit development





● IJCLab

- Hardware : Daniel Charlet
- Firmware : Eric Plaige, Antoine Back, C dric Esnault, D.charlet
- Software : Monique Taurigna, Chafik Cheikali, A.Back, Christelle Soulet
- Test : C dric Esnault, Daniel Charlet

● Paris Observatory

• SYRTE

- Clock expertise and qualification : Paul-Eric Pottie
- Hardware : Michel lours

• Obs Nancy

- Firmware : C dric Viou



Systemes de R f rence Temps-Espace





Current WR projects:

- R&T TIMED
- IDROGEN board
- Paon IV project
- Master Oscillator



WR RESEARCH & TECHNOLOGY : TIMED

- 5 Laboratories , 2 institutes (IN2P3 & INSU)

- Schedule : 4 years

- Budget : 80K€

- Goals : WR capability extensions :

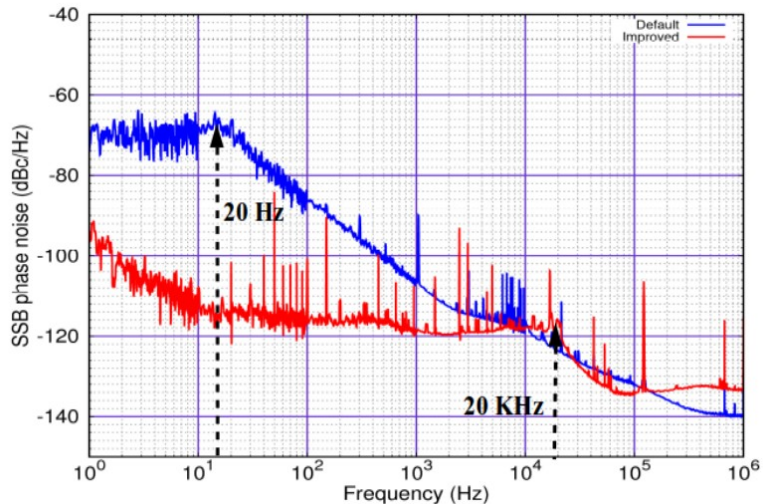
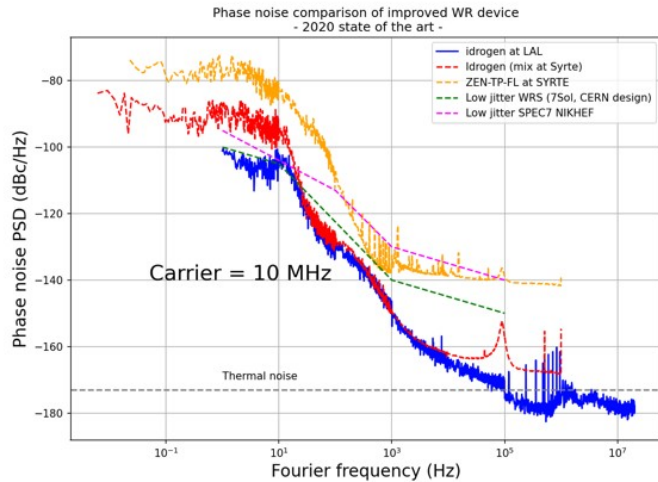
- xTCA crate implementation
- WR implementation simplification
- WR FPGA external functions integration
- WR enhancements (High stability frequencies)

- Contributions :

- LPC Caen : Performance evaluation of a commercial crate controller including a WR switch
- LPSC : Custom development of a crate controller including a WR switch
- LP2IB : WR external VCXO (controlled oscillator) integration
- IJCLab : WR simplification & enhancements,
- IJCLab accelerator department & KEK accelerator: Master oscillator distribution
- Observatoire de Paris : WR enhancements



R & T TIMED : Increasing performances



Collaboration with Paris Observatory Laboratory

- Goal 1 : $\sim 1\text{ps}$
- Goal 2 : $< 100\text{fs}$

Soft PLL modification

- Decreases the response time of software PLL : μP frequency upgrading
- Gain integrator optimization

Increased PLL bandwidth of the GM Local oscillator

Components upgrading

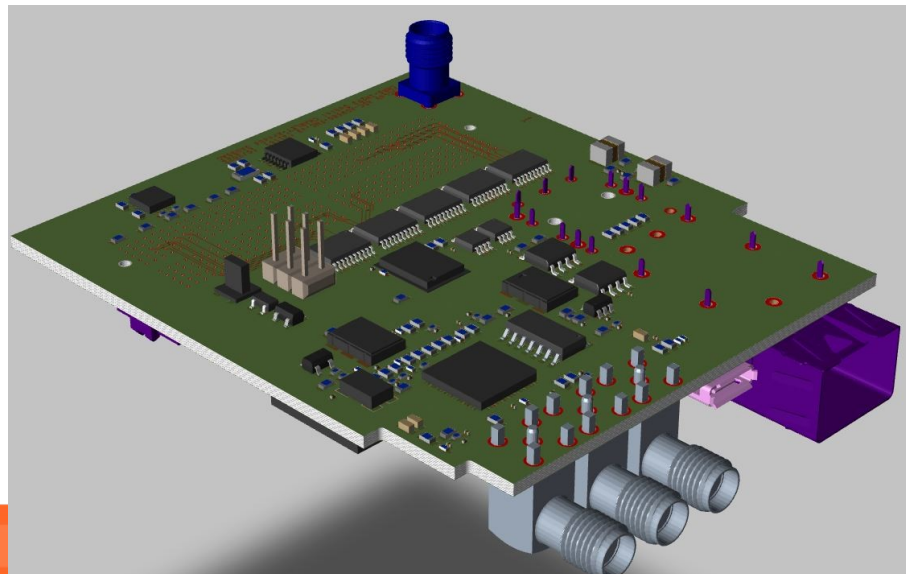
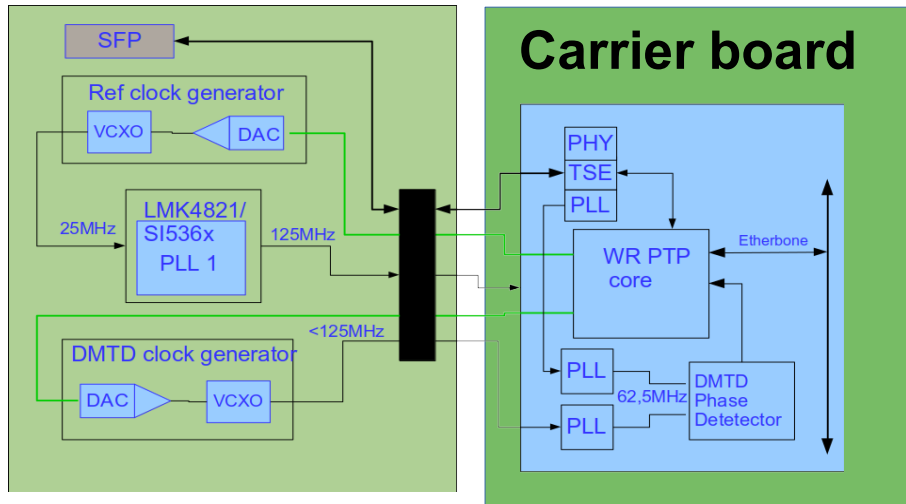
- VCXO selection
- Increased internal Frequency (PLL number reduction)

Modification of WR principle

- phase modulation and demodulation of an ultra-stable optical carrier
- Replacement of message protocol by timecode
- Phase measurement in optic



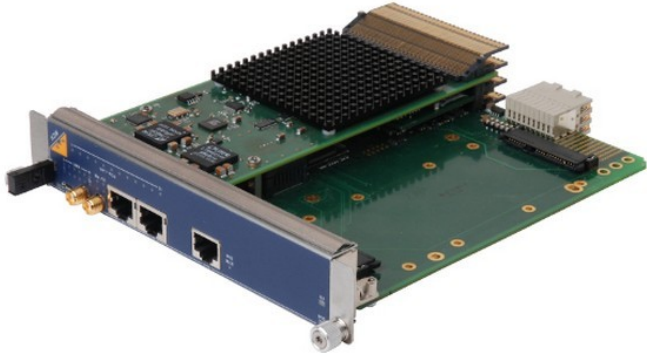
WR development boards : FMC_PLL



- FMC WR development
- 2 IN2P3 laboratories collaboration
- 2 types of boards : SI536x, LMK4821
- All external functionalities
 - PLL, SFP, DAC, VCO, CLOCK, PPS, WR
- Test for new components
 - FPGA : AGILEX,
 - LMK4828/LMK4821
 - SI5362
 - VCXO
- Currently in layout design phase



R & T TIMED : WR Crate integration

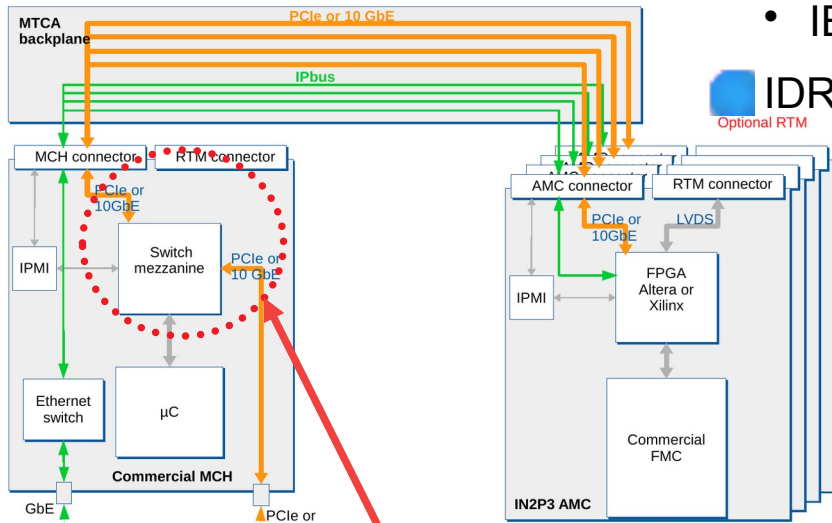


WhiteRabbit on μ TCA

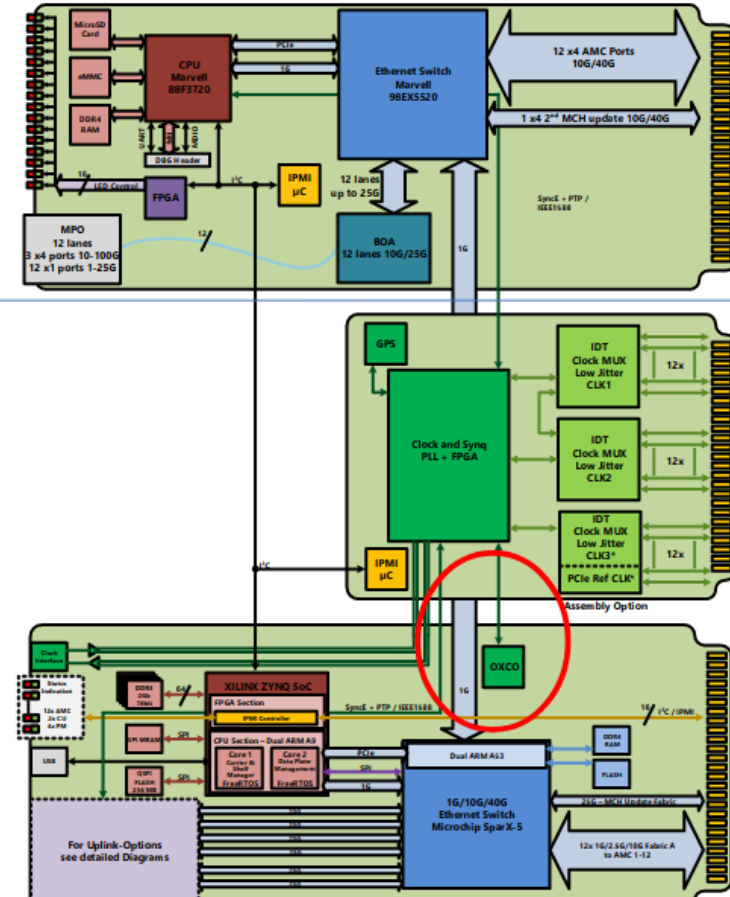
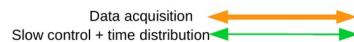
- Only switch functionality (no master)
- WhiteRabbit on copper link
- Sync-E function on MCH board
- NAT-MCH-4

- IEEE1588V2 compliant switch

IDROGEN board

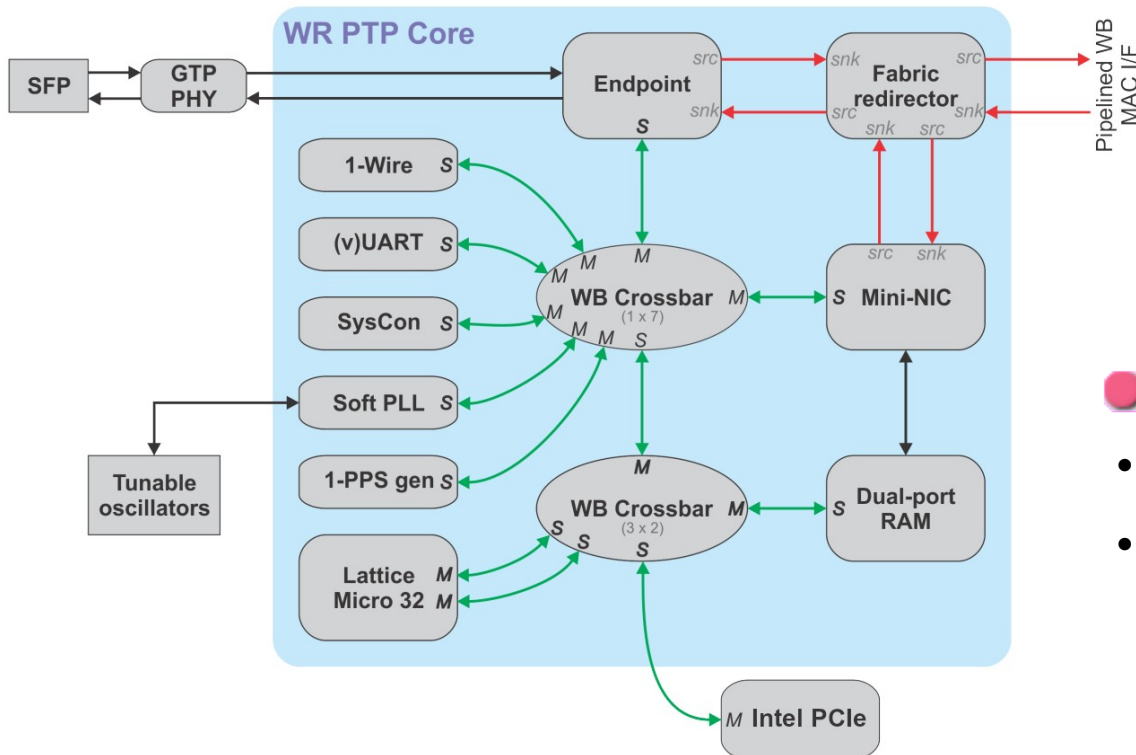


Sync-E switch





WR Firmware & software ALTERA developments



Firmware :

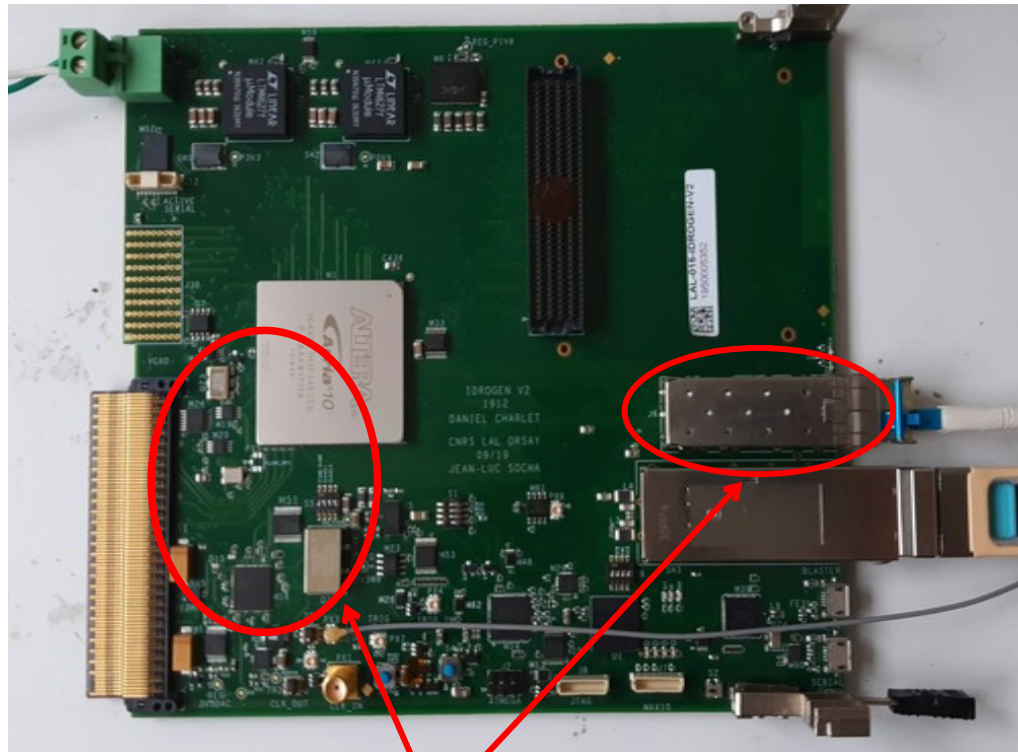
- ARRIA 10 WR implementation : PHY and PLL port (Based on ARRIA 5 GSI project)
- Avalon to Wishbone bus access
- PCIe with DMA
- IpBus 1G/10G (Base on LPSC project)

Software :

- WR shell on PCIe interface and IpBus (1G & 10G)
- Direct access to WR Wishbone bus
- Virtual UART
- Diagnostic mode
- Micro 32 ram



WR hardware IJCLab IDROGEN board : Low phase noise WR node

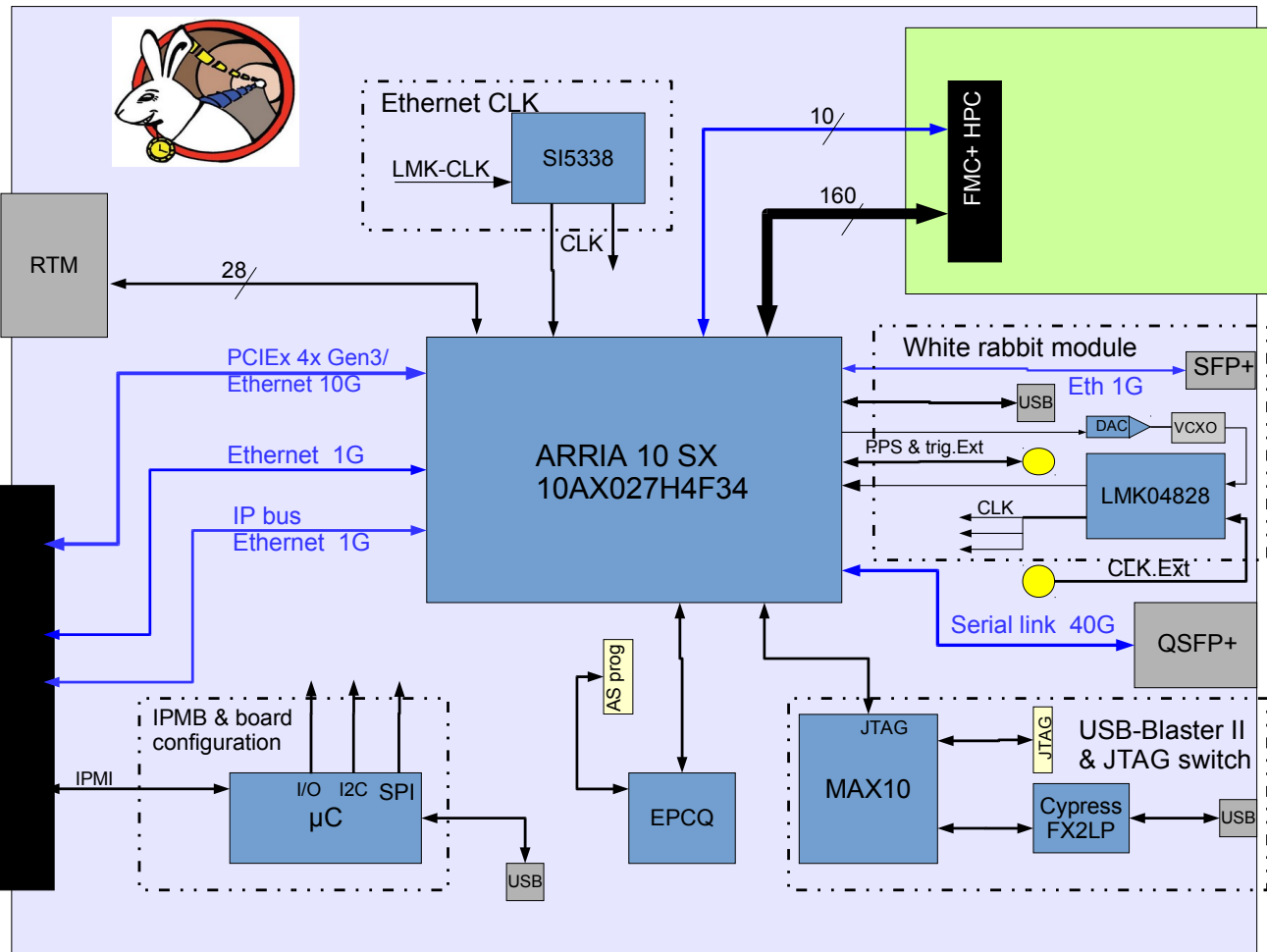


WR implementation

- Design & development done by IJCLab
- CERN schematic improved
 - Components upgrade : PLL, VCXO, FPGA
 - PCB design compliant with EMC rules
- High performance WR low jitter node :
 - Accuracy < 20ps, Jitter < 1ps
- High performance data acquisition system:
 - PCI express > 30Gbs, Ethernet > 20Gb
- Crate (μ TCA) or stand alone use
- FMC+ carrier board for additional functions :
 - ADC, DAC, Clock synthesis, ...
- Firmware development done by Nancay Observatory and IJCLab
- Clock expertise and qualification by SYRTE (Observatoire de Paris)



IJCLab IDROGEN board : Low phase noise WR node

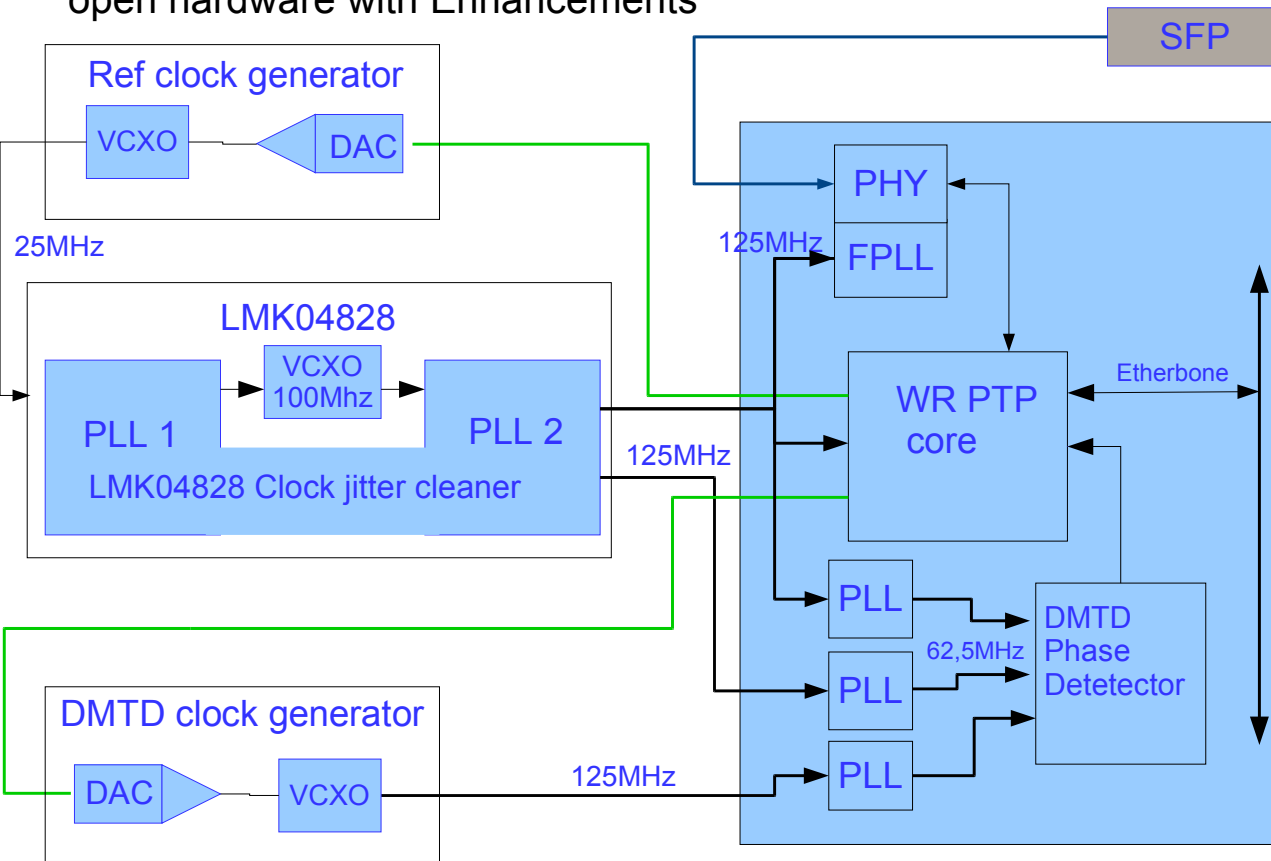


- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC+ slot)
- 160 single-ended I/Os (80 LVDS) and/or up to 40 transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant
- Configurable output clock
- Front panel connectivity :
 - WR SFP+
 - QSFP+ 40G, USB
- Backplane connectivity :
 - 1Gbe Ipbus, PCI 4x Gen3
 - IPMB, CLK & trigger lane
 - RTM connector : J30



IJCLab IDROGEN board : WhiteRabbit implementation

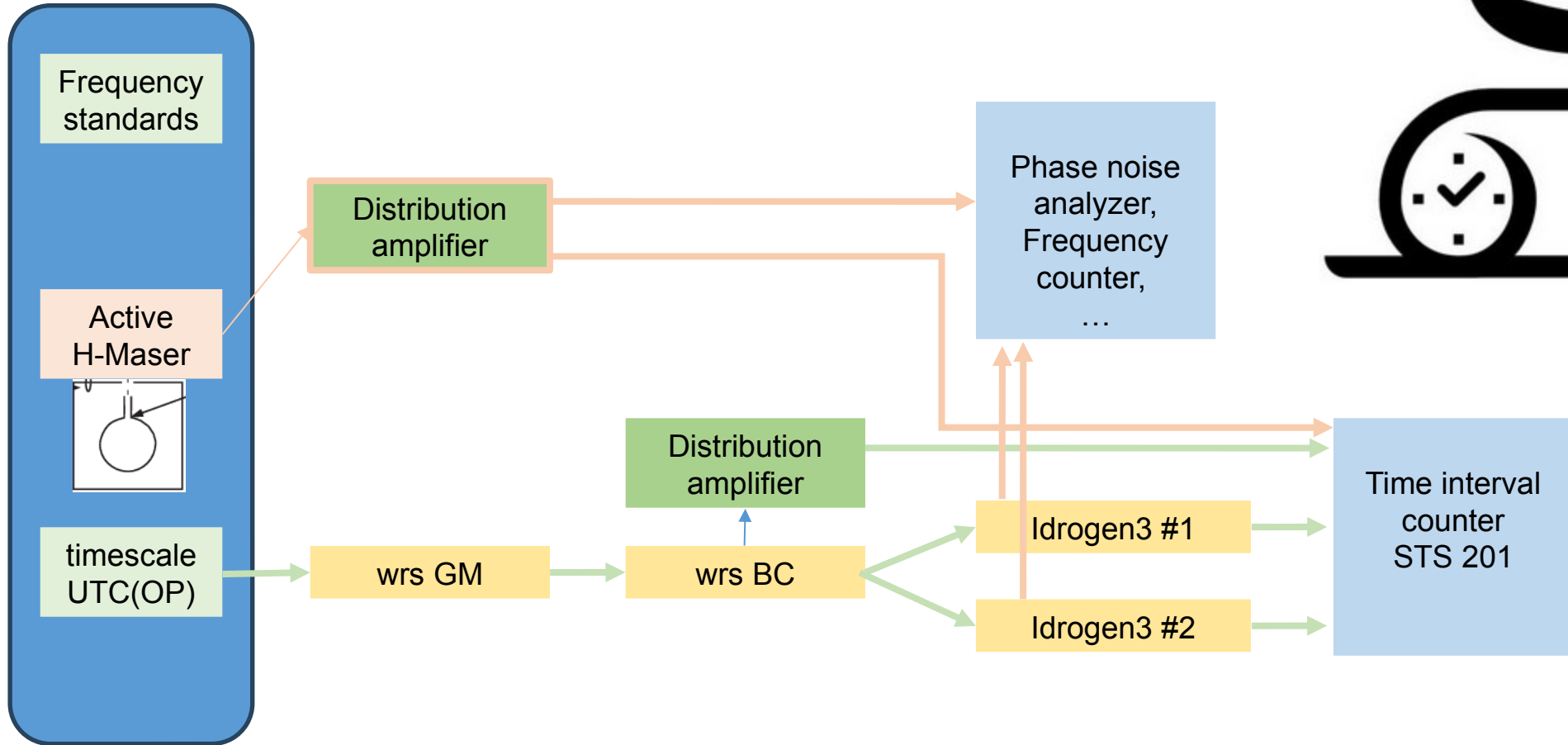
The WhiteRabbit IDROGEN hardware is based on CERN open hardware with Enhancements



- Based on LMK4828 synthesiser
- Ultra low noise clock jitter Cleaner with Dual Loop PLL
- 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
 - DDMTD source (comparison between WR master clock from SFP)
 - PLL source with phase adjustment
- IDROGEN Enhancements**
 - PLL selection
 - VCXO Frequency
 - Input frequency for DDMTD
 - Tx/Rx routing equalisation

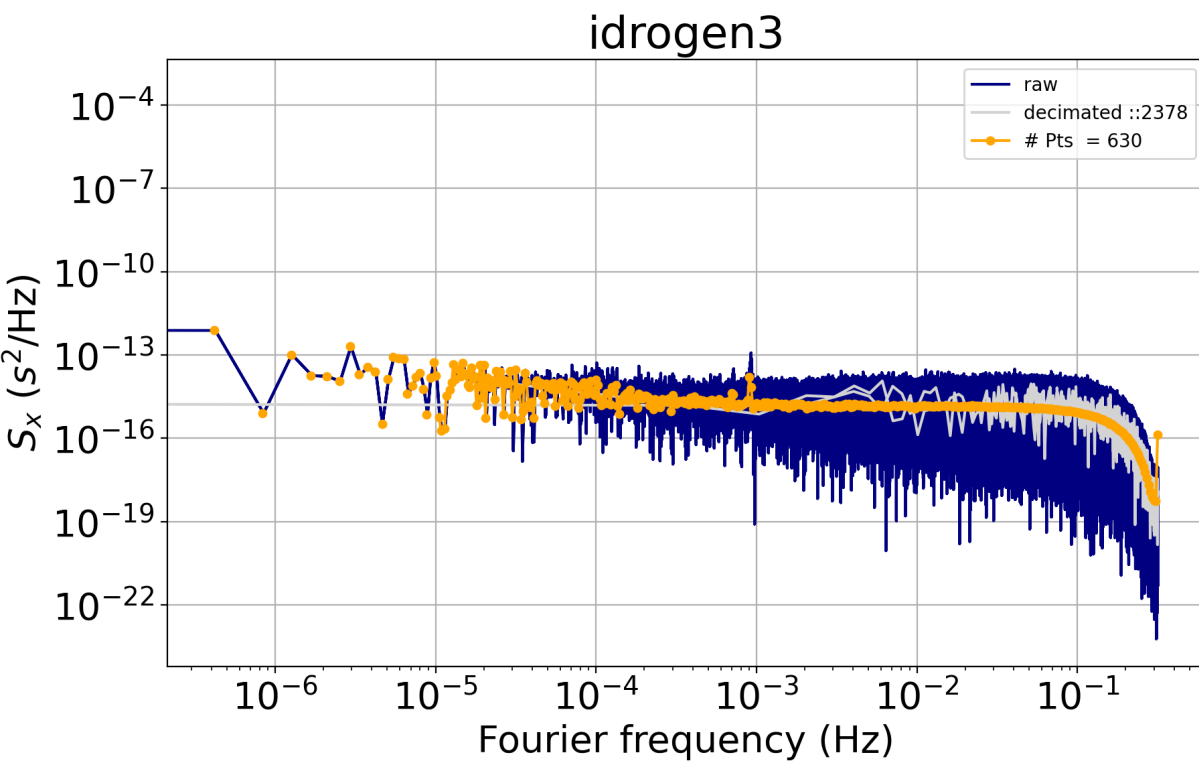


Syrte test setup

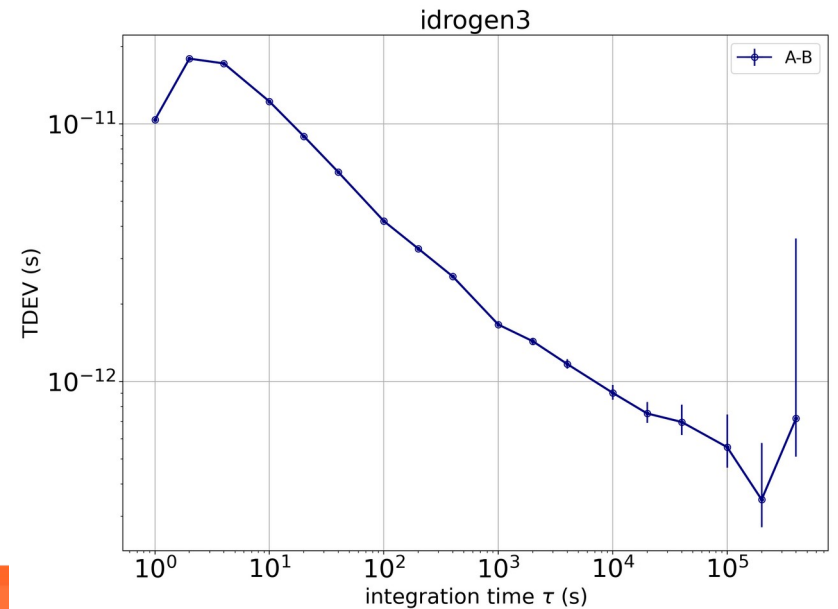


2 Idrogen boards, in the same chassis, connected by 2-m fiber to the same wrs. H-maser is in common view.

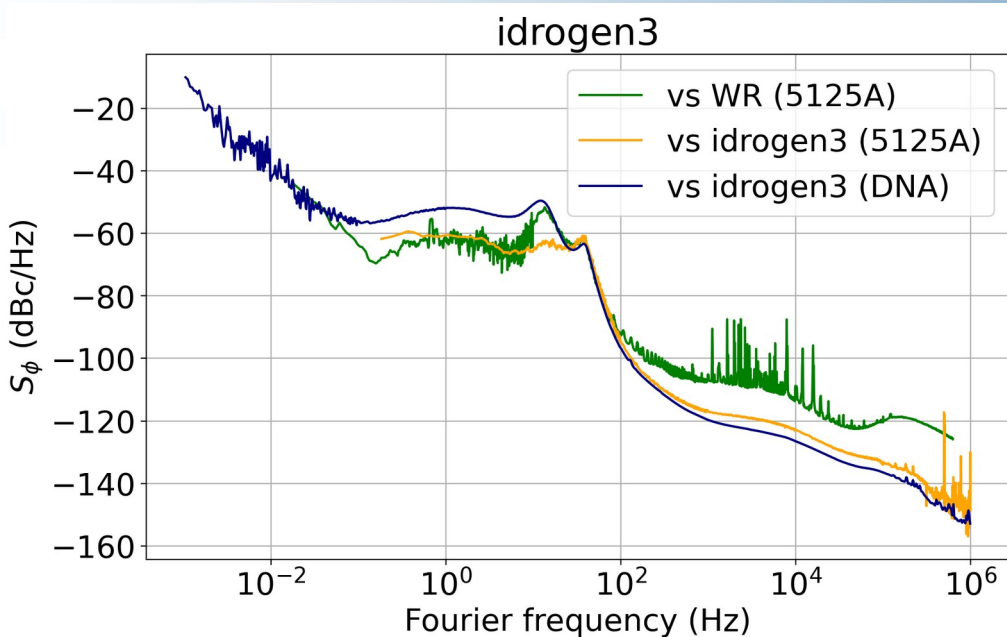
IDROGEN board performances



- the measurements were made by SYRTE (P.-E.Pottie)
- Measure the time interval between idrogen#1 and idrogen#2 PPS :
 - Rms jitter ~ 20 ps
 - TDEV: 10 ps @1s; <400 fs @ 2^e5 s.
 - Flat FFT (ti) down to $< 1^e-6$ Hz



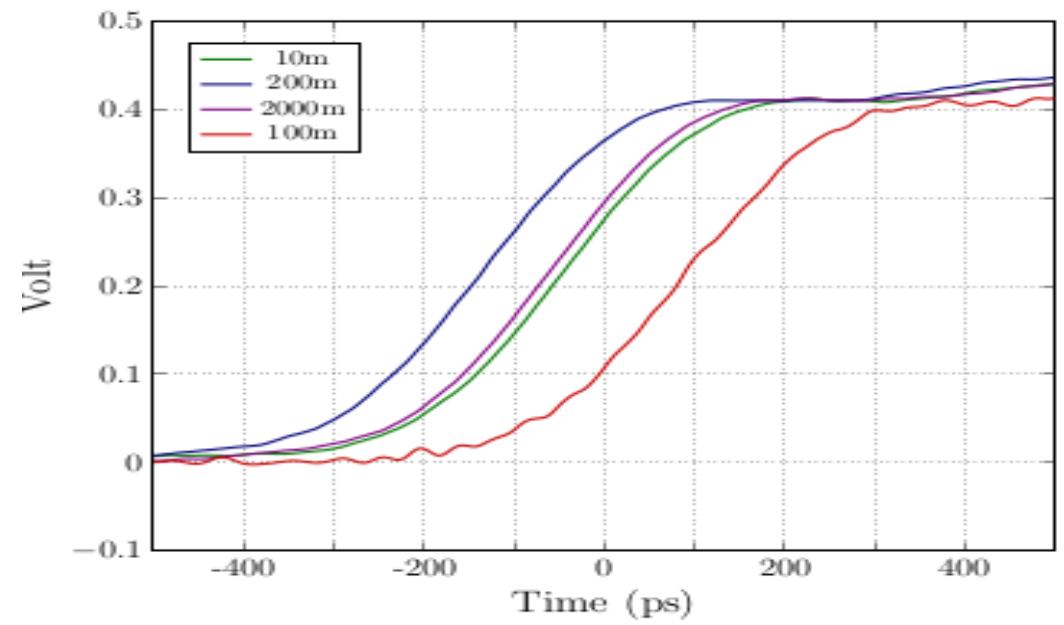
IDROGEN board performances



2 phase noise analyzers :
5125A (Symmetricom)
DNA (Noise XT)

- PPS measurements for different fiber lengths
- From 10 m to 2 km
- Time accuracy below 100 ps

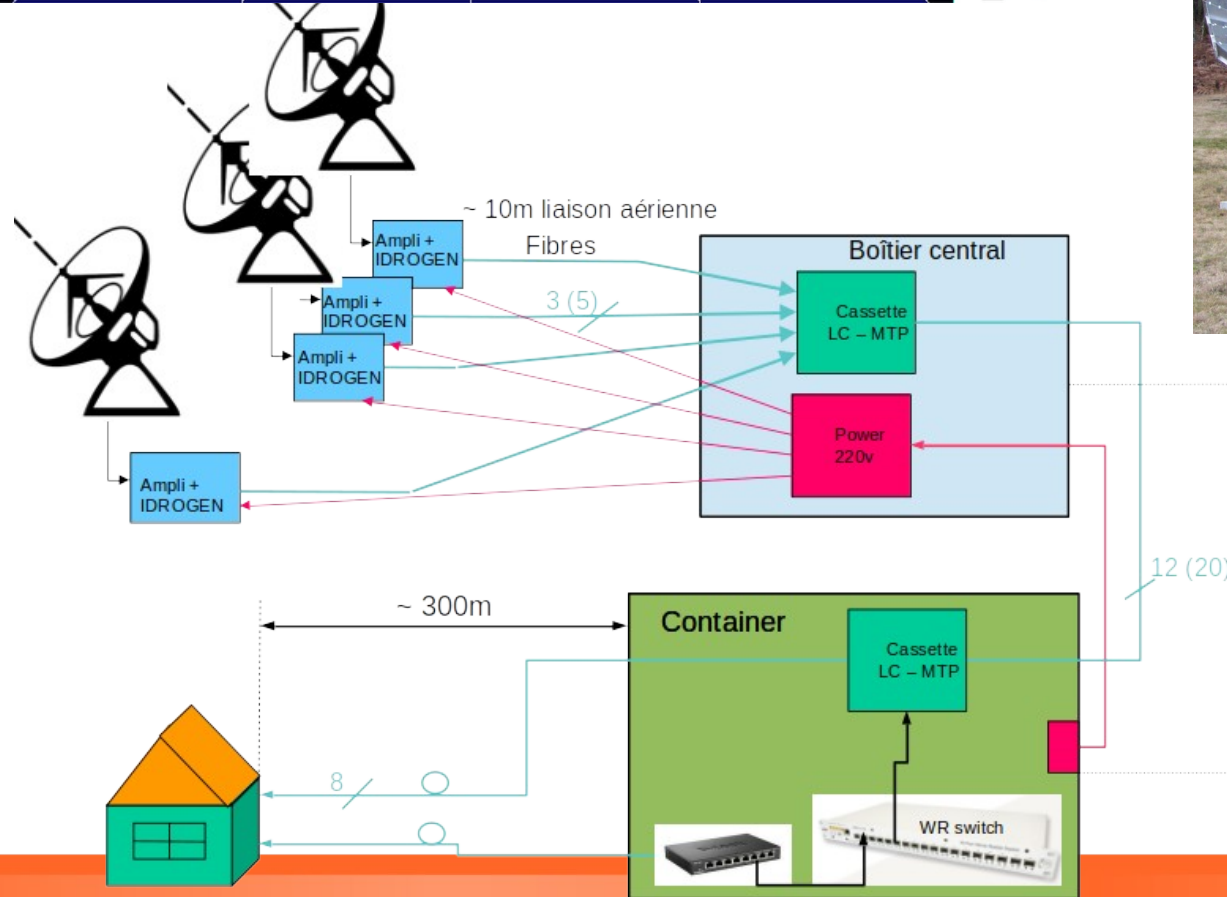
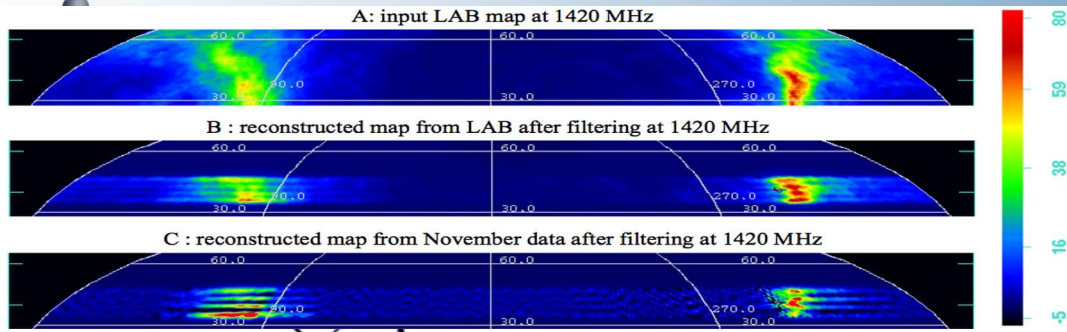
- the measurements were made by SYRTE (P.-E.Pottie)
- transfer from one WR switch to two IDROGEN boards





PAON IV project

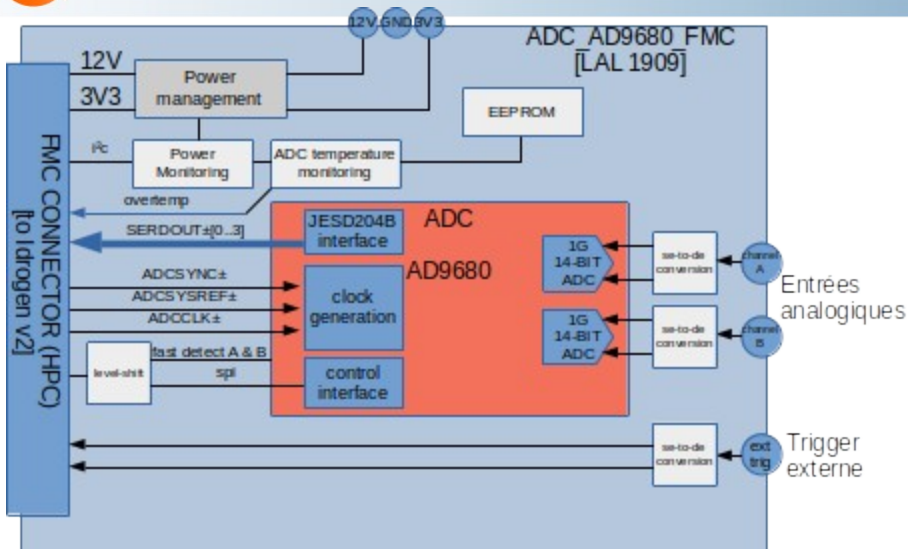
PAON IV : Radio interferometer



- Radio interferometer for 3D mapping of atomic Hydrogen
- Direct coding at the antennas
- Bandwidth $1\text{GHz} < \text{Freq} < 1.5\text{GHz}$
- Synchronize by WR
- Data transfer by UDP 2 x 10Gb



FMC_AD9680_500MSPS



The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :

- includes : its own PLL.
- ADC clock source : External clock

Mezzanine main features :

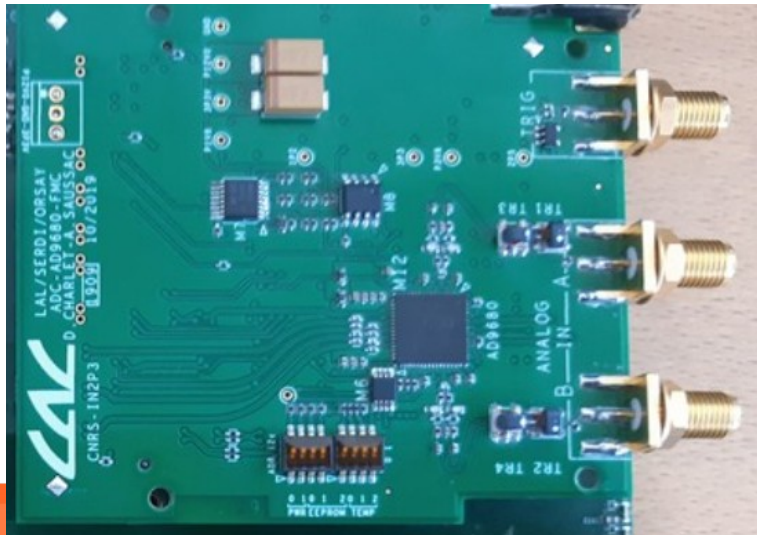
- VITA57.1 (FMC), ADC 9680, 2 channels, 14 bits
- 500 MSPS, JESD204B, 2GHz analog bandwidth
- External trigger in

Bandwidth 500 MHz to 1.5GHz

Synchro & timing by WR

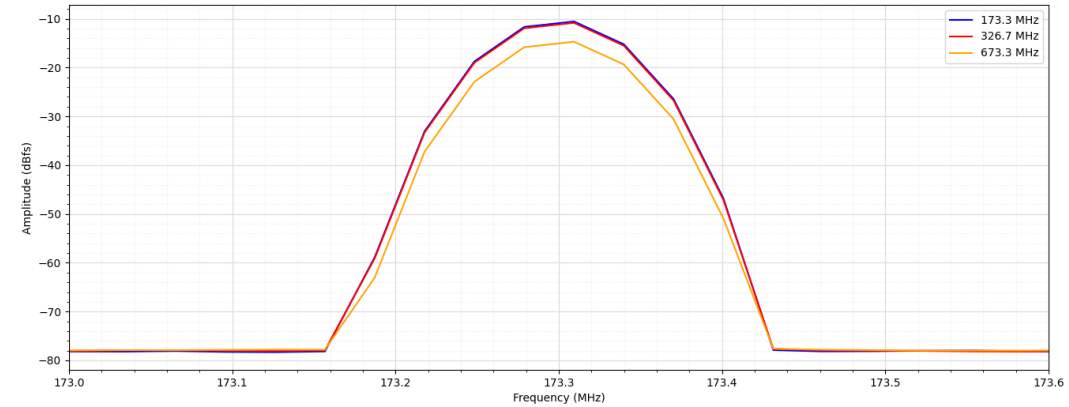
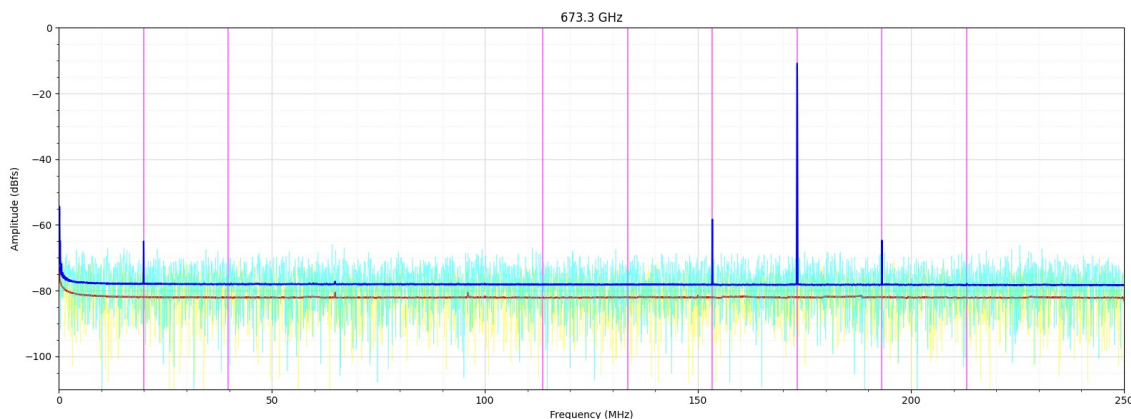
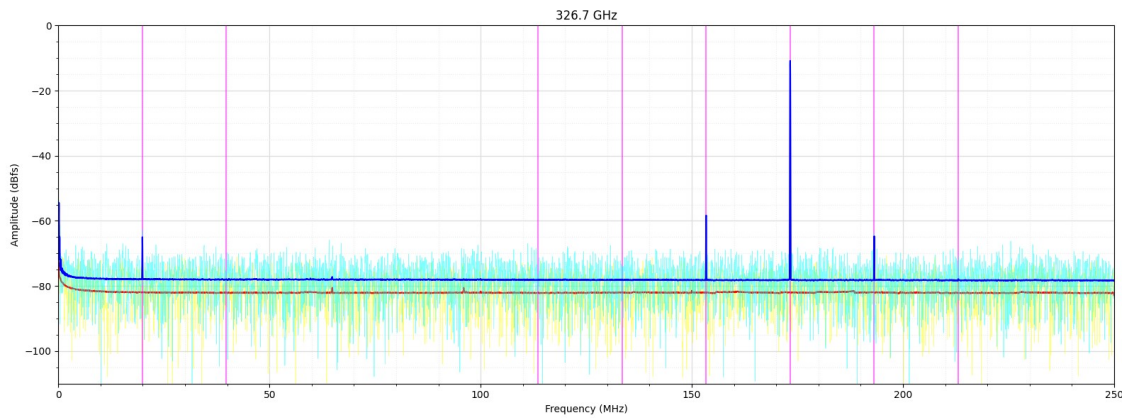
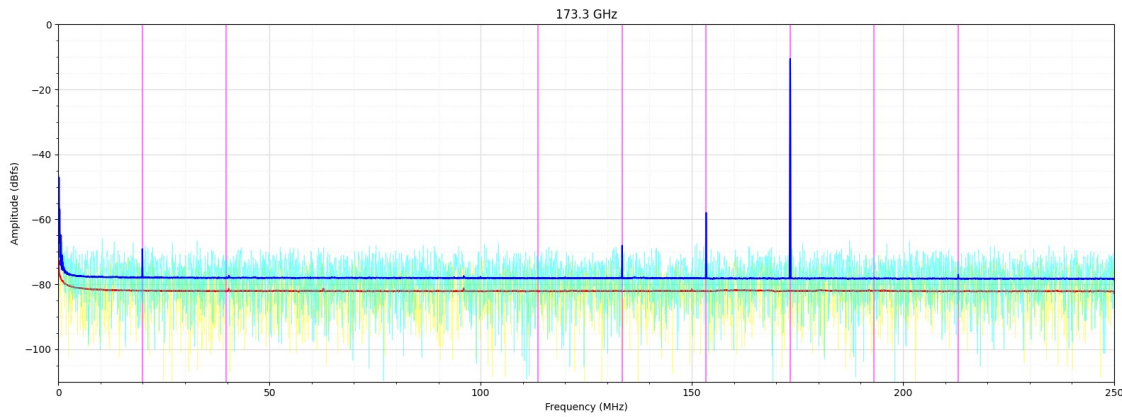
Data transfer 2x 10G Ethernet

Configuration by IPBus 10G



FMC_AD9680 results

- Blue channel with signal
- FFT 16K, Average over 10000
- First : second , third Nyquist band



- Level of central frequency
- 0,4db on second Nyquist band
- 4db on Third Nyquist band
- Level calibration to be performed



FMC ADC_9680 : Synchronisation

LM04828

SYSREF Clock SYNC

SYSREF

Clock

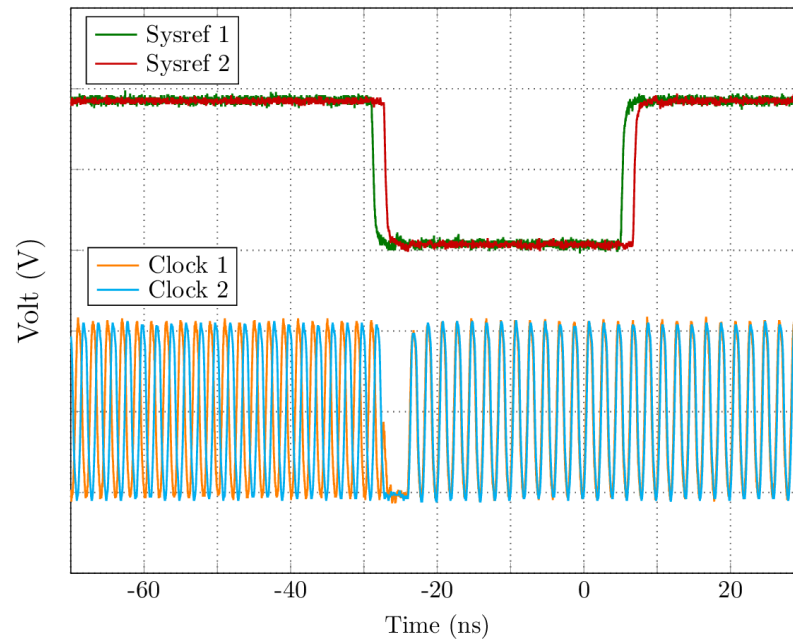
ADC9680

PPS

FPGA

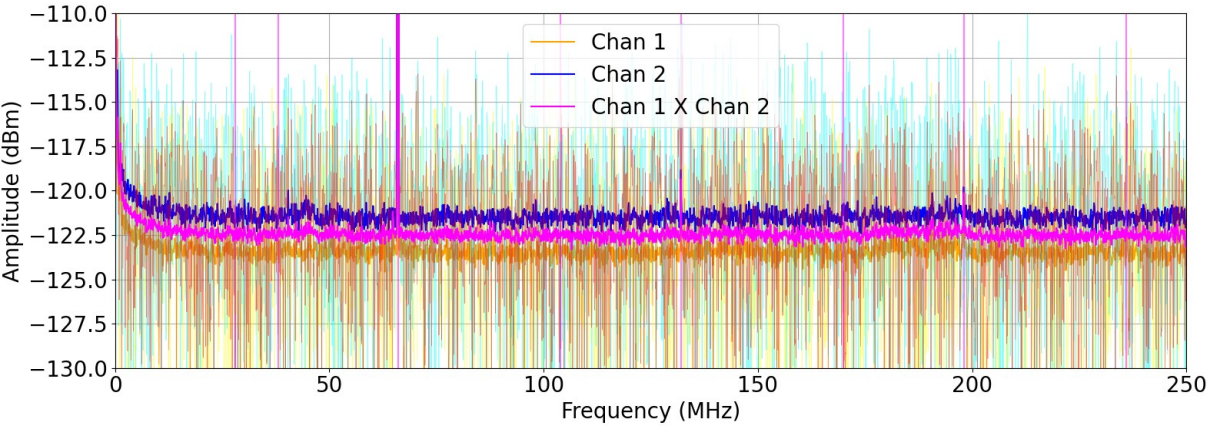
- 2 IDROGEN boards synchronize by WR
- PLL : LMK04828
- ADC data transfert : JESD204B class 1
- 500MHz Clock
- Phase alignment by PPS

LMK04828 Clock Synchronization

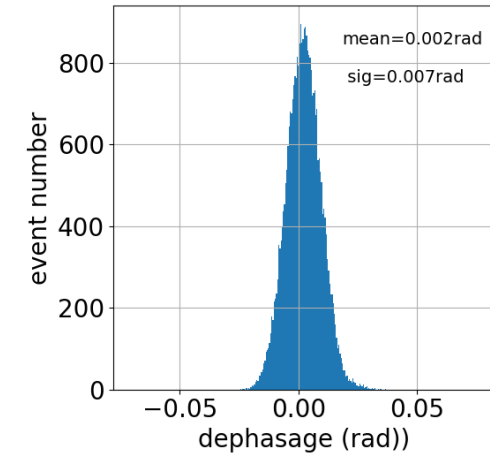
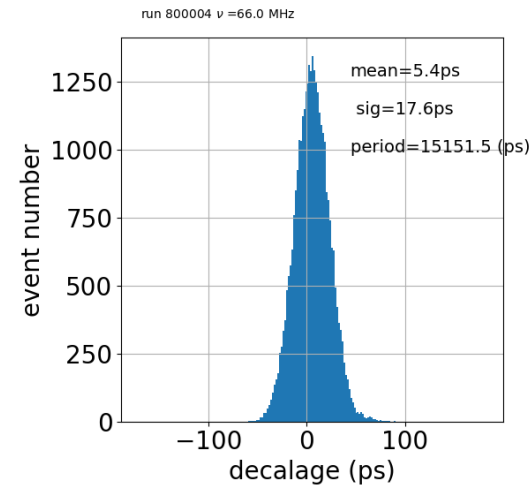
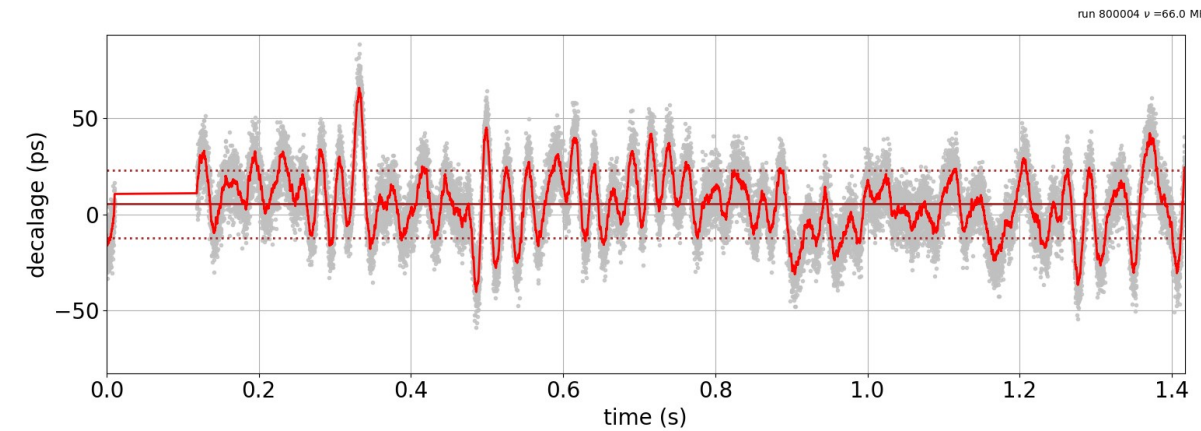




FMC ADC_9680 : Synchronisation

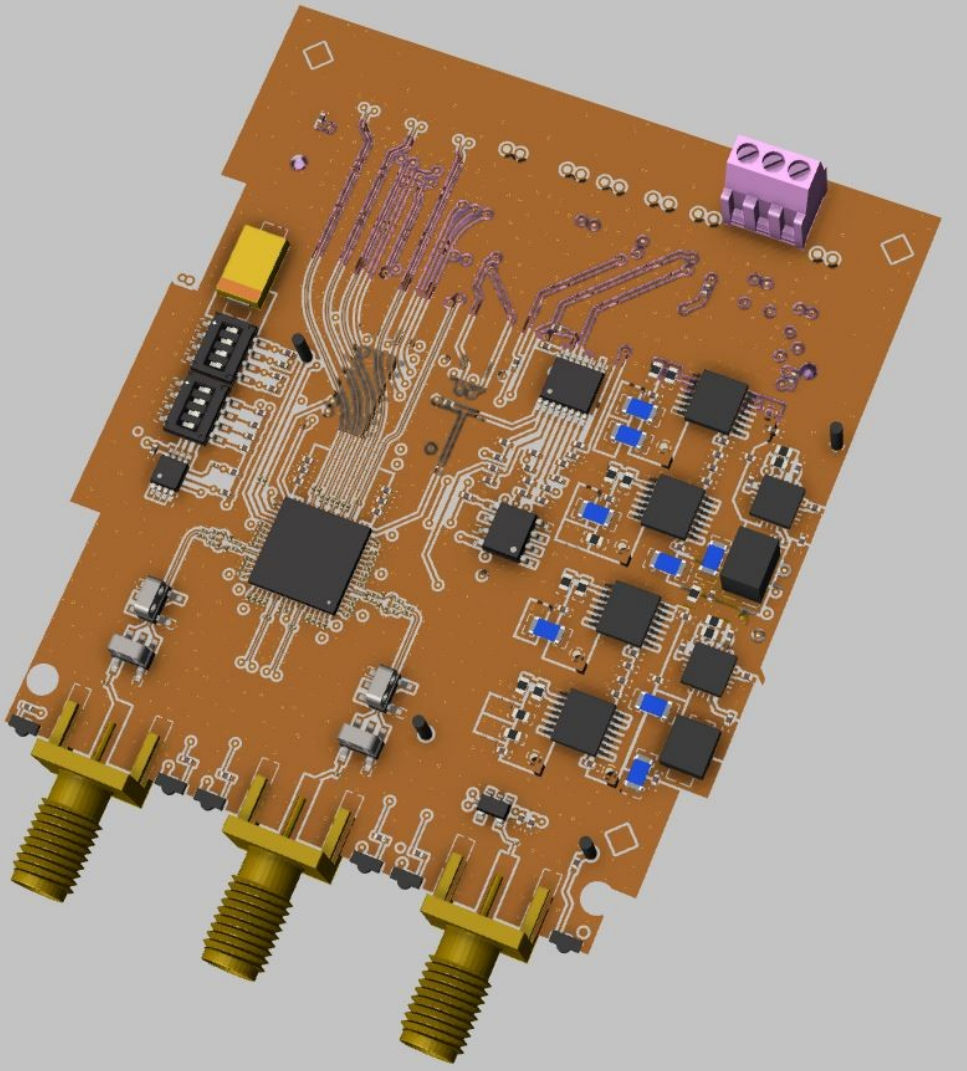


- 2 IDROGEN boards synchronize by WR
- Same RF signal (66MHz) split on boards
- FFT 16K point
- Cross correlation





FMC_AD9680_1GSPS



■ Mezzanine main features :

- VITA57.1 (FMC), ADC 9680, 2 channels, 14 bits
 - 1 GSPS, JESD204B, 2GHz analog bandwidth
 - External trigger in
- ## ■ Bandwidth 500 MHz to 1.5GHz
- ## ■ Synchro & timing by WR
- ## ■ Data transfer 2x 10G Ethernet
- ## ■ Configuration by IPBus 10G
- ## ■ Layout finished, in production next week



Master oscillator distribution



FMC_SI536X for IDROGEN

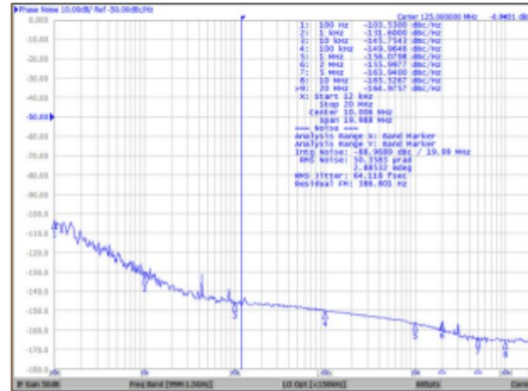
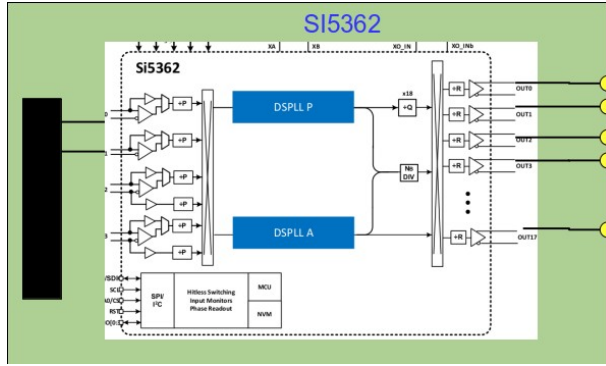
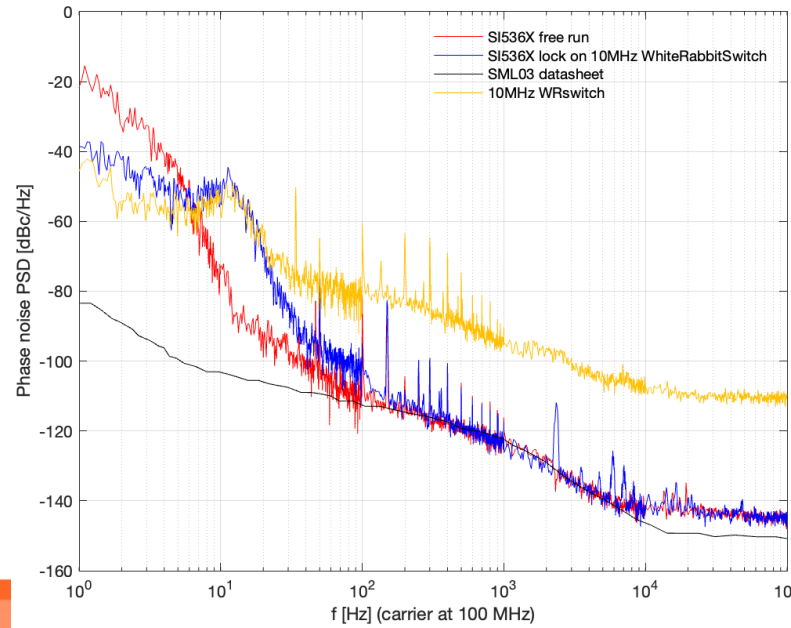
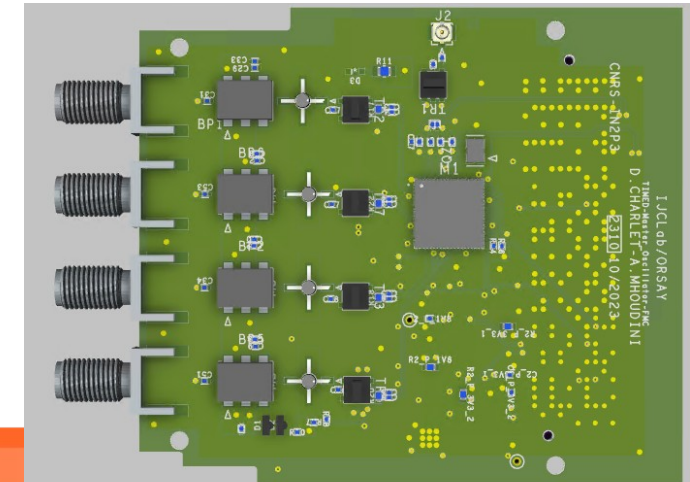
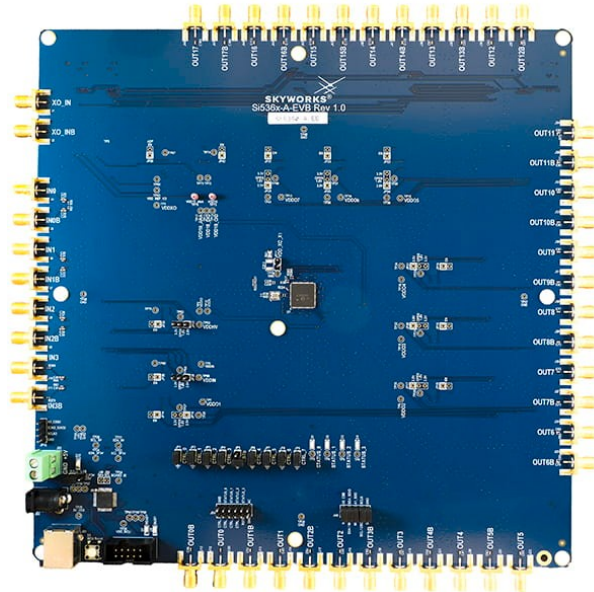


Figure 4.6. 64 fs Jitter for 125 MHz LVDS;
Path=DSPLL+Qdiv



- The motivation to develop the PLL FMC
 - **Generate any frequency disciplined by WR clock**
- Current test with SI536x evaluation board
 - ultra-high-performance jitter attenuator
 - Ultra-low phase jitter (<55 fs typ)
 - 18 outputs 10KHz to 2.75GHz

- FMC_SI536X
 - 4 single ended outputs clock
 - Currently in layout design phase





Conclusion

- Very promising results with IDROGEN board
- A new board version (V4) will be designed due to obsolescence of components
- New functionalities will be available in 2024 : Any frequencies generator, 2 channels ADC 1GSPS 14bits, 4 channels 250MSPS 16bits, LVDS parallel bus
- Development efforts are to be focused on low frequencies
- A lot of improvements are possible on the WR