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► **To cite this version:**

Sara Manna, Cédric Marchand, Damien Deleruyelle, Bastien Deveautour, Alberto Bosio, et al.. 3D VNWFET-Based Standard Cell Library Design Flow: from Circuit and Physical Design to Logic Synthesis. 2024 IFIP/IEEE 32nd International Conference on Very Large Scale Integration (VLSI-SoC), Oct 2024, Tanger, France. pp.1-4, <10.1109/VLSI-SoC62099.2024.10767812>. <hal-04982742>

HAL Id: hal-04982742

<https://hal.science/hal-04982742v1>

Submitted on 7 Mar 2025

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3D VNWFET-Based Standard Cell Library Design Flow: From Circuit and Physical Design to Logic Synthesis

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Abstract—The vertical nanowire field effect transistor (VNWFET) is an emerging technology that promises to improve the sustainability of future transistor scaling beyond the limitations of conventional lateral devices. With its 3D gate-all-around (GAA) architecture, such a technology enables designs with improved energy-efficiency as well as reduced footprint and thus interconnect capacitance. In this work, and based on the compact model of a real VNWFET device, we present the design flow for the generation of a standard cell library starting from the circuit and physical design of logic cells to logic synthesis based on the VNWFET technology. The results on the synthesized benchmark cells, as compared against 45nm and 65nm CMOS libraries, demonstrate a significant decrease in the average dynamic power consumption and delay values up to 71X and 34X respectively, with an average area gain of up to 5X. However, an increase in leakage power consumption (up to 2X on average) was observed.

Index Terms—Emerging Technology, Vertical Nanowires, Gate-all-around field effect transistor, Standard Cell Library, Physical Design, Logic Synthesis

I. INTRODUCTION

The massive increase in the number of smart devices deployed at the edge, from cellphone light sensors to advanced driver assistance systems, has dramatically increased the quantity of generated raw data to be processed. This translates to a need for ever-higher edge computing performance within stringent energy, delay, security and bandwidth constraints. Thus, the design of hardware processors capable of performing complex computational operations is facing many challenges. Improving such processors starts by improving the basic building blocks and circuits at the heart of key operations. During Moore’s law, it was possible to rely on scaling to increase the number of transistors integrated within processors in order to achieve the required performance improvements. However, this approach is now limited by the physical properties of CMOS devices, reflected mainly through the increase in power consumption per chip as devices scale down. Hence, new emerging technologies are under active investigation to overcome these limitations while

maintaining the required performance and constraints. One promising alternative consists of moving toward 3D technologies such as the Vertical Nanowire Field Effect Transistor (VNWFET) [1]; an emerging technology that can be considered a “More Moore” technology. While its operation is based on the same principle as that of the field effect transistor, the semiconductor channel is a nanowire sandwiched between two electrodes. This technology relies on a Gate All Around (GAA) architecture which will give improved electrostatic control, reduced short-channel effect and better scalability opportunities. In this work, we present a complete design flow enabling the successful generation of a standard cell library based on VNWFET technology. This includes the characterization of basic logic cells under different drive strengths as well as the generation and verification of the physical layout of the standard cells. We finally tested our library by synthesizing some logic circuits.

The remainder of this paper is organised as follows: Section II describes the main aspects of the VNWFET technology. Section III details the work carried out toward the generation of the standard cell library while Section IV explains our approach targeting the generation of the physical layouts of the cells present in the library, as well as the verification of our design. Then, Section V shows the results of the logic synthesis. Finally, Section VI concludes our work and summarizes possible future work.

II. VERTICAL JUNCTIONLESS TECHNOLOGY

In this work, we use a VNWFET with a junctionless GAA architecture as shown in Figure 1. It is composed of a homogeneous highly doped nanowire channel patterned into a silicon substrate, which itself is highly doped with boron [1]. In vertical GAA designs, the gate material completely surrounds the nanowire channel, forming a cylindrical control region around the vertical silicon nanowires which improves both power consumption and immunity toward short channel effects. In addition, JL devices [2] can overcome the

complex manufacturing process of the p-n junctions (present in traditional transistors) with the continuous shrinking of the devices. These aspects, along with the device’s vertical orientation help to push the limits of scaled transistors while maintaining the desired performance and reducing footprint. Throughout this work, we consider a device compact model [3] which is based on the actual fabricated device described above and the physics of carrier transport in the junctionless architecture.

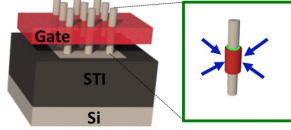


Fig. 1. Vertical gate-all-around junctionless nanowire transistor (JLNT) [4]

III. STANDARD CELL LIBRARY CHARACTERIZATION

For the generated library, we adopt the Liberty (.lib) file format, which includes the timing and physical information relative to the standard cells present in the library while also adopting the nonlinear delay model (NLDP). In this sense, Lookup tables (LUTs) are defined to store timing and power values or constraints. For the generation of the VNWFET logic cell library [5], we designed and characterized four elementary logic cells that should be available in such a library: INV1X1_CStatic_JL1, NAND2X1_CStatic_JL1, NOR2X1_CStatic_JL1 and XOR2X1_CStatic_JL1 where the formalism *OPnXk_Style_Technology* indicates the Boolean operation *OP*, the number of inputs *n* and the number of outputs *k*, as well as the logic design style (i.e., Complementary static logic obtained by using n- and p-type VNWFET) and the technology variant used to implement the cells (i.e. JL nanowire transistor with single gate: JL1). In this context, we carried out SPICE simulations where we used the compact model described in Section II implemented as an executable Verilog-A model for the VNWFET. Throughout this work, and based on the fabricated device and associated model, the gate physical length l_g and the nanowire (NW) diameter d_{nw} are set to 18 nm and 22 nm respectively. However, and in order to study the cells’ behavior under different drive strength, we designed different instances of each cell by varying the number of NWs. For simple cells such as the inverter, we found that a ratio of 1 between the n-type and p-type NW values will assure having a well-matched rise and fall times of the cells. For the other cells, and in order to achieve drive strengths equivalent to that of the inverter, we redefined the number of nanowires by doubling the number of NWs in case of two series transistors. After defining the sets of NW parameters, and verifying the logical functionality of the designed cells, we performed a detailed study of the static and dynamic behavior of these cells. We evaluated their energy consumption and delay while varying the number of NWs used per transistor. We observed that with the increase of the number of NWs and as expected, the static (Figure 2a) and dynamic power increases whereas the delay

TABLE I
LOGIC CELLS PRESENTED IN OUR VNWFET GENERATED LIBRARY AND THEIR AREA VALUES

Logic Cells	n-type #NW	p-type #NW	Area(um ²)
Combinational Cells			
BUF1X1_Static_JL1 Instance	4	4	0.116
	24	24	0.403
	44	44	0.694
	64	64	0.982
INV1X1_Static_JL1 Instance	4	4	0.188
	24	24	0.764
	44	44	1.344
	64	64	1.921
NAND2X1_Static_JL1 Instance	8	4	0.314
	48	24	1.470
	88	44	2.625
NOR2X1_Static_JL1 Instance	4	8	0.401
	24	48	1.441
	44	88	2.712
XOR2X1_Static_JL1 Instance	8	8	0.902
	48	48	3.791
	88	88	6.681
Sequential Cell			
DFFSR	24NW based logic cells & two 4NW INV		4.544

decreases (Figure 2b). In addition to the above combinational logic cells, we also designed a sequential gate, the mandatory D-type Flip Flop (DFF), with synchronous set/reset control signals. Unlike other cells, we only designed one variant, due to convergence limitations in the device compact model. The designed DFF uses mainly 24-NWs logic gates, with two 4-NW INV1X1_CStatic_JL1 gates used as weak inverters in the bistable circuit elements. The current version of the logic cell library is generated by using a commercial tool. The tech library is named JLNT and its cells are summarized in Table I.

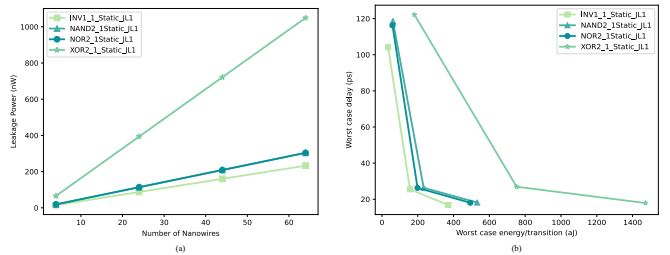


Fig. 2. Plots showing (a) the leakage power and (b) the Pareto Fronts for different logic cells while varying the number of nanowires per VNWFET

IV. PHYSICAL DESIGN AND LAYOUT

The physical design is an important step in the characterization flow of logic cells. It enables an actual estimation of their area values and more accurate timing and power consumption values that can be obtained after the parasitic extraction from such designs. We set about developing an automated physical design flow for logic cells. We based this work on the use of an existing open-source tool [6] which is available as a satisfiability modulo theories (SMT)-based many-tier VFET standard cell (SDC) synthesis framework that provides minimum-sized cell layouts by performing concurrent Place and Route (P&R) of FETs. The SMT tool generates a .conv file, which is essentially a text file

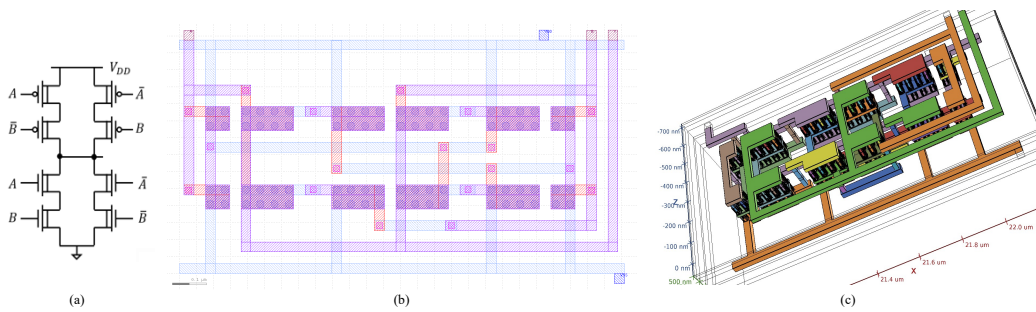


Fig. 3. (a) Schematic (b) layout, and (c) 3D view of a 2-input XOR2 cell

describing the unsized layout template of the desired logic cell. In order to generate a full layout in GDSII file format, sized according to the design rules defined by the technology, we extended the flow of the tool. The first step was to extract from the generated .conv file the necessary information relative to metal layers, transistors, and pins to be transformed into an actual layout. To this end, we developed a Python script which then adapts the layout template to user-defined technology rules and generates the full layout using the GDSII tool kit (Gdstk [7]; C++ library available as a Python module). We then generated a preliminary physical layout for the cells in the standard cell library as described above (in GDSII file format). This allowed us to obtain the height and width of the cells and thus their area values as summarized in Table I. We assure that all cells will have the same height (0.688 μm) to enable conventional row-placement however, their width varies according to the complexity of the cell as well as the number of nanowires used per cell. After that, we were able to generate a Library Exchange File (.lef) containing the physical data for the library cells. In order to verify that the generated layout has no issues and will guarantee the functional logic behavior of the standard cells, we completed a verification test using Global TCAD Solutions (GTS) tools. We chose to carry out the verification on a two-input XOR gate, one of the more complex logic cells. As shown in Figure 3, the cell under test, in addition to the XOR logic functionality (8 NWs per transistor), also has two inverters (4 NWs per transistor) that are used for inverting the two inputs. After completion of the parasitic extraction, a transient analysis was carried out using the generated netlist. This analysis shows that no degradation with the XOR logic functionality was observed. We then carry out a comparative study in order to quantify the impact of parasitic interconnect networks on key performance metrics. Comparing delay and energy per transition figures, we quantify the average increase in delay as 1.72X and energy/transition as 1.13X when considering the parasitic interconnect network.

V. LOGIC SYNTHESIS

A typical Logic Synthesis flow takes as input a circuit model description, usually expressed in a hardware description language (e.g., VHDL) and produces as output the gate level netlist by using building blocks (i.e. logic cells) from

the provided standard cell library. To test our generated library, we first targeted the synthesis of some of the ISCAS-85 benchmarks [8] and the subsequent comparison of the obtained results with conventional CMOS logic cell libraries (i.e. 45 nm free PDK [9] and a 65 nm industrial logic cell library PDK) Table II summarizes the main reports (i.e. the number of cells used to synthesize the target benchmarks, the corresponding physical area values as well as the expected delays) obtained from benchmarks synthesis. We can see that the number of cells used by the 45 nm and 65 nm technologies to synthesize the circuits is smaller than that used by our VNWFET library (i.e. JLNT lib). This is due to the fact that these libraries are full libraries containing much more logic cells than the ones present in our library. However, we can still achieve an average area gain upon the synthesized cells up to 5.57X and 4.53X as compared to the area values of the 45 nm and 65 nm respectively. Also, the VNWFET library was able to improve the delay values up to 3.33X and 2.81X on average as compared to the full 45 nm and 65 nm libraries respectively. Comparing the power values, we can see that the circuits synthesized with the VNWFET library will have a very low dynamic power values as compared to the other two technologies (up to an average decrease of 71X and 34X as compared to the 45 nm and 65 nm technologies). The library also showed a significant improvement on how the dynamic power is distributed among the internal and switching power values. It occupies an average of 32% of the dynamic power instead of 56% and 47% for the 45 nm and 65 nm technologies respectively. However, we realised that

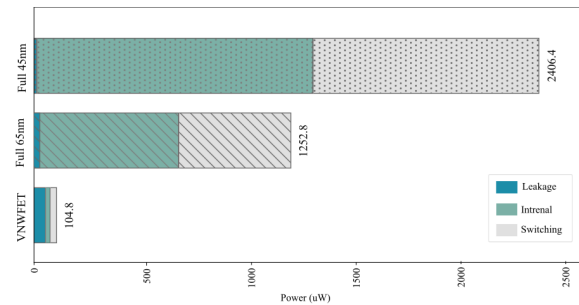


Fig. 4. Detailed power values of benchmark circuit C6288

TABLE II
CELL COUNT SCALABILITY, AREA VALUES AND DELAYS OF SYNTHESIZED CIRCUITS

Benchmark Circuits	Cell Count			Area Values (um ²)			Delay (ns)		
	VNWFET	Full 45 nm	Full 65 nm	VNWFET	Full 45 nm	Full 65 nm	VNWFET	Full 45 nm	Full 65 nm
C432	172	127	78	47.58	293.78	219.44	0.41	1.24	0.83
C499	229	254	142	128.53	726.95	588.12	0.27	0.90	0.87
C1355	193	248	135	120.22	706.77	562.12	0.23	0.81	0.76
C1908	247	268	175	115.65	711.46	556.92	0.38	1.37	1.12
C6288	1503	625	591	712.76	2857.57	2840.76	0.99	3.12	2.52
Processing Element	VNWFET	Rest. 45nm	Rest. 65nm	VNWFET	Rest. 45nm	Rest. 65nm	VNWFET	Rest. 45nm	Rest. 65nm
N2C2 4_bits	229	530	234	152.85	1055.46	624.52	0.087	0.156	0.064
N2C2 8_bits	769	1674	761	432.43	3288.39	1985.36	0.114	0.185	0.071
N2C2 16_bits	2699	5697	2648	1503.02	11074.54	6764.16	0.187	0.235	0.087
N2C2 32_bits	10020	20608	9884	4597.06	39733.28	24717.68	0.335	0.340	0.122

the leakage power dominates the dynamic power for the cells synthesized by our library (an average of 53% of the total power) which is considered to be 2X higher as compared to other technologies. Still, the VNWFET gave the lowest total power i.e. an average of 26X and 13X decrease in total power consumption as compared to the 45 nm and 65 nm libraries respectively. For simplicity, only the detailed power values of one benchmark circuit is shown in Figure 4.

After that, we moved toward the synthesis of our Neural Network Compute Cube (N²C²) [10] which is a processing element that is capable of performing multiplication-accumulation (MAC) operations and can be used for neural networks. We synthesized 4 different instances of the N²C² blocks with data sizes of 4,8,16 and 32 bits aiming to assess the scalability of VNWFET in comparison to traditional CMOS technology. For this part, and due to the fact that our library contains only basic cells, we realised that it would be interesting to constrain the 45 nm and 65 nm. Therefore, we restricted the 45 nm library to only the logic cells present in the VNWFET library whereas we only restricted some of the 65 nm cells. The obtained reports after the synthesis of the N²C² benchmarks are also shown in Table II. Comparing the cell count We can see that the synthesized N²C² circuits by our library outperforms the restricted 45nm library, but uses almost the same count as that of the restricted 65 nm library. However, taking into account the physical cost of the synthesized benchmark circuits, we can clearly see that the VNWFET library provides the lowest area values among the other libraries. Based on the latency reports, we can observe that the VNWFET performs better than the restricted 45 nm however it performs poorly as compared to the 65nm restricted library. This observation contradicts what we observed for the above benchmark circuit; this could be due to the fact the N²C² cells are composed of both sequential and combinational cells and still the restricted 65 nm library contains much more cells than our library. For the power consumption values we observe the same trend; i.e. both versions of 45nm as well as the restrained 65nm always perform worse than that of the VNWFET version in terms of the total power consumption. When looking at the details however, we triggered the same behavior of the synthesized benchmarks, i.e. the leakage power of the VNWFET library represents its highest consumption.

VI. CONCLUSION AND FUTURE WORK

In this work, we presented a complete flow targeting the generation of a standard cell library based on a real VNWFET device. We detailed our approach starting from the logic cells characterization to the physical design and verification methodology as well as the generation of the library .lef file. Finally, we were able to use our generated library to synthesize well-known benchmark circuits and our compute cube then to compare the obtained results with well know CMOS technologies. Our library generally showed improvements in terms of delay, area, dynamic power and short-channel effect values however it showed an increase in the leakage power values. In fact, the increase in leakage power values is expected with more advanced technologies due to the lower threshold voltage and shrunked devices. Further investigations to be done on the obtained leakage power values,

ACKNOWLEDGMENT

This work has been funded by the European Union's Horizon 2020 research and innovation programme under grant agreement No 101016776 (FVLLMONTI).

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