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Introducing 28-nm technology in Microwind

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Abstract: This paper describes the key performance parameters of the CMOS 28-nm technology and its implementation in Microwind. We focus on the supply voltage, the high-k metal gate, ION/OFF trade-off, process variants, device options and general rules such as the contacted gate pitch, metal pitch and principles for device implementation. The design of basic gates such as inverter, RAM, DRAM, ring oscillator is illustrated along with their characteristics.
Keywords: CMOS design, 28-nm, cell design, Microwind

Introduction

The announcement of the construction of nano-scale semiconductor factories in India [Moore 2024], together with a 15 billion $ investment from the Indian government is an opportunity to highlight the strategical significance of domestic manufacturing of integrated circuits, in the hope of becoming less dependent of IC manufacturing giants such as TSMC, Samsung, UMC, SMIC, etc. Although having less attractive performances that FinFET and Nano-sheet technologies (Figure 1), the 28-nm node still plays a key role for low-cost ICs with non-critical performances, such as automotive, communications and consumer electronics.

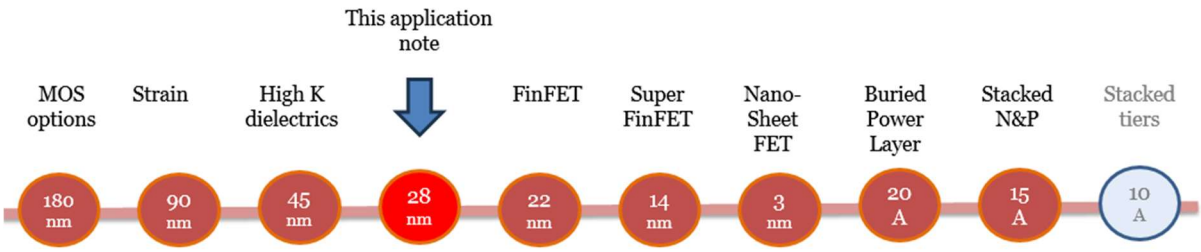


Figure 1 : 28-nm node situated in the technology roadmap for semiconductors

Technology node	Year of introduction	Key innovations	Application note
180 nm	2000	Cu interconnect, 6 metal layers	
130 nm	2002	Low-k dielectric, 8 metal layers	
90 nm	2003	SOI substrate	[Sicard 2005]
65 nm	2004	Strain silicon	[Sicard 2006]
45 nm	2008	2nd generation strain, 10 metal layers	[Sicard 2008]
32 nm	2010	High-K metal gate	[Sicard 2010]
28 nm	2011	High-K metal gate	This application note
20 nm	2013	Double patterning, 12 metal layers	[Sicard 2014]
14 nm	2015	FinFET	[Sicard 2017]
10 nm	2017	FinFET, double patterning	[Sicard 2017]
7 nm	2019	FinFET, quadruple patterning	[Sicard 2017]
5 nm	2020	FinFET enhancement, EUV	[Sicard&Trojman 2021]
3 nm	2021	Nano-Sheet FET, EUV	[Sicard&Trojman 2021b]
2 nm /20A	2024	Nano-Sheet, Buried power rail, nano Through-Silicon-Via	[Sicard&Trojman 2022]
1.5 nm /15A	2027	Nano-Sheet Complementary FET	To appear 2024
1 nm /10A	2030	Nano-Sheet Stacked Complementary FET	

Table 1: Most significant technology nodes introduced over the past 20 years and prospective vision for 2030.

India's semiconductor journey began with the Semiconductor Laboratory (SCL) in Mohali, a key facility established in 1983 and later integrated into ISRO in 2005. SCL specializes in 0.18µm (180nm) technology, producing critical components for space and defense applications. While reliable, this technology is outdated for modern demands, highlighting the need for advanced capabilities. The laboratory has contributed to the development of Application-Specific Integrated Circuits (ASICs), microprocessors, and other critical components that are essential for India's self-reliance in high-tech and defense sectors.

To modernize its semiconductor ecosystem, India is setting up fabs with 28nm process technology, leveraging SCL's expertise to transition into global competitiveness. This move aims to reduce reliance on imports, meet market needs, and position India as a major player in the high-tech sector.

Targeted components include microprocessors, microcontrollers, as well as power management units for which the technology provider PSMC (Taiwan) is one of the world leaders. The availability of nano-CMOS industry on the Indian soil should also benefit to the academic and research community, which relied up to now on semiconductor processes available mainly in Taiwan (TSMC, UMC) or around the world (Imec, Global Foundries) through dedicated services such as Europractice [Europractice 2024]. More than 3,00,000 jobs should be created to support the fab and ancillary units, which should boost student interest to the electronics field.

The purpose of the application note is to analyze the scientific literature on the 28-nm node and tune the educational software Microwind to that specific technology, by defining key parameters such as the supply voltage, device performances, general design rules to situate the design performances as compared to less and more advances nodes (See Table 1).

In part 2, we focus on the transistor performances, including a focus on ION/IOFF trade-off, N-channel & P-channel device characteristics according to the 3 main variants: high-voltage devices for input/outputs, low-power device for general purpose and high-performance device.

In part 3, we detail the cell design, with the illustration of the gate pitch, the increased cell density, and general strategy for N-P placement/routing and interconnect capacitance. Part 4 illustrates designs made with 28nm node like inverter, ring oscillator, 6-T SRAM, DRAM. In part 5 we put our views on selection of 28nm technology node by India.

Transistor performances in 28-nm technology

Key features

Several 28-nm processes have been introduced by various manufacturers TSMC (Taiwan) [Wu 2009], Samsung Foundry (South Korea) [Fukutome 2011], Global Foundries (USA) [Capodieci 2012], PSMC (Taiwan), SMIC (China), Intel (USA), STMicroelectronics (France) [Arnaud 2011], Renesas Electronics (Japan) [Tomimatsu 2009], Texas Instruments (USA) [Gammie 2011] addressing different types of applications. Some of the key features of the 28-nm technologies from various providers are given in Table 2.

Parameter	Value Range
V_{DD} (V)	0.6 ~ 1.1
Effective gate length (nm)	25-35
Ion N (µA/µm) at 1V	500-1010
Ion P (µA/µm) at 1V	265-600
Ioff N (nA/µm)	0.2-200
Ioff P (nA/µm)	0.2-200
Gate dielectric	HfO_2, SiON
# of metal layers	6-11
Interconnect layer permittivity K	2.4-3.0

Table 2: Key features of the 28 nm technology

Compared to 45-nm technology, most 28-nm technologies offer [Capodieci 2012]:

- 50 % increase in switching performance
- 50 % less power consumption
- 2 times higher density

MOS types

Some 28-nm technologies comprise as much as 10 types of MOS devices (i.e. 20 devices in total) [Chidambaram 2010]. In Microwind, only three types of MOS devices (3 nMOS, 3 pMOS, 6 MOS devices in total) exist in the 28-nm technology:

- The low-leakage MOS is the default MOS device,
- The high-speed MOS has higher switching performance, thanks to a shorter effective channel length, at the price of a much higher leakage.
- The high voltage MOS used for input/output interfacing. In Microwind's cmos28 nm rule file, the I/O supply is 1.8 V. Some foundries also propose 2.5 V and 3.3 V interfacing.

The main objective of the low leakage MOS is to reduce the *Ioff* current significantly, that is the small current that flows between drain and source with a zero-gate voltage (See Table 2). The price to pay is a reduced *Ion* current. The designer has the choice of using high-speed MOS devices, which have high *Ioff* leakages but large *Ion* drive currents. More details follow.

N-channel MOS device characteristics

The 28-nm technology uses a stack of high-k dielectric and metal gate (TiN). Layouts and cross-sections of two varieties of n-channel MOS devices are given in Fig. 2 and 3, where the high-speed device has a reduced channel length (26 nm instead of 32 nm). Although the high speed NMOS has a slightly shorter channel, it is drawn with the same size as the low leakage NMOS. The nMOS gate is capped with a specific silicon nitride layer that induces lateral tensile channel strain to improve electron mobility. The pMOS strain is based on SiGe diffusion [Chidambaram 2010] [Liang 2011]. Key parameters for the MOS devices are shown in Table 3.

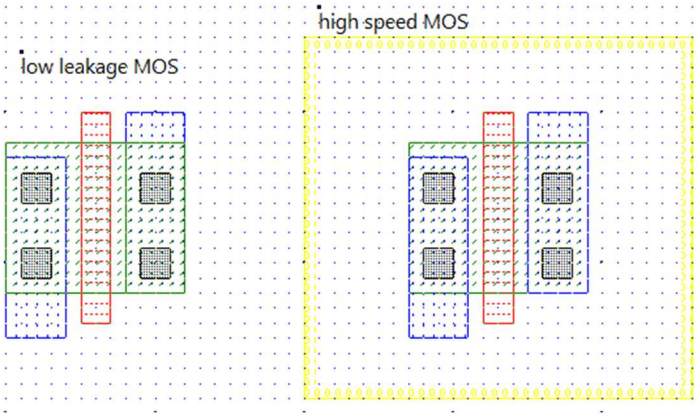


Figure 2: Layout of the low-leakage and high-speed MOS devices (basic_MOS.MSK). Dimensions are identical (2 lambda length).

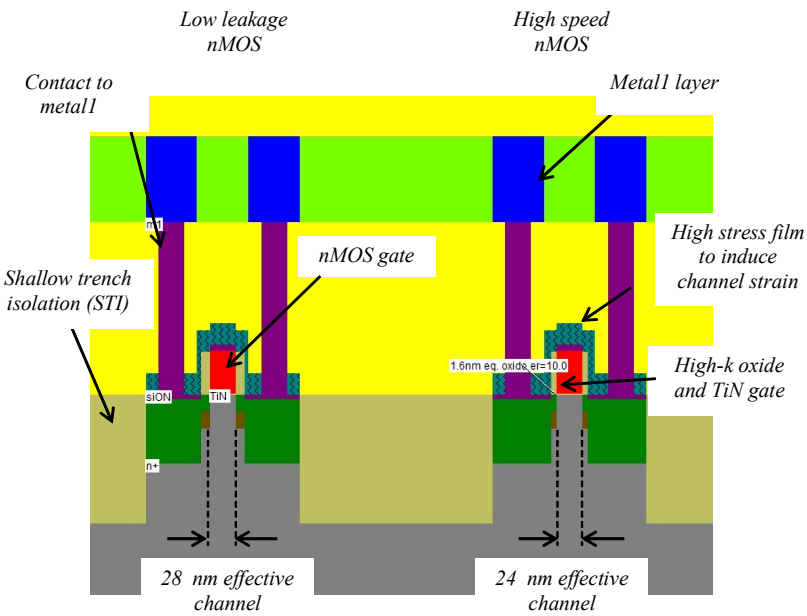
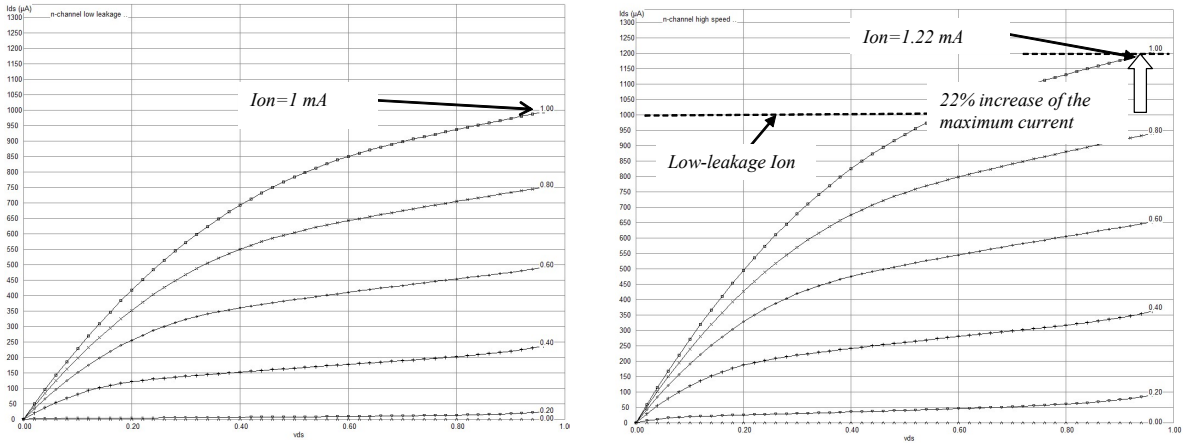


Figure 3: Cross-section of the nMOS devices (Mos/allMosDevices.MSK)

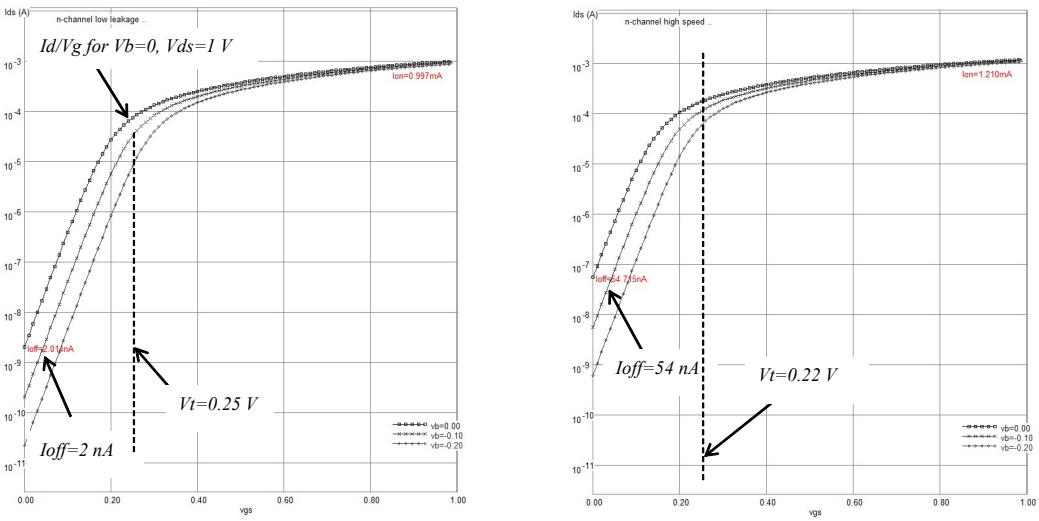
Parameter	NMOS Low leakage	NMOS High speed
Drawn gate length (lambda)	2	2
Drawn gate length (nm)	30 nm	30 nm
Effective gate length (nm)	30 nm	26 nm
Threshold voltage (V)	0.25	0.22
Ion (mA/µm) at VDD=1.0V	1.00	1.22
Ioff (nA/µm)	2	54

Table 3: nMOS parameters featured in the CMOS 28-nm technology provided in Microwind v3.9



(a) Low leakage W=1µm, Leff= 30nm *(b) High speed W=1µm, Leff= 26nm*

Figure 4: Id/Vd characteristics of the low leakage and high speed nMOS devices. Note that L_{drawn}=30nm in both cases. The effective length is significantly smaller for the high-speed MOS



(a) low leakage MOS (Leff=30 nm) *(b) high speed MOS (W=1 µm, Leff=26 nm)*

Figure 5: Id/Vg characteristics (log scale) of the low leakage and high-speed nMOS devices

The I/V characteristics of the low-leakage and high-speed MOS devices (Figs. 4 and 5) are obtained using the MOS model BSIM4 (See [Sicard2007] for more information about this model). The I/V characteristics reported in Fig. 5 demonstrate that the low-leakage NMOS has a drive current capability of around 1.0 mA for W=1.0 µm at a voltage supply of 1.0 V (1.0 mA/µm).

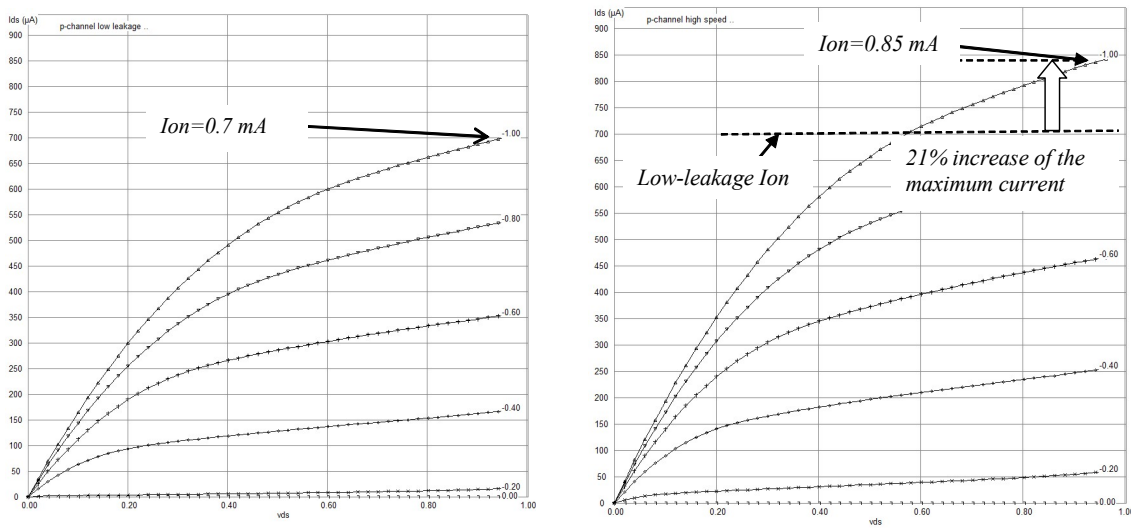
For the high speed NMOS, the effective channel length is slightly reduced (26 nm instead of 30 nm), to achieve a drive current around 1.22 mA/µm. The drawback associated with this high current drive is the leakage current which rises from 2 nA/µm (low leakage NMOS) to 54 nA/µm (high speed NMOS), as seen in the Id/Vg curve at the X axis location corresponding to Vg= 0 V (Fig. 5).

P-channel MOS device characteristics

The PMOS drive current in CMOS 28-nm technology (Ion in Table 4) is around 700 µA/µm for the low-leakage MOS and up to 850 µA/µm for the high-speed MOS. The leakage current is around 2 nA/µm for the low-leakage MOS and nearly 44 nA/µm for the high-speed device.

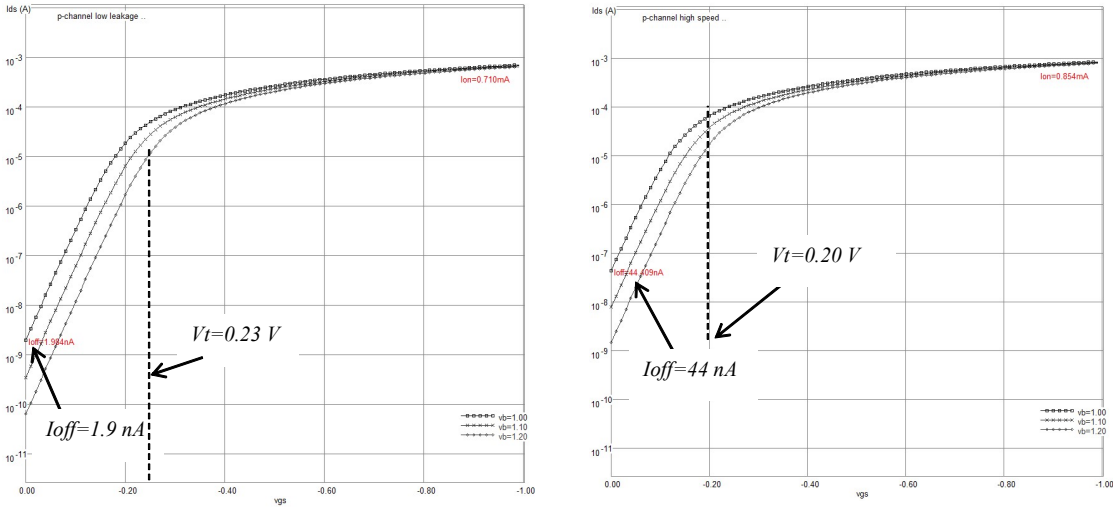
Parameter	**pMOS Low leakage**	**pMOS High speed**
Drawn gate length (lambda)	2	2
Drawn gate length (nm)	30	30
Effective gate length (nm)	30	26
Threshold Voltage (V)	-0.25	-0.20
Ion (mA/µm) at VDD=1.0V	0.70	0.85
Ioff (nA/µm)	2	44

Table 4: pMOS parameters featured by the 28-nm CMOS technology provided in Microwind v3.9



(a) Low leakage W=1µm, Leff= 30nm *(b) High speed W=1µm, Leff= 26nm*

Figure 6: Id/Vd characteristics of the low leakage and high speed pMOS devices. Note that L_{drawn}=30nm in both cases. The effective length is significantly smaller for the high speed MOS



(a) low leakage MOS (Leff=30 nm) *(b) high speed MOS (W=1 µm, Leff=26 nm)*

Figure 7: Id/Vg characteristics (log scale) of the low leakage and high-speed pMOS devices

Cell Design

Surface area benefit

Scaling to smaller technology nodes is synonymously done to achieve area benefit, thereby increasing profits of the fab. Shifting to 28nm from 45nm technology node offers notable surface area optimization by reducing feature sizes and increasing integration density. Relative to 45nm node [Sicard 2008], the 28nm provides up to 50% scaling benefits, that is a ~100% density increase, up to 50% increased speed and 50% reduction in energy/switch [Capodieci 2012].

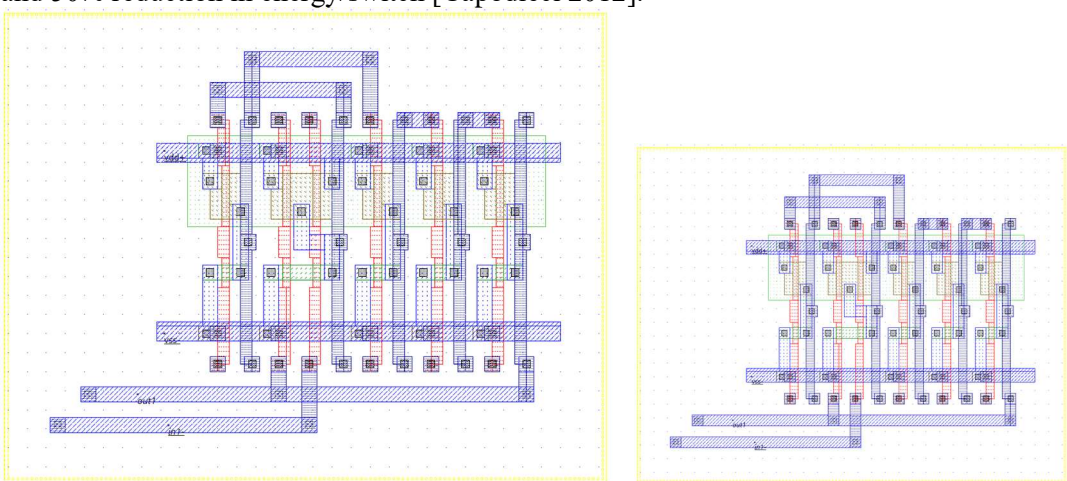


Figure 8: Left layout is ring oscillator in 45nm with lambda as 20nm; right layout is same design with 28nm with lambda as 15nm, which is 45% surface area gain.

Metal layers

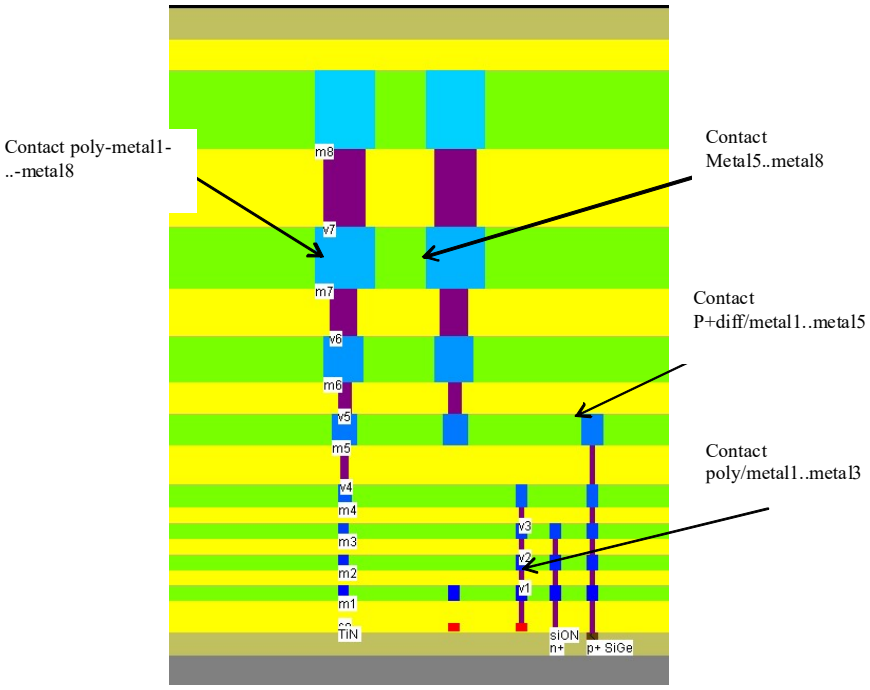


Figure 9: Examples of layer connection using the complex contact command from Microwind (Interconnects /Contacts.MSK)

Each metal layer is embedded into a low dielectric oxide (referred to as "interconnect layer permittivity K" in Table 2), which isolates the layers from each other. A cross-section of a 28-nm CMOS technology is shown in Fig. 9. In 28-nm technology, the layers *metal1...metal4* have almost identical characteristics. Concerning the design rules, the minimum width *w* of the interconnect is 3 λ (3 x 15 nm = 45 nm) and the minimum spacing is 4 λ (4 x 15 nm = 60 nm). The metal pitch is 7 λ, that is 105 nm. Layers *metal5* and *metal6* are a little thicker and wider, while layers *metal7* and *metal8* are significantly thicker and wider, to drive high currents for power supplies. The design rules for *metal8* are 15 λ (0. 225 µm) width, 20 λ (0.3 µm) spacing.

Interconnect Capacitance

An average value of 0.2 fF/µm is found in the literature for metal 2 capacitance. Some details are given by TSMC [Wu 2009]. The usual setup consists of routing the lower and upper metal layers (resp. metal 1 and metal 3) at minimum pitch, as shown in Fig. 10, which is close to a realistic case. Consequently, the metal2 capacitance is much higher compared to when it is routed alone without surrounding metal interconnects. Note that the crosstalk capacitance, i.e. the capacitance between adjacent wires, is also quite large at minimum pitch.

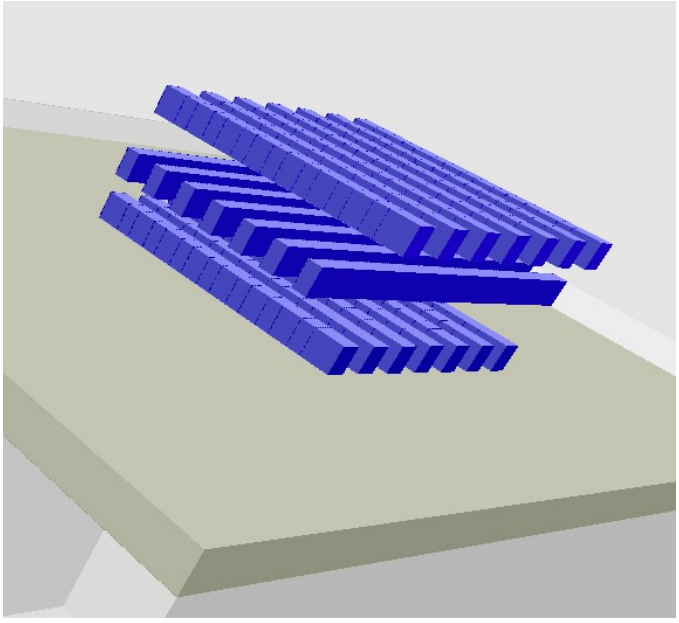


Figure 10: The interconnect capacitance is evaluated assuming that multiple wires are running below and above the layer under consideration (Interconnects > Metal1-3.MSK)

Designing in 28 nm technology

Inverter

Designing layout design can be easily done using Microwind software. The simplest way to create a CMOS inverter is to generate both n-channel MOS an p-channel MOS devices using the cell generator provided by Microwind. The advantage of this approach is to avoid any design rule error. The corresponding menu is reported below. You can generate an n-channel or p-channel device. By default, the proposed length is the minimum length available in the technology (2 lambda), and the width is 10 λ. In 28 nm technology, where lambda is 15nm, the corresponding size is 30 nm for the length and 150 nm for the width.

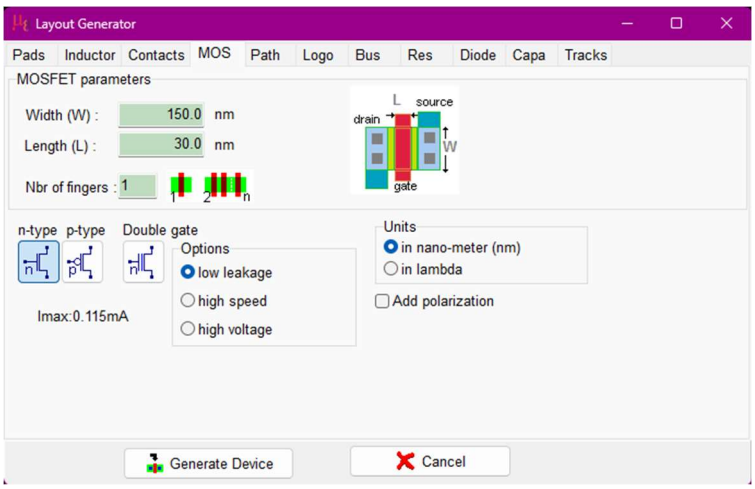


Figure 11: Using the MOS generator to add n-channel and p-channel MOS devices on the layout

The design starts with the implementation of one nMOS and one pMOS, as shown in figure 12. Using the same default channel width (0.15µm in CMOS 28nm) for nMOS and pMOS is not the best idea, as the p-channel MOS switches half the current of the n-channel MOS. The origin of this mismatch can be seen in the general expression of the current delivered by n-channel MOS devices (equation 4-1) and p-channel MOS devices (equation 4-2).

$$Ids(Nmos) \approx \varepsilon_0 \varepsilon_r \frac{\mu_n}{TOX} \frac{W_{Nmos}}{L_{Nmos}} f(Vd,Vg,Vs,Vb) \qquad \text{(Equ. 4-1)}$$

$$Ids(Pmos) \approx \varepsilon_0 \varepsilon_r \frac{\mu_p}{TOX} \frac{W_{Pmos}}{L_{Pmos}} f(Vd,Vg,Vs,Vb) \qquad \text{(Equ. 4-2)}$$

If *Wnmos=Wpmos* and *Lnmos=Lpmos*, *Ids(Nmos)* is proportional to µn while *Ids(Pmos)* is proportional to µp. Typical mobility values are:

$\mu_n = 0.028 m^2/v.s$ for electrons

$\mu_p = 0.020 m^2/v.s$ for holes

Consequently, the current delivered by the n-channel MOS device is 40% more than that of the p-channel MOS. Usually, the inverter is designed with balanced currents to avoid significant switching discrepancies. In other words, switching from 0 to 1 should take approximately the same time as switching from 1 to 0. Therefore, balanced current performances are required.

There are several techniques to counterbalance the intrinsic mobility difference: increase the nMOS channel length (left of figure 12), decrease the nMOS channel width (middle), or increase the pMOS channel width (right side). The main drawback of the design of figure 12 (left) is the spared silicon area.

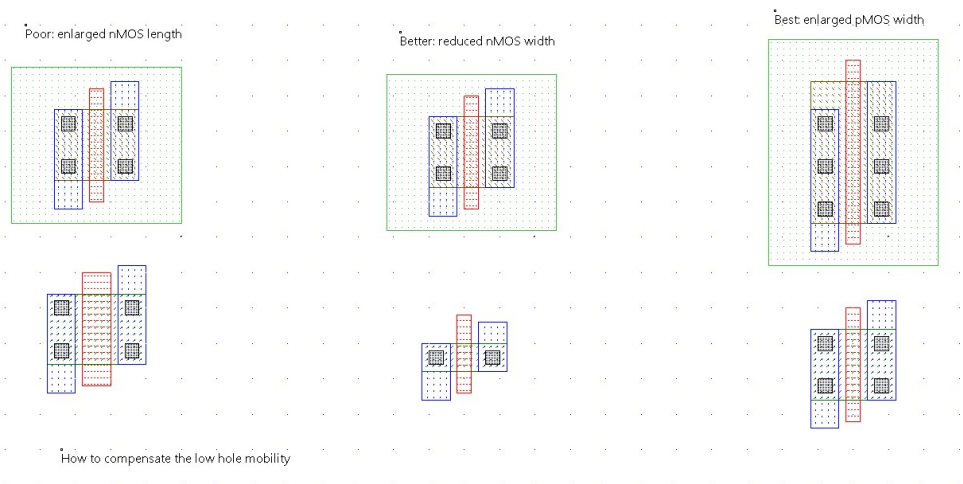


Figure 12: Three techniques to compensate the poor hole mobility (invSizing.MSK)

The design in the middle is equivalent, but consumes less silicon space, additionally it not practical to have varied length device on same column. However, reducing the nMOS width slows down the switching. The best approach (right) consists in enlarging the pMOS width. Its *Ion* current is doubled, and becomes comparable to the nMOS current. The behavior will be balanced in terms of switching speed.

Connection between Devices

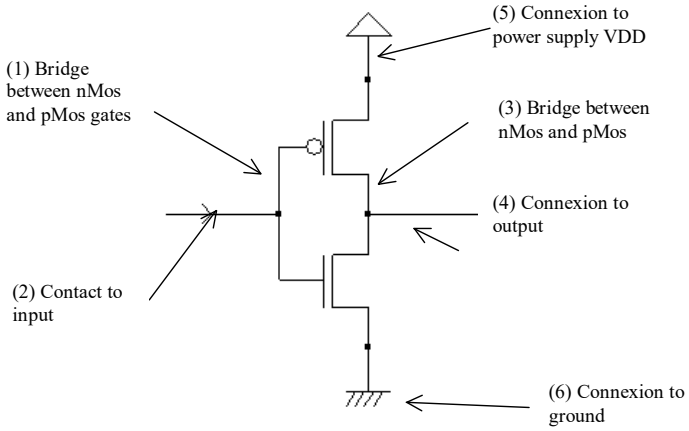


Figure 13: Connections required to build the inverter (CmosInv.SCH)

Within CMOS cells, metal and polysilicon are used as interconnects for signals. Metal is a much better conductor than polysilicon. Consequently, polysilicon is only used to interconnect gates, such as the bridge (1) between pMOS and nMOS gates, as described in the schematic diagram of figure 13. Polysilicon is rarely used for long interconnects, except if a huge resistance value is expected.

In the layout shown in figure 14, the polysilicon bridge links the gate of the n-channel MOS with the gate of the p-channel MOS device. The polysilicon serves as the gate control and the bridge between MOS gates. The right side of figure shows completed inverter with

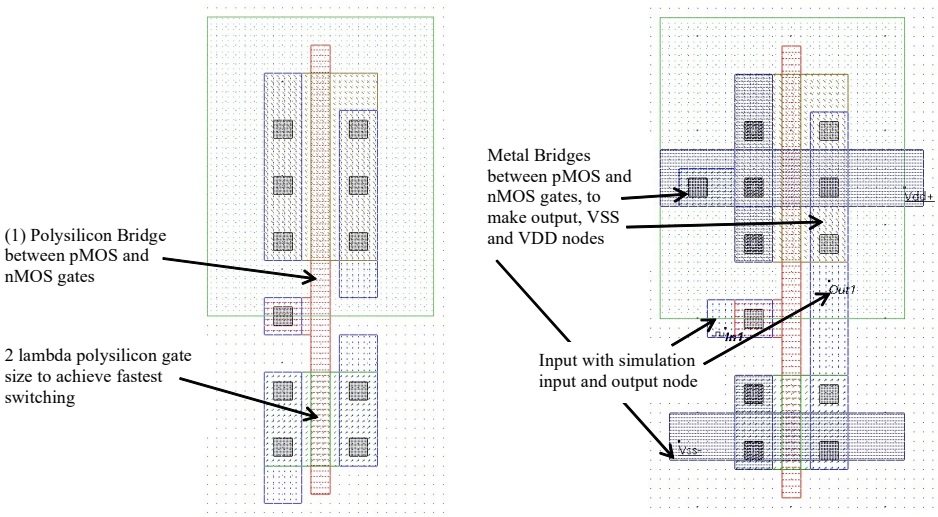


Figure 14: Polysilicon bridge between nMOS and pMOS devices (InvSteps.MSK)

Inverter Simulation

The inverter made as shown in figure 14 was simulated at layout level in Microwind software using 28nm technology. The inverter was applied with square clock of 1ns period. We recorded the inverting output of the inverter, which is shown in figure 15. The measured corresponding parameters like output delays, power consumption.

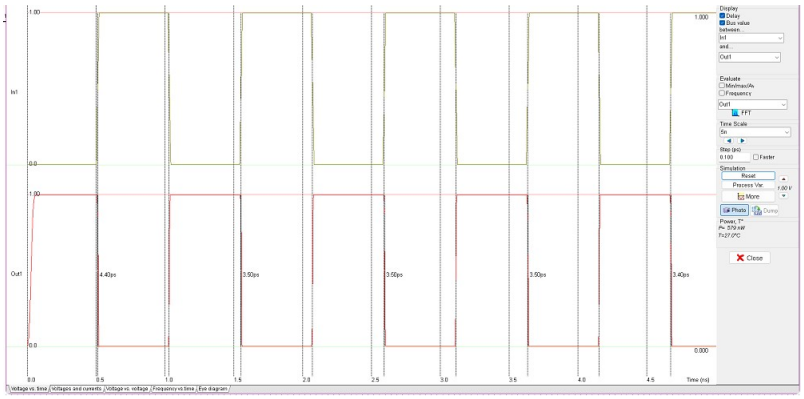


Figure 15: Inverter voltage vs time simulation lot with power as 580nw for entire window.

Ring oscillator

Comprising an odd number of inverters connected in a closed loop, ring oscillators are pivotal for applications ranging from clock generation to the characterization of process variations in semiconductor fabrication. We constructed a ring oscillator using inverts connected back-to-back as seen in fig. 16. Rings oscillations offer a simple but constructive way to analyze impact of process parameters and loading effects; which will be depicted ahead with min/max impact of parameters.

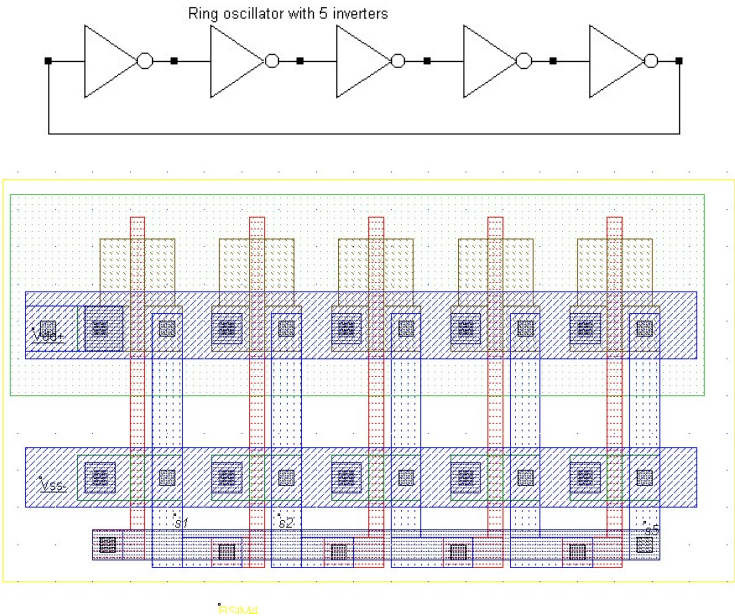


Figure 16: Schematic diagram and layout of the ring oscillator used for simulation (INV5.MSK)

Ring Inverter Simulation

Our ring oscillator is made using 5 inverters, as shown in Fig. 16 (INV5.MSK), has the property of oscillating naturally. It was simulated at layout level in Microwind software using 28nm technology. We also recorded the oscillating outputs of the circuit for various technologies and measure their corresponding frequencies for comparison. The period and frequency of the output signal are displayed in the analog simulation window (Fig. 17); if the "Frequency" box is selected when running simulation, you may observe the frequency of oscillation to be initially lower, increasing gradually with time and settling to the stable values reported above. Therefore, it is important to run the simulations for long enough so that the correct (stable) oscillating frequency can be observed.

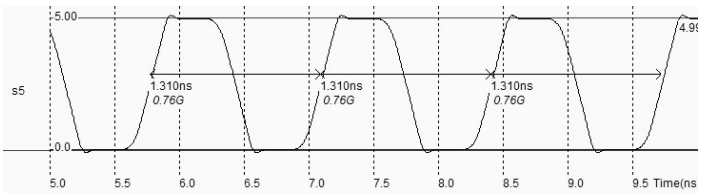
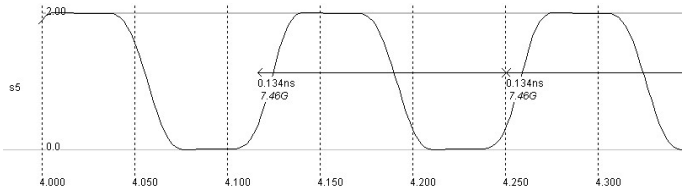
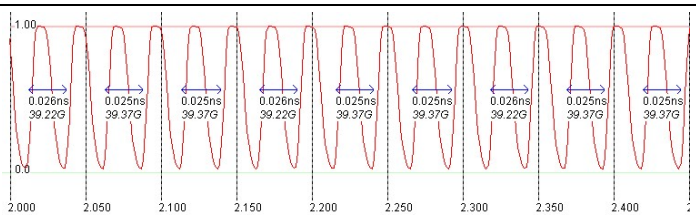
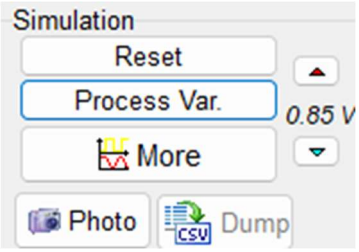
Technology	Supply	Oscillation	Chronograms
0.8 µm	5 V	0.76GHz	
0.18 µm	2 V	7.5 GHz	
28 nm	1.0 V	39 GHz (high speed option)	

Figure 17: Oscillation frequency improvement with the technology scale down (Inv5.MSK)

Process Variations (PVT)



Microwind 3.9 gives access to "Process-Voltage-Temperature" (PVT) simulation through the command **Simulate → Simulation Parameters → Process Variations**. Direct access from the simulation waveform window is also possible using the button **"Process Var.".** The most usual simulation consists of simulating extreme situations (Min and Max), as compared to typical conditions, as shown in Fig. 18. In Fig. 18, nearly a factor of 3 is observed between the performances under Min and Max situations.

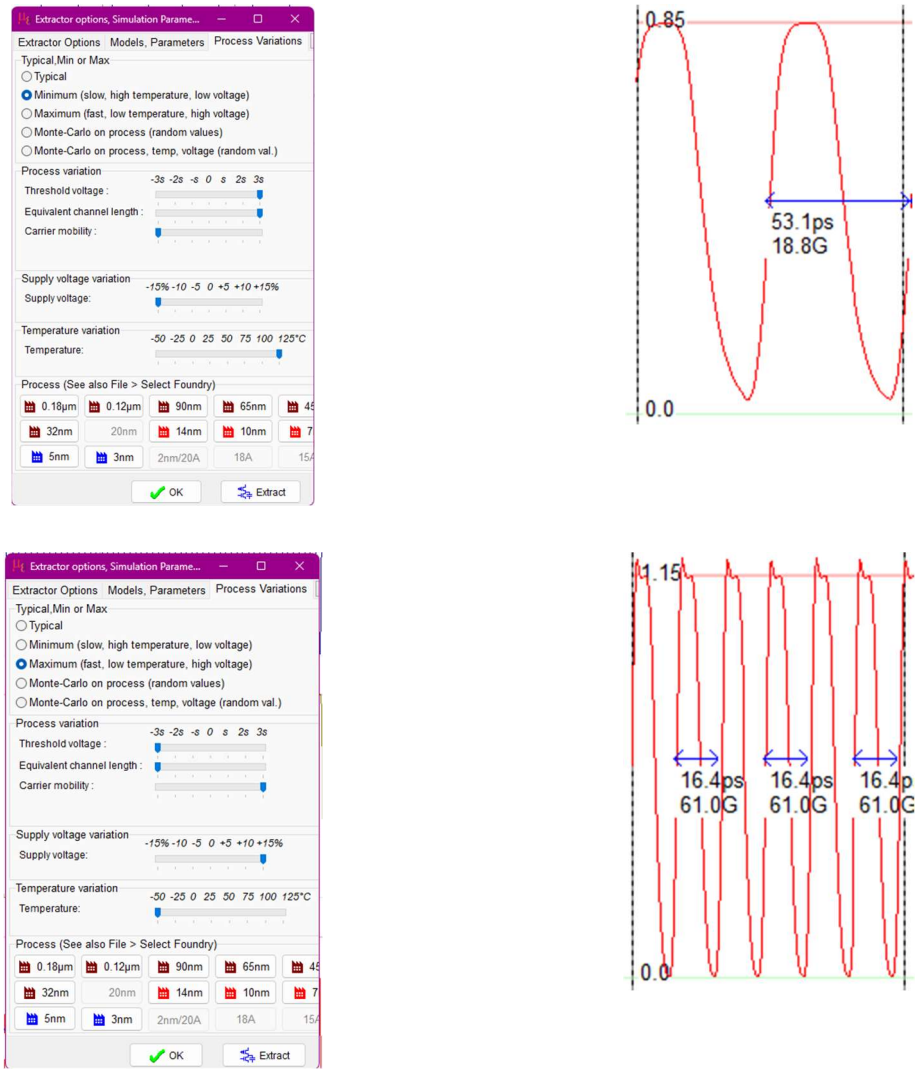


Figure 18: PVT Min-Max simulation showing x3 variation in switching performances

6-transistor static RAM

One of the most representative designs for comparing technology nodes is the static RAM cell designed using 6 transistors (6T-SRAM). In our implementation in Microwind (see Fig. 19), the layout size is 0.555 x 0.24 µm, with a surface area of 0.133 µm^2, which is slightly smaller than the published data ([Wu 2009] 0.155um2 6-T SRAM cell by TSMC). Note that the layout strictly obeys the basic design rules. Most contacts are shared with neighboring cells: the VSS, VDD contacts, the Select and Data lines. It is usual to find more aggressive layout design rules in RAM cell designs, to further decrease the cell area.

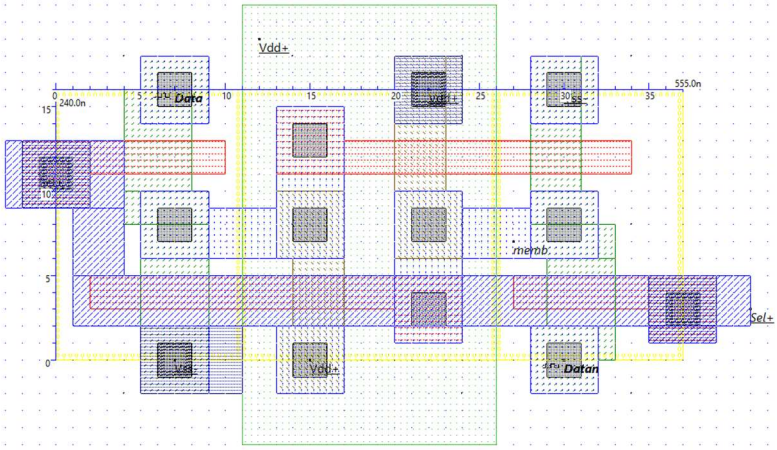


Figure 19: The 6-transistor RAM layout using 28-nm design rules (Ram6T_28nm.MSK)

DRAM

At its core, DRAM leverages the charge storage capabilities of capacitors, but it is the integration with CMOS technology that has dramatically enhanced its efficiency, scalability, and cost-effectiveness. Fig. 20 shows a embedded capacitor with for DRAM; thereby offering higher densities for memory application. The bit line is routed in metal2, and is connected to the cell through a metal1 and diffusion contact. The word line is the MOS gate. On the right side, the storage capacitor is a sandwich of conductor material connected to the diffusion, a thin oxide with high K (dielectric permittivity) and a second conductor that fills the capacitor and is connected to ground by a contact to the first level of metal. The capacitance is around 10 fF.

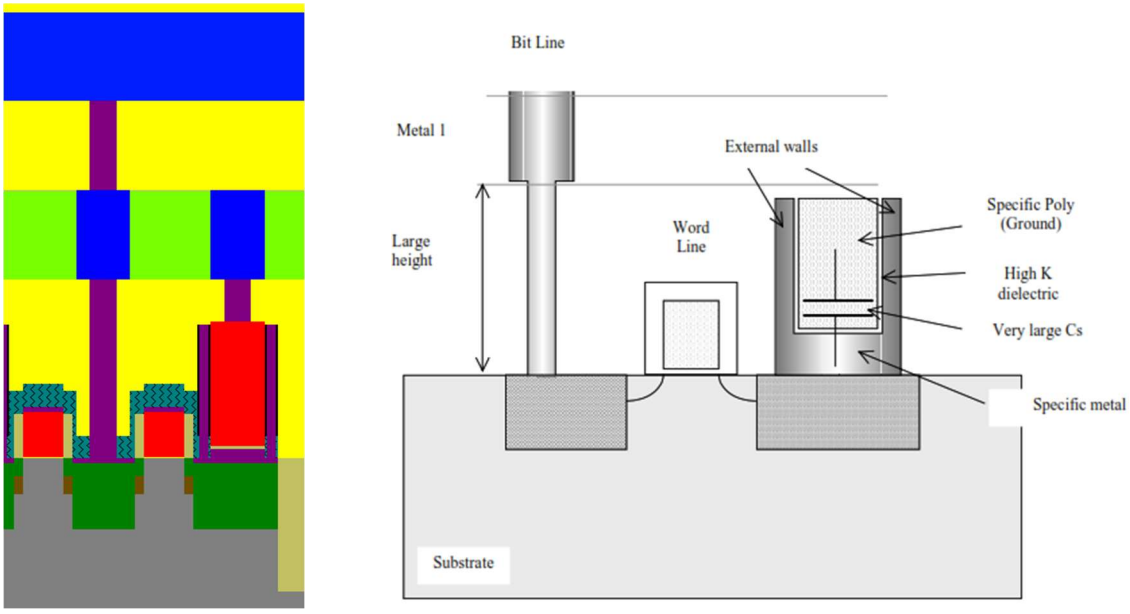


Figure: 20 Embedded DRAM

Indian 28nm technology node

India's choice of the 28nm technology node for its semiconductor manufacturing initiative is driven by strategic, economic, and market factors, making it a practical and impactful decision over advanced nodes like 7nm or 5nm. Here is why:

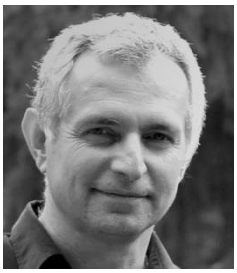
- **Lower Complexity, Faster Setup:** This is first step, hence it needs to be easy going. Manufacturing at 28nm involves less complexity compared to advanced nodes, ensuring faster setup and easier scaling of operations.
- **High Demand for Mature Nodes:** The 28nm node is widely used in industries like automotive, IoT, telecommunications, and consumer electronics; making it a lucrative market choice and offering products at lower cost.
- **Economic Feasibility:** Advanced nodes like 5nm or 3nm require significantly higher investments in equipment, expertise, and infrastructure; hence starting with 28nm allows India to start without steep investment costs.
- **Versatility across Applications:** The 28nm node is ideal for a variety of applications, it balances performance, power efficiency, and production costs effectively, catering to various needs of 5G to industrial electronics.
- **Alignment with Expertise:** India's experience with the 180nm technology at SCL provides a stepping stone for 28nm, avoiding the steep learning curve. It ensures a smoother adaptation of existing skills and resources.
- **Global Relevance:** Even with the availability of smaller nodes, many industries continue to rely on mature nodes like 28nm due to their cost-performance trade-offs. This ensures India's semiconductor products remain relevant in the global market.

By focusing on 28nm, India is taking a strategic approach that balances current market demand, economic viability, and technical feasibility, while laying the groundwork for future advancements.

Conclusions

This application note has illustrated the few trends in CMOS technology and introduced the 28-nm technology generation, based on technology information available from integrated circuit manufacturers. A set of specific topics has been addressed, including the new gate dielectric, gate stack and the strained silicon technique for enhanced mobility, and the 28-nm process variants. N-channel and P-channel MOS device characteristics have been presented, as well as an illustrative study of a circuits like inverters, RAMs, ring inverter oscillator was done for 28nm technology node. Finally, selection of 28nm technology node for India was discussed.

About the authors



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