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Development and test of a superconductor-to-semiconductor interface circuit for high data rates

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Introduction

Superconducting analog to digital converters and network switches are the first demonstrated digital systems based on RSFQ technology. Their superconducting electronics is operating at a very high speed. One of the main issues in the system design is the data interface from RSFQ to CMOS electronics.

Fast interface circuits require a high signal to noise ratio, achievable with reduced noise of the amplifier and with a higher RSFQ output voltage. In this work we demonstrate new solutions for both points:

- a RSFQ voltage doubler together with a SFQ/dc converter to increase the output voltage
- a cryogenic low noise p-HEMT amplifier directly connected to the RSFQ chip

The combination of both interface circuits is analysed through high-speed measurements.

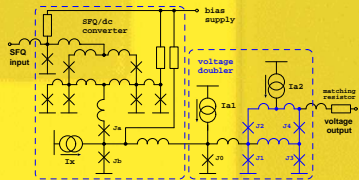


Figure 1: Schematic diagram of the RSFQ output driver.

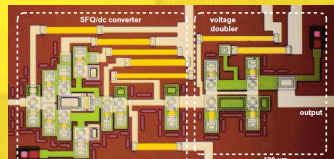


Figure 2: Chip photograph of the RSFQ output driver.

RSFQ output driver

- Fabrication: FLUXONICS Foundry
 $J_c = 1 \text{ kA/cm}^2$
- Layout size: $400 \times 200 \mu\text{m}^2$
- Output voltage: $360 \mu\text{V}$ average, $438 \mu\text{V}$ maximal
- Operation speed: larger than 10 GHz

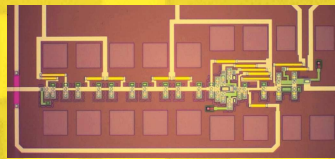


Figure 3: RSFQ test circuit including dc/SFQ-converter, Josephson Transmission Line (JTL) and output driver.

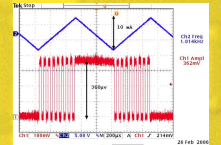


Figure 4: Low speed measurement of the output interface with a room temperature amplifier (60 dB gain).

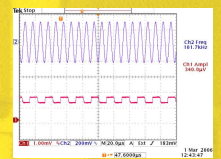


Figure 5: Direct oscilloscope measurement without amplifier.

Cryogenic p-HEMT amplifier

The key element of the amplifier design is a commercial available p-HEMT transistor of depletion type. The whole biasing circuitry has been implemented at ambient room temperature in respect of the small power consumption. All gate and drain voltage bias lines are controlled separately to adjust the operation point. The best operation points for each single stage of the amplifier are optimized by various ambient and cryogenic measurements of the discrete transistors before the compilation of the amplifier.

- Two realizations: micro-strip and co-planar (CPW)
- Power consumption: 2 mW per transistor
- Voltage gain: about 26 dB (4 stage CPW version)
- Bandwidth: $40 \text{ MHz} - 12 \text{ GHz}$

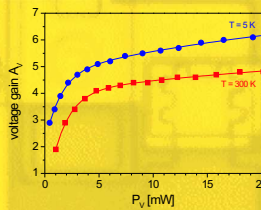


Figure 6: Voltage gain versus power consumption of a single transistor stage.

The transistors were embedded in a microwave design with different transmission line techniques, namely micro-strip (MS) and coplanar (CPW) lines.



Figure 7: Two stage MS (a) and four stage CPW (b) amplifier.

The stages were capacitively coupled and resistively broadband matched to each other. Both designs (MS and CPW) were realized on a Rogers TMM 10i PCB substrate and designed for an input and output impedance of 50Ω .

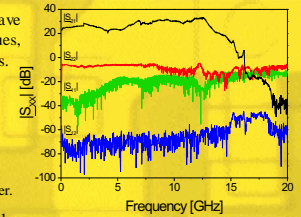


Figure 8: Measurement of the scattering parameters with a power consumption of about 8 mW at 4.2 K .

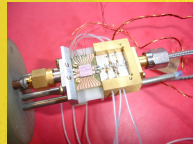


Figure 9: Photograph of the direct coupled MS amplifier and RSFQ circuit.

The low-ohmic dc-coupling to the RSFQ circuit is difficult, because any voltage bias of the first transistor stage introduces a current and change the operation point of the SFQ/dc converter. This can be adjusted by using a separate bias current source (I_b in Fig. 1).

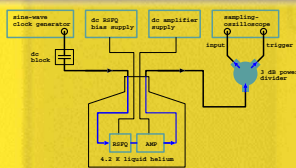


Figure 10: System set-up including: Sine-wave clock generator with dc-block, sampling oscilloscope and two dc-power supplies of RSFQ and amplifier part.

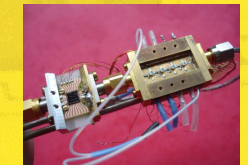


Figure 11: RSFQ circuit and CPW-amplifier are separated to avoid crosstalk of RSFQ input signals to the first amplifier stage.

High-speed test of the RSFQ-CMOS interface

The correct operation of the hybrid interface device is demonstrated by triggering the RSFQ circuit with a sine-wave signal and with current pulses. The bias supply margin of the RSFQ part was not reduced by operating the semiconductor amplifier. We used a microwave power divider for splitting of the weak output signal to generate input and trigger signal at the same time. A dc-block was added in the input line to avoid a ground-loop between the sine-wave generator and the sampling-oscilloscope.

- Output voltage: 3.5 mV
- Demonstrated speed: 3 Gbps maximum

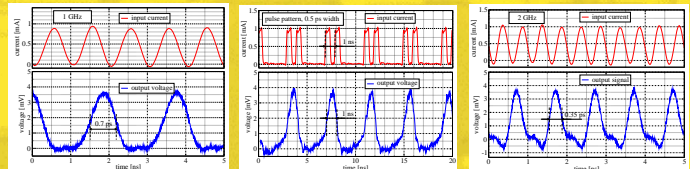


Figure 13: First high speed experiments of the interface circuit without optimization of the passive interconnect.

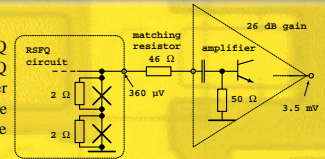


Figure 12: Impedance matching with an additional resistor.

The microwave design of semiconductor circuits at frequencies above 10 GHz and low temperatures meets various challenges, whereby our approach of design and direct implementation is the only reliable way of system analysis. Our first high-frequency experiments of the hybrid interface device show pulse measurements of RSFQ signals with input clock rates up to 3 GHz . The cryogenic amplifier stage provides output voltages of about 3.5 mV at high frequencies.

In the first integrated device test, we mount the RSFQ chip on a PCB and wire-bond it together with the p-HEMT amplifier.

The power consumption of 8 mW in the semiconductor circuit did not disturb the operation of the RSFQ circuit.

If we assume the realization of our RSFQ output driver using the 10 kA/cm^2 NEC standard II process, its voltage before amplification could be as high as 1.2 mV .