Real-time SER measurements of CMOS bulk 40 nm and 65 nm SRAMS combined with neutron spectrometry at the JET Tokamak during its final D-T plasma operation

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***Abstract*— We performed soft error rate (SER) characterization of 40 nm and 65 nm bulk CMOS SRAMs combined with neutron spectrometry in the deuterium-tritium fueled JET tokamak during its final D-T plasma operation (Sept-Oct 2023) producing a series of several dozens of power pulses. Our experimental results demonstrate the impact of machine operation on the electronics reliability, emulating realistic conditions for circuits exposed to the partially radiation-shielded environment of future fusion reactors. Typical bit flip rates of 493 h^{-1} $Gbit^{-1}$ for 65 nm SRAMs and of 2342 h^{-1} $Gbit^{-1}$ for 40 nm SRAMs were measured for a residual machine-induced neutron flux of ~3.15×10^5 cm^{-2} s^{-1} below the reinforced concrete slab (thickness of 1,045 mm) supporting the tokamak chamber. To complete this characterization work, a general methodology for the SER prediction in such a mixed-field D-T neutron radiation environment composed of both thermal and fast neutrons (up to 14 MeV) is presented and validated from this ensemble of experimental data for the two SRAM technologies. Finally, the interest of this approach for future tokamaks and high-energy physics accelerators is discussed.**

***Index Terms*— CMOS, deuterium–tritium (D-T), fusion, JET, neutron, real-time experiment, single event effects (SEE), single-event upset (SEU), soft-error rate (SER), static random-access memory (SRAM), tokamak, WEST.**

I. Introduction

CONTROLLED thermonuclear fusion is a promising energy source currently being investigated by many nations. The main current designs for controlled thermonuclear fusion reactors are based on magnetic confinement (tokamaks) and laser inertial confinement [1]. Both are fueled with deuterium (D) or a mixture of deuterium and tritium (T). A fusion reactor fueled with pure deuterium produces 2.45 MeV neutrons from one of the following two main reactions, which have equal probability of occurrence:

$$\begin{aligned} D + D &\longrightarrow {}^3He(0.82MeV) + n(2.45MeV) \\ D + D &\longrightarrow T(1.01MeV) + p(3.02MeV) \end{aligned} \quad (1)$$

A fusion reactor fueled with a mixture of deuterium and tritium produces 14.07 MeV neutrons after the main reaction:

$$D + T \longrightarrow {}^4_2He(3.52MeV) + n(14.07MeV) \quad (2)$$

In both cases, individual neutrons coming from the plasma and reaching an electronic circuit after passing through shielding can interact instantaneously with the constituent materials of a discrete semiconductor device or those of an integrated circuit. They can produce a wide range of single event effects (SEEs), such as single event upsets (SEUs), single event functional interrupts (SEFIs) or single event hard errors, including single event latchups (SELs), gate ruptures (SEGR) or burn-outs (SEB) [2]. These SEEs can damage or destroy electronic devices or sensors, corrupt signals in digital circuits, corrupt data or programs in memories, microprocessors, microcontrollers, FPGAs, etc. Note that in the field of high-energy physics and particle physics, modern accelerators may face a similar problem. For example, in the Large Hadron Collider (LHC) at CERN, electronics are exposed to thermal neutrons and intermediate-energy neutrons (defined up to 20 MeV), which are close to the energies of fusion-induced

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neutrons but with different energy distributions (harsher spectra, up to GeV of energies), causing SEEs that can affect machine availability [3,4].

In the context of the intense neutron fields produced by future fusion power reactors [5], the transport of the fields outside the reaction chamber and their impact on the reliability of the machine electronics distributed in the facility building (for command, control, and diagnostics) must be anticipated and carefully evaluated to ensure machine operation, long-term dependability, and safety of the installation, for the protection of the people and investment involved. This has motivated the first exploration studies of neutron-induced SEUs on electronics in existing fusion devices we have carried out in recent years on the W-Tungsten Environment in Steady-state Tokamak (WEST) [6,7] during its deuterium plasmas campaigns C5 [8,9] and C7 [10,11], and the second exploration studies on the same subject we have carried out in autumn 2023 on the Joint European Torus (JET) Tokamak during its final deuterium-tritium experiments (JET/DTE-3, also identified as JET campaign C46), presented in this paper. The main goal of all these studies is to support a general methodology under development for the estimation of the sensitivity of general modern electronics to neutron radiation-fields of future fusion machines or high-energy physics accelerators, as discussed in the last part of the paper.

The JET tokamak in which we performed our second exploration studies is a fusion research machine located at the Culham campus for Fusion Energy in Oxfordshire, UK. It was commissioned in 1983 and is currently operated by the UKAEA to carry out the scientific program defined by EUROfusion consortium [12]. The machine has a major radius of 3 meters, and the D-shaped vacuum chamber is 2.5 m wide and 4.2 m high; the total plasma volume within it is 90 m^3. At the time of its design in the 80's, it was the largest tokamak ever built. Between 2009 and 2011, JET was upgraded to adopt concepts being used in the development of the ITER experimental tokamak. During its 2023 final JET/DTE-3 campaign, using 0.2 milligrams of D-T fuel, JET produced 69 megajoules of fusion energy during a six-second plasma pulse [13], beating its previous world record from 2021 DTE-2 campaign of 59 megajoules [14], which itself broke its world record from 1997 DTE-1 campaign of 21.7 megajoules [12,15].

Using the same robust real-time (RT) 65 nm SRAM soft error rate (SER) test setup as in [8,9,10] (hereafter referred to as RTSER test bench) and a DIAMON (Direction-Aware Isotropic and Active Monitor) neutron spectrometer from RAYLAB [16] identical to that used in [8,9], as well as a 40 nm SRAM test setup extensively studied by CERN [4] (hereafter referred to as CERN test bench), this study during the JET/DTE-3 campaign quantifies the effects of neutrons from a large tokamak operating with D-T plasmas on the SER of two different SRAM technologies (40 and 65 nm nodes) representative of modern integrated electronics. Contrary to our previous studies at WEST, and due to the intensity of the neutron fields generated by JET, the test benches were not placed directly in the experimental hall next to the machine, but in a partially radiation-shielded environment (in the basement of the JET tokamak building, under the reinforced concrete slab – thickness of 1,045 mm – supporting the experimental chamber). In this sense, the study is even more relevant, since the error rates obtained are directly representative of the level of unreliability to be expected in areas of a modern tokamak building where a lot of electronic equipment or equipment housing electronics can be installed [9,17]. In the remainder of this paper, after describing the configuration of the experiments, we report the bit flip distributions obtained for the two generations of SRAM memory during the JET DTE-3 campaign, in direct relation to the neutron spectra measured during each individual plasma pulse at the same location as the tested memory devices. The implications of these results for future fusion devices are also discussed, as well as perspectives for future work.

II. Experimental Details

Fig. 1 shows the general layout in which the RTSER and CERN test benches and the DIAMON spectrometer have been integrated to carry out these experiments at JET. It also shows the distribution of the test equipment in the JET building, including the computer connections and network routers between the experimental benches, the power supplies and the computers used for remote control and monitoring of the experiments from the JET, CERN and IM2NP sites. Fig. 2 defines the positions B6 and B7 and the central southern trench in the JET tokamak building. Position B6, shown in Fig. 3, corresponds to the exact location where the test benches and the DIAMON spectrometer were installed, as illustrated in Fig. 4. This position B6 was chosen because it provides a sufficiently high neutron flux during D-T plasma pulses to obtain good SEEs statistics on the RTSER and CERN test benches, while minimizing the risk of neutron-induced failures of the auxiliary equipment (tester, power supply, Ethernet switch) of the RTSER test bench and of the spectrometer. As indicated in Fig. 3, position B6 is equipped with thermo-luminescent dosimeters (TLD) for neutron fluence measurements, which will be used for the analysis of the neutron energy spectra measured with the DIAMON spectrometer.

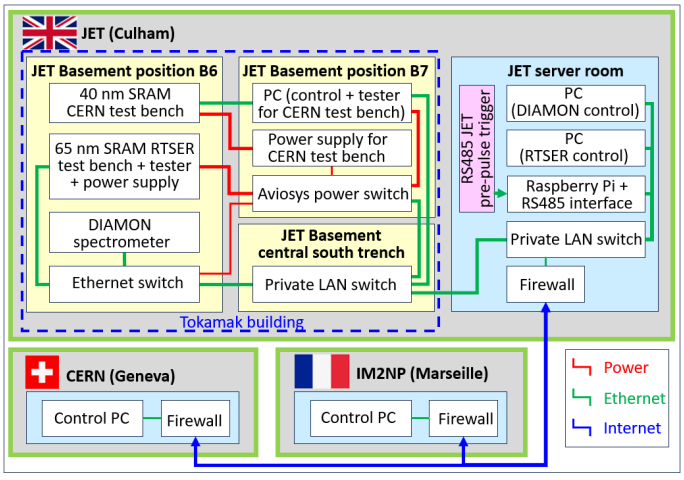

Fig. 1. General layout of the JET-SEE experiment showing the distribution of the test equipment in the different areas of the JET building, the computer connections and network routers between the experimental benches, the power supplies and the computers used for remote control and monitoring of the experiments from the JET, CERN and IM2NP sites.

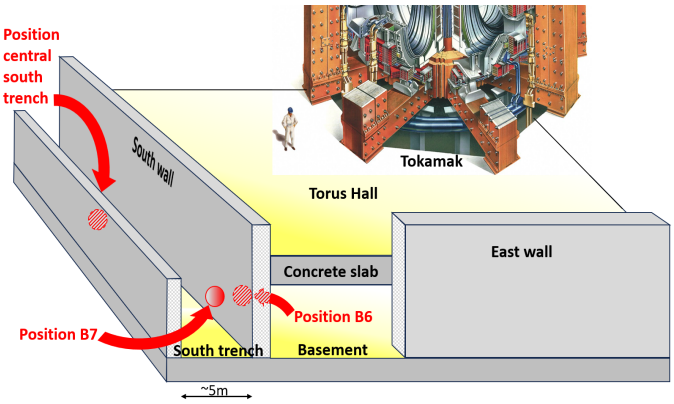

Fig. 2. Positions B6, B7 and the central south trench inside the JET tokamak building.

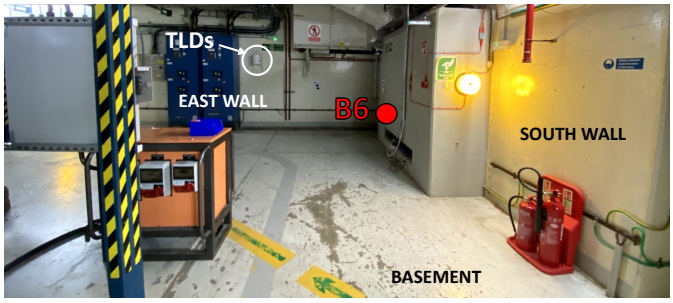

Fig. 3. Positions B6, in the basement of the JET tokamak building (below the reinforced concrete slab supporting the tokamak chamber), where the RTSER and CERN test benches and the DIAMON spectrometer were installed.

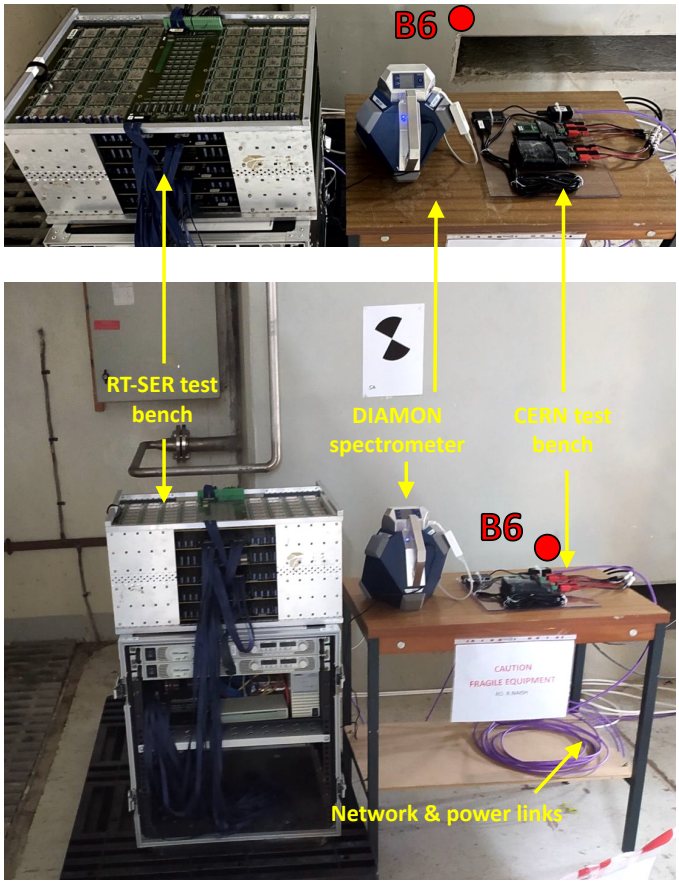

Fig. 4. Installation of the RTSER and CERN test benches and of the DIAMON spectrometer in position B6 in the basement of the JET building.

Position B7 in the south trench is separated from position B6 by the south concrete wall, which attenuates the neutron flux by a factor of approximately 100, thereby further reducing the risk of neutron-induced failure of the control electronics installed in position B7.

For the interpretation of the experimental results, it is crucial to accurately measure the local neutron flux and energy spectrum at the location of the tested electronic memories. For this purpose, we installed in position B6, in the immediate vicinity of the RTSER and CERN test benches (see Fig. 4), a DIAMON spectrometer identical to that used during the SEE experiments in the WEST tokamak [8,9]. DIAMON is a commercial real-time spectrometry-based detection system specifically designed for neutron field characterization and dosimetry with metrological standards. The calibration of the instrument was performed at the National Institute for Ionizing Radiation Metrology of the Italian National Agency for New Technologies, Energy and Sustainable Economic Development (ENEA) [18]. DIAMON performances have also been accurately characterized at various reference neutron radiation facilities, such as the Czech Metrology Institute [19] and the Neutron Calibration Facility of the Polytechnico di Milano [16]. In addition, neutron spectra in many different reference fields have been reported and compared with those evaluated numerically or by a reference calibrated Bonner sphere system [16,20,21]. Neutron spectra, field and dosimetry quantities are thus characterized with metrological quality in the instrument energy range from thermal to 20 MeV of energies.

This spectrometer was connected to a private local area network (LAN) via the Ethernet switch of the RTSER test bench to allow its control by a Raspberry Pi PC installed in the JET server room. This Raspberry Pi PC was equipped with an RS485 interface that received a JET pre-pulse trigger 30 seconds before the start of each plasma pulse. After receiving this trigger, the Raspberry Pi PC sends a request to the DIAMON spectrometer via the LAN to start a spectrum measurement and to stop it after a defined time (2 minutes) that is longer than the maximum plasma pulse duration (45 seconds) plus the countdown time (30 seconds) and shorter than the time between consecutive pulses (about 20 to 30 minutes). Thanks to this, for each plasma pulse, the neutron measurement period by the DIAMON spectrometer starts before the start of the pulse and ends after the end of the pulse. Therefore, for each plasma pulse, the entire fluence of the pulse is measured during the measurement period of the DIAMON spectrometer.

During the SEE experiments at JET, the RTSER test bench was used in the same format as for the previous experiments at WEST (see details in [8,10]). We recall here that this setup contains a bank of 384 SRAM circuits fabricated in 65 nm CMOS bulk by STMicroelectronics using a boro-phospho-silicate-glass (BPSG)-free manufacturing process. Each memory circuit contains 8.5 Mbits of single-port SRAM (no deep N-well) with a bit cell area of 0.525 μm^2, operating at a nominal core voltage of 1.2 V. During measurements, the tester scans the entire memory map (3.226 Gbit) once every 2.5 seconds [22]. The testing procedure corresponds to dynamic tests (permanent accesses): at power on, all devices are written with the reference pattern, then all devices are read back in loop to check for errors.

The CERN test bench consists of two identical motherboards, each containing a 32 Mbit SRAM fabricated in 40 nm bulk CMOS by Integrated Silicon Solution Inc. (ISSI) and operating at a core voltage of 1.1 V [23]. The motherboards allow the memory to be written with an initial pattern (checkboard) and the SEUs to be read every 1 to 5 minutes. The testing procedure corresponds to static tests: the checkboard pattern initially written was read (and rewritten) every 5 minutes.

The ISSI SRAM was chosen for this experiment because of its large thermal neutron cross-section and high sensitivity in the range of 0.1-10 MeV compared to other memories. It has been well characterized in several facilities with neutrons, protons, and heavy ions, and specifically for these tests at JET, its response as a function of neutron energy is well known [24]. In addition, this memory has been modeled in FLUKA Monte Carlo and the neutron SEU cross sections at different energies have been benchmarked to the measured values. One of the two setups (motherboard and memory) was completely shielded with boron carbide in order to record SEUs induced by non-thermal neutrons. The shielding consists of a flexible layer 0.5 cm thick composed of natural boron for 80% of its weight and resulted in an efficient absorption of neutrons below 1 eV [25]. The two motherboards were connected to a power supply and a control PC which were installed in position B7 to reduce the risk of neutron-induced failure.

The RTSER memory bank and its auxiliaries (tester, power supply and Ethernet switch), as well as the CERN test bench power supply and control PC, were powered by an Aviosys power switch to allow remote launch of an OFF/ON cycle in the event of a malfunction. This power switch was installed in position B7 to reduce the risk of neutron-induced malfunctions.

The RTSER tester and power supply were connected to the private LAN via the Ethernet switch to allow their control from a PC installed in the JET server room. The CERN test bench control PC and the Aviosys power switch were also connected to this private LAN. This private LAN was connected to the JET firewall to allow the control of all the equipment connected to it and the downloading of the experimental data recorded by the CERN and RTSER test benches and by the DIAMON spectrometer, via the Internet, from the CERN premises in Switzerland and from the IM2NP premises in France.

III. Experimental Results

Fig. 5 shows a cumulative neutron energy spectrum summing up all valid spectra measured by DIAMON at position B6 during the JET/DTE-3 campaign. We have kept as valid those spectra whose average uncertainty on the experimental data does not exceed a threshold arbitrarily set at 3.5% and whose data show no signs of saturation of the measurement chain (rarely observed for certain pulses inducing a neutron flux greater than the maximum recommended by RAYLAB for DIAMON).

As usual for the atmospheric spectrum, we report the respective weights of the neutron fluence integrated over three energy regions defined in Fig. 5: Part I ($E < 10^{-6}$ MeV), Part II (10^{-6} MeV $< E < 1$ MeV) and Part III ($E > 1$ MeV). The spectrum shows a high-energy neutron peak at 3 MeV and a thermal neutron peak at 56 meV. It is clearly dominated by thermal neutrons noted ThN (Part I: 49.5%), with intermediate neutrons (Part II) and fast neutrons noted FN (Part III) accounting for only 28.7% and 21.8% of the cumulative fluence per lethargy, respectively. The shape of this spectrum results from the degradation of the initial neutron energy (14.07 MeV for D-T plasma pulses) by the shielding they passed through (mainly the concrete ceiling slab of the tokamak building basement) before arriving at position B6, where a large part of them was thermalized by bouncing off the concrete walls, floor and ceiling of B6.

Fig. 6 shows the 61 spectra used to construct the cumulative spectrum of Fig. 5. As expected, the energy of the thermal neutron peaks of these 61 spectra is very stable (between 56 and 93 meV), while that of the high energy neutron peaks is quite scattered (between 0.3 MeV and 12 MeV). The peak amplitudes also vary between pulses, as does the ratio (thermal peak amplitude/high energy peak amplitude), which varies between 0.4 and 2.6. All these variations are due to the variety of pulse operating modes.

The distribution of the number of neutrons produced per pulse as a function of the pulse duration is given in Fig. 7 for all D-T plasma pulses of the JET/DTE-3 campaign with the RTSER and/or CERN test bench operating in position B6 (254 pulses, cumulative duration of 4371 s, cumulative neutron production of 6.84×10^{20} n). Pulses with one or more SEUs detected by the RTSER and/or CERN test bench are colored red (148 pulses). As expected, SEUs occur mainly during the pulses that produced the largest number of neutrons, regardless of pulse duration. For the JET/DTE-3 campaign, virtually all

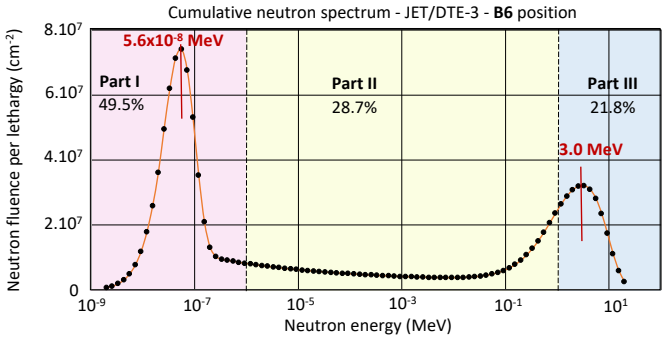

Fig. 5. Cumulative neutron energy spectrum measured by DIAMON at the device level (position B6) during the JET/DTE-3 campaign, integrating all valid spectra of the D-T pulses (61 pulses in total, cumulative neutron production of 1.61×10^{20} n, cumulative plasma duration of 1136 s, cumulative neutron fluence at the device level of 3.21×10^{8} n.cm^{-2}).

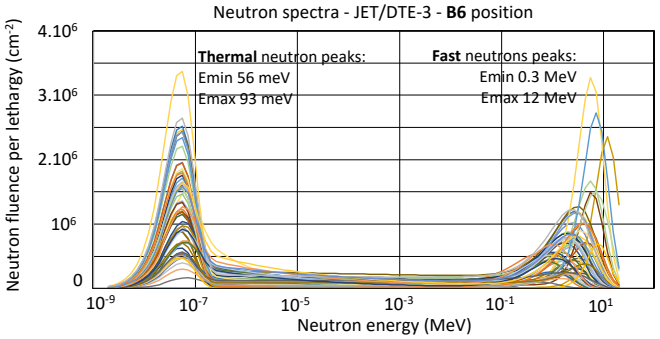

Fig. 6. The 61 valid neutron spectra measured by DIAMON at the device level (position B6) during the JET/DTE-3 campaign and used to construct the cumulative curve of Fig. 5. Emin and Emax correspond to the minimum and maximum energy positions of the neutron peaks, respectively.

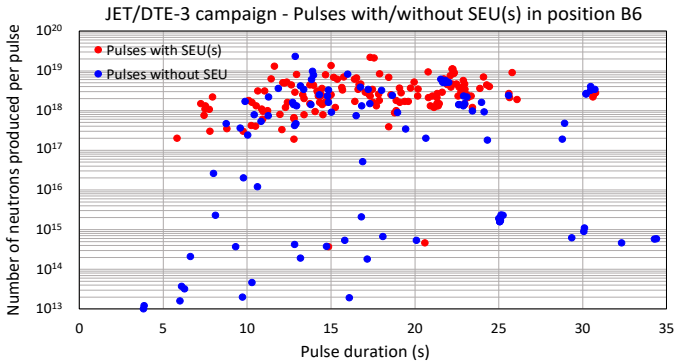

Fig. 7. Number of neutrons per plasma pulse vs. pulse duration during the JET/DTE-3 campaign (D-T plasma). Pulses with one or more SEUs in RTSER and/or CERN test bench are colored red.

pulses producing more than 10^{17} neutrons induced SEUs.

For the RTSER test bench a total of 786 events were recorded for a cumulative fluence of 8.5×10^{8} n/cm^2. These 786 SEUs include 673 single bit upsets (SBUs), 76 multiple cell upset (MCU) of multiplicity 2 (noted MCU(2)), 34 MCUs of multiplicity 3 (MCU(3)), 1 MCU(4), 1 MCU(6) and 1 MCU(9), which gives 946 bit-flips in total. Note that during the second part of the JET/DTE-3 campaign, the RTSER test bench suffered from instabilities in its data acquisition hardware. To address these instabilities, one-third of the bench was decommissioned during this period, reducing the number of memories tested to (2/3) × 3.226 = 2.151 Gbit. This partial decommissioning has been taken into account in Fig. 8 (see explanations in its caption), which shows the accumulation of SEUs recorded by the RTSER test bench as a function of the cumulative neutron fluence at position B6 during D-T plasma pulses. In this figure, the filled symbols correspond to fluences measured by DIAMON at position B6, while the empty symbols correspond to fluences extrapolated at the same position when DIAMON measurements were invalid (for reasons explained at the beginning of Section III) or missing (due to a period of unavailability of DIAMON). The extrapolated fluences at position B6 have been estimated from (i) the number of neutrons produced by the considered plasma pulse (JET data) and (ii) the average ratio {fluence measured at position B6 / neutron produced by the plasma} obtained from all pulses with a valid spectrum measured by DIAMON at position B6. This extrapolation was necessary mostly due to a period of unavailability of DIAMON and rarely due to an invalid spectrum. In this figure also, the black symbols represent the cumulative number of bit flips actually measured at position B6 by the RTSER test bench before and after its partial decommissioning, while the red symbols represent the projection of the cumulative number of bit flips that the test bench would have measured if it had not been partially decommissioned. This projection consisted of applying a factor 3/2 to the bit flips measured during the partial decommissioning.

Similar to Fig. 8, Fig. 9 shows the distribution of SEUs recorded by the CERN test bench as a function of the cumulative neutron fluence at position B6 during the D-T plasma pulses. For a cumulative fluence of 1.34×10^{9} n/cm^2, a total of 91 events (all SBUs) were recorded on the storage without local B_4C shielding (blue symbols) and a total of 21

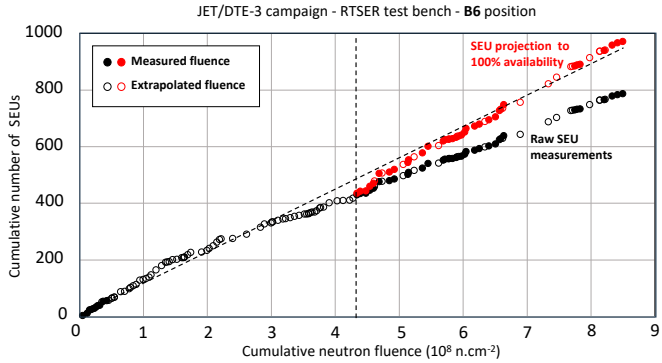

Fig. 8. Distribution of single event upsets (65 nm RTSER test bench) as a function of the cumulative neutron fluence at device level for all the events detected during the JET/DTE-3 campaign. The filled symbols correspond to the fluences measured by DIAMON at position B6, while the empty symbols correspond to the extrapolated fluences at the same position. On the right side of the vertical hatched line, one third of the SRAM circuits of the RTSER test bench was decommissioned: the black symbols represent the cumulative measured SEU and the red symbols indicate the cumulative number of SEU multiplied by a correction factor of 3/2 (in order to emulate a situation similar to the left side of the hatched line where 100% of the circuits were available).

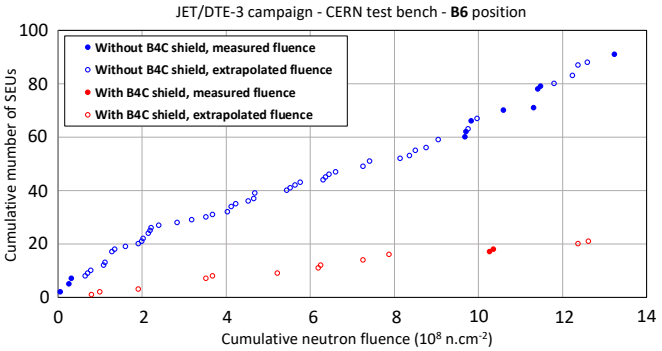

Fig. 9. Distributions of single event upset (40 nm CERN test bench) as a function of the cumulated neutron fluence at the device level for all the events detected on the two motherboards (one bare, the other covered with a B_4C shield) during the JET/DTE-3 campaign.

events (also all SBUs) were recorded on the storage protected against thermal neutrons by local B_4C shielding (red symbols). The CERN test bench received a higher cumulative fluence during its operation in position B6 than the RTSER test bench because the latter suffered a period of unavailability.

IV. Discussion

A. *Validation of bit-flip prediction method and models*

Our first exploration studies of neutron-induced SEUs on electronics in the WEST tokamak during its C5 deuterium plasma campaigns [8,9] allowed us to preliminarily validate a method and models for predicting the bit-flip rate induced by a given D-D plasma neutron environment in a bank of elementary devices (the RTSER test bench), whose effective cross-section of bit-flip production by neutrons had been previously determined by several irradiation tests [26,27]. In these initial studies at WEST, we did not have for the RTSER test bench the parameter of the model of the cross-section of the production of bit-flips by thermal neutrons. We considered only the effective cross section of bit-flip production by fast neutrons (σ_{FN}^{bf}) excluding that due to thermal neutrons, which we considered negligible due to the absence of BPSG in the SRAM memories

of the RTSER test bench [9]. However, in order to improve the precision of the predictions of bit-flip production in the experiments conducted at JET, we finally decided to measure the cross-section of production of bit-flips by thermal neutrons [28] and take it into account for the prediction of bit-flips in the JET environment at position B6.

The main objective of the present study is to validate in a D-T plasma neutron environment the method and models previously validated at WEST under D-D plasma, this time taking also into account the cross-section of bit-flip production by thermal neutrons (σ_{ThN}^{bf}) in the RTSER test bench experiment, and by also considering data obtained with the CERN test bench.

The number of bit-flips N_{bf} induced by a differential neutron fluence $d\varphi/dE$ in a device as a function of its neutron cross-sections of bit-flip productions σ_{ThN}^{bf} and σ_{FN}^{bf} is given by:

$$N_{bf} = \int \left(\sigma_{ThN}^{bf}(E) + \sigma_{FN}^{bf}(E)\right) \times \frac{d\varphi(E)}{dE} dE \quad (3)$$

In (3), σ_{ThN}^{bf} and σ_{FN}^{bf} are given by [9]:

$$\sigma_{ThN}^{bf}(E) = \sigma_{0.025eV}^{bf} \times \sqrt{\frac{25\times10^{-9}}{E(MeV)}} \quad (4)$$

$$\sigma_{FN}^{bf}(E) = \sigma_{sat}^{bf} \times \left(1 - e^{-\left(\frac{E-E_{th}}{w}\right)^{s}}\right) \ , \ E > E_{th} \quad (5)$$

where E is the energy (in MeV) and parameters $\sigma_{0.025eV}^{bf}$, σ_{sat}^{bf}, E_{th}, w and s are given in Table I for the components of the RTSER and CERN test benches.

We define below a global performance indicator for the model evaluation, called PI, which is given by:

$$PI = \frac{N_{bf}^{predicted}}{N_{bf}^{measured}} \quad (6)$$

where $N_{bf}^{predicted}$ is the number of neutron-induced bit-flips predicted by (3) for a given device exposed to a neutron environment characterized by the curve $d\varphi/dE$, and $N_{bf}^{measured}$ is the number of bit-flips measured in this same device exposed to the same environment (note that $N_{bf}^{measured}$ always includes both thermal and fast neutron contributions).

We evaluated this performance indicator for the RTSER and CERN experiments for the two following cases:

(a) We considered all D-T plasma pulses for which (i) the test bench under consideration was functional in position B6 and (ii) a valid spectrum had been produced by DIAMON in position B6;

(b) We considered all D-T plasma pulses for which the considered test bench was functional at position B6 (with and without valid spectrum). In this case, we assigned to the pulses without valid spectra, neutron spectra extrapolated at position B6 from (i) the number of neutrons produced by the considered plasma pulse (JET data) and (ii) the average ratio {neutron measured at position B6 / neutron produced by the plasma} obtained from all the pulses with a valid spectrum measured by DIAMON at position B6.

Tables II, III and IV give, respectively for the RTSER and CERN test benches with and without B_4C shielding, the number of predicted and measured bit flips and the performance indicator PI obtained in cases (a) and (b) defined above. Tables II and III also show the contributions of thermal and fast neutrons to the number of predicted bit flips and to the overall performance indicator PI. The PIs provided in Tables II and III for BF_{ThN} are the ratio (bit-flips predicted for ThN / bit-flips measured for ThN+FN), which represent the contribution of the ThN to the global PI for ThN+FN. Similarly, the PIs provided in these tables for BF_{FN} are the ratio (bit-flips predicted for FN / bit-flips measured for ThN+FN), which represent the contribution of the FN to the global PI for ThN+FN. In Table III for the CERN test bench not protected by B_4C shielding, $N_{bf}^{predicted}$ is calculated using (3) in which $\sigma_{ThN}^{bf}(E)$ and $\sigma_{FN}^{bf}(E)$ are given by (4) and (5). For the CERN test bench protected by B_4C shielding (Table IV), $N_{bf}^{predicted}$ is calculated using (3) in which $\sigma_{ThN}^{bf}(E)$ is set to 0 (assuming 100% attenuation of thermal neutrons) and $\sigma_{FN}^{bf}(E)$ is given by (5). The partial decommissioning of the RTSER test bench (see Section III) was

TABLE I
PARAMETERS OF σ_{ThN}^{bf} AND σ_{FN}^{bf} FOR RTSER AND CERN TEST BENCHES EXTRACTED FROM ACCELERATED TESTS UNDER VARIOUS NEUTRON BEAMS (NORMAL INCIDENCE)

Device	Node	σ_{sat}^{bf}	E_{th}	w	s	$\sigma_{0.025eV}^{bf}$
	nm	cm²/bit	MeV	MeV	-	cm²/bit
RTSER [9, 28]	65	3.17×10^{-15}	0.148	9.115	0.856	1.80×10^{-16}
CERN [4, 24]	40	1.40×10^{-14}	0.01	14.05	0.82	3.16×10^{-15}

TABLE II
BIT-FLIPS (BF) AND PERFORMANCE INDICATOR FOR RTSER TEST BENCH
case a: 49 pulses, $\varphi=2.59\times10^8$ n/cm², case b: 159 pulses, $\varphi=8.50\times10^8$ n/cm²

	Case	BF_{ThN}	BF_{FN}	BF_{ThN+FN}
$N_{bf}^{measured}$	(a)	N/A	N/A	426(*)
$N_{bf}^{predicted}$	(a)	62 (21%)	239 (79%)	301 (100%)
PI	(a)	15%	56%	71%
$N_{bf}^{measured}$	(b)	N/A	N/A	1167(*)
$N_{bf}^{predicted}$	(b)	205 (20%)	801 (80%)	1007 (100%)
PI	(b)	18%	69%	87%

(*) incl. factor 3/2 on bit-flips when partial decommissioning.

TABLE III
BIT-FLIPS (BF) AND PERFORMANCE INDICATOR FOR CERN TEST BENCH WITHOUT B_4C SHIELDING
case a: 61 pulses, $\varphi=3.02\times10^8$ n/cm², case b: 254 pulses, $\varphi=1.34\times10^9$ n/cm²

	Case	BF_{ThN}	BF_{FN}	BF_{ThN+FN}
$N_{bf}^{measured}$	(a)	N/A	N/A	28
$N_{bf}^{predicted}$	(a)	13 (55%)	11 (45%)	24 (100%)
PI	(a)	47%	38%	85%
$N_{bf}^{measured}$	(b)	N/A	N/A	91
$N_{bf}^{predicted}$	(b)	53 (55%)	44 (45%)	97 (100%)
PI	(b)	59%	48%	107%

TABLE IV
BIT-FLIPS AND PERFORMANCE INDICATOR FOR CERN TEST BENCH WITH B_4C SHIELDING
case a: 61 pulses, φ=3.02×10^8 n/cm^2, case b: 254 pulses, φ=1.34×10^9 n/cm^2

	Case	BF_{FN}
$N_{bf}^{measured}$	(a)	2
$N_{bf}^{predicted}$	(a)	11
PI	(a)	550%
$N_{bf}^{measured}$	(b)	21
$N_{bf}^{predicted}$	(b)	44
PI	(b)	209%

accounted for in the PI calculation by multiplying the number of bit flips measured during the relevant pulses by 3/2.

Tables II and III show that the prediction slightly differ from the measurement, in the worst case by 29% (RTSER, case a, PI = 71%), and in the best case by 7% (CERN test bench without B_4C, case b, PI = 107%). For each test bench, case (b) always gives a prediction closer to the measurement than case (a), because it is based on a broader statistical base (number of bit-flips measured). In both cases (a and b), the prediction obtained with the CERN test bench is closer to the measurement than that obtained with the RTSER test bench, possibly due to better precision of the parameters of the models $\sigma_{ThN}^{bf}(E)$ and/or $\sigma_{FN}^{bf}(E)$. However, as for the CERN test bench, the prediction obtained for the RTSER test bench is also very satisfactory.

Table IV shows much larger gaps between prediction and measurement (450% in case (a) and +109% in case (b)) than in Tables II and III. These gaps between predictions and measurements are due to: i) the model itself and the experimental uncertainty on its parameters and ii) the statistical uncertainty on the experimental bit-flip counting process. To evaluate this second uncertainty (i.e., only for the counting process), bit flips are treated as random events and modelled using the Poisson distribution [29,30]. The confidence interval for the number of bit flips N_{bf} detected by the test bench can be then expressed using the relationship between the cumulative distribution functions of the Poisson and chi-squared distributions. The upper and lower estimates of N_{bf} are:

$$\frac{1}{2}\chi^2\left(\frac{\alpha}{2}, 2\left(N_{bf}+1\right)\right) \leq N_{bf} \leq \frac{1}{2}\chi^2\left(1-\frac{\alpha}{2}, 2\left(N_{bf}+1\right)\right) \quad (7)$$

For Table IV, we obtained $1 \leq N_{bf} \leq 6$ for the case (a) and $15 \leq N_{bf} \leq 30$ for the case (b) for a 90% confidence interval (α =0.1). The extreme estimated values for PI can be directly evaluated from these confidence intervals: 183% ≤ PI ≤ 1100% for the case (a) and 146% ≤ PI ≤ 293% for the case (b). Similar calculations can be performed for Tables II and III. Focusing on the best PI values that can be deduced from these data, we obtain for Table II 71% (case a) and 87% (case b), for Table III 85% (case a) and 107% (case b) and for Table IV, as indicated above, 183% (case a) and 146% (case b). All these values show that in the best expected case the predictions are within a factor lower than 2 of the experiment.

Another possible source of difference between measurements and predictions is the angle of incidence of the neutrons. It should be noted that all the values reported in Table I were obtained from monoenergetic or thermal beam tests with neutrons arriving perpendicular to the surface of the devices. These values have been considered to make predictions in the current situation at JET, where the distribution of angles of incidence for neutrons in position B6 is unknown, but most likely very different from a normal and uniform incidence. The fact that the characteristics of neutron-induced SEUs may depend significantly on the angle of incidence, especially for high-energy neutrons, could be a source of discrepancy for the numerical predictions of our model, difficult to evaluate at this stage.

Finally, it should be noted that the prediction of MCU/SBU rates should be of interest for the comprehensive and fine characterization of device reliability. The same approach and formula can be used to carry out an analysis of MCU-type events. However, due to the experimental constraints, we were not able to accumulate sufficient statistics for MCU events at high multiplicities (the confidence intervals would have been much too wide because of the low statistical power). For this reason, the analysis of the results was carried out only in terms of the number of bit flips and not in terms of MCU/SBU rates, in addition to the fact that only single bit flips were observed for the CERN test bench.

B. Comparison of the SEU sensitivity of the two test benches

On the one hand, Table I shows that the RTSER test bench has a lower sensitivity to thermal neutrons ($\sigma_{0.025eV}^{bf}$) than the CERN test bench. On the other hand, Tables II and III show that thermal neutrons only contribute to 20% (Table II, case (b)) of the bit-flips induced in the RTSER test bench by D-T plasma neutrons from JET/DTE-3 campaign, while they contribute to 55% (Table III, case (b)) in the CERN test bench. Table V compares the ratio (bit-flip/Mbit)/(neutron fluence) of the CERN and RTSER test benches for cases (a) and (b). Thus, in the neutron environment of position B6 of the D-T plasma operated JET tokamak, which is representative of the areas of a modern tokamak building where many electronic devices or devices with electronics can be installed, the 40 nm SRAM of the CERN test bench shows a sensitivity to neutron-induced bit-flips about 5 times higher than that of the 65 nm SRAM of the RTSER test bench. These differences in neutron-induced SEU sensitivity between two components provide an illustration of the dispersion of sensitivity that can be found among the components of the panel that will be investigated in future studies (see Section IV-D).

C. Thermal neutron attenuation by B_4C local shield

Tables III and IV show for case (b) (which has a better statistical basis than case (a)) that the CERN test bench protected against thermal neutrons by a local B_4C shield has about 4.3 (= 91/21) times fewer bit flips than the CERN test bench without a local B_4C shield. This figure does not directly reflect the attenuation of the thermal neutron flux by the B_4C shielding, since it takes into account the bit flips induced by fast neutrons. However, it gives a first indication of the attenuation of the number of bit-flips that local B_4C shielding could provide in the thermal and fast neutron environment of a tokamak operated with D-T plasma.

TABLE V
BIT-FLIPS PER MBIT AND PER FLUENCE FOR RTSER TEST BENCH AND CERN TEST BENCH WITHOUT B_4C SHIELDING

	Case	CERN	RTSER	CERN /RTSER
$\frac{N_{bf}^{measured}/Mbit}{neutron\ fluence}$	(a)	2.89×10^{-9}	5.10×10^{-10}	5.67
$\frac{N_{bf}^{measured}/Mbit}{neutron\ fluence}$	(b)	2.12×10^{-9}	4.26×10^{-10}	4.99

TABLE VI
MAIN EXPERIMENTAL DATA FOR RTSER TEST BENCH AND CERN TEST BENCH WITHOUT B_4C SHIELDING IN POSITION B6

	RTSER	CERN
Memory size (Mbit)	3226	32
Number of D-T plasma pulses	159	254
Cumulative neutron production (n)	4.21×10^{20}	6.84×10^{20}
Cumulative fluence (n.cm^{-2})	8.50×10^{8}	1.34×10^{9}
Cumulative plasma duration (s)	2638	4371
Cumulative bit flips	1167(*)	91
Average neutron flux (n.cm^{-2}.s^{-1})	3.22×10^{5}	3.07×10^{5}
Average bit flip rate (h^{-1}.Gbit^{-1})	493	2342

(*) incl. factor 3/2 on bit-flips when partial decommissioning.

TABLE VII
RELIABILITY DEGRADATION FACTOR (RDF) FOR RTSER TEST BENCH AND CERN TEST BENCH WITHOUT B_4C SHIELDING

	RTSER	CERN
Average bit flip rate in position B6 (s^{-1}.Gbit^{-1})	1.37×10^{-1}	6.51×10^{-1}
Average bit flip rate on earth at sea level (s^{-1}.Gbit^{-1})	1.47×10^{-8}	6.77×10^{-8}
RDF	9.34×10^{6}	9.60×10^{6}

D. Neutron impact on electronics reliability in future reactors

Table VI summarizes the main experimental data for RTSER test bench and CERN test bench without B_4C shielding exposed to neutrons from D-T plasma pulses in position B6 with an average neutron flux of ~3.15×10^{5} n.cm^{-2}.s^{-1}. In this neutron environment, representative for tokamak electronics, the average neutron-induced bit-flip rates normalized to 1 Gbit are respectively 493 bit-flip per hour for the 65 nm SRAM and 2342 bit-flip per hour for the 40 nm SRAM. These values have been estimated from the ratio between (i) the total number of bit-flips recorded during all of the plasma pulses (during which the test bench has been operated) and (ii) the total cumulative duration for all these pulses. This is an average rate because the neutron flux can vary during plasma pulses and from one plasma pulse to another, depending on the operating mode (plasma composition, auxiliary heating, etc.). There is no uncertainty in the number of bit-flips measured. The uncertainty on the average rate of bit-flips is therefore only determined by the uncertainty on the duration of the plasma pulses, which is ±4ms (JET operator data), i.e. lower than ±0.1% for plasma pulses longer than 5 s. The resulting uncertainty on the average bit-flip rate is therefore negligible, around ±0.1%. Note that a typical value of one Gbit is the estimated amount of configuration memory in control electronics installed in the basement of the WEST tokamak [9], a medium-size tokamak. In a larger and more modern D-T tokamak, the amount of configuration memory in control electronics exposed to neutrons could be several orders of magnitude greater. These figures, which give a preliminary rough estimate of the failure rates which could occur in electronic circuits housing 1 Gbit of SRAM configuration memory exposed to the neutron environment of position B6 during D-T plasma pulses, confirm the impact of neutrons of tokamak D-T plasma operation on the reliability of electronics in conditions approaching those of future reactors. Note that these error rates may in certain cases be lower than the bit-flip rate due to masking phenomena.

The reliability degradation of a component, induced by a given neutron environment, can be represented by a Reliability Degradation Factor (RDF) which is defined as the ratio of the neutron-induced bit-flip error rate in the neutron environment considered (here noted BER_{B6}^{RTSER} for the RTSER test bench in position B6 during D-T plasma pulses) to the neutron-induced bit-flip error rate (BER_{Earth}^{RTSER}) in the natural terrestrial atmospheric neutron environment at sea level (total neutron flux of 0.012 n.cm^{-2}.s^{-1} [31]). Thus, the RDF can be defined as:

$$RDF = \frac{BER_{B6}^{RTSER}}{BER_{Earth}^{RTSER}} \quad (8)$$

In (7), BER_{B6}^{RTSER} and BER_{Earth}^{RTSER} are given by:

$$BER_{B6}^{RTSER} = \int \left(\sigma_{ThN}^{bf}(E) + \sigma_{FN}^{bf}(E)\right) \times \frac{d\Phi_{B6}(E)}{dE} dE \quad (9)$$

$$BER_{Earth}^{RTSER} = \int \left(\sigma_{ThN}^{bf}(E) + \sigma_{FN}^{bf}(E)\right) \times \frac{d\Phi_{Earth}(E)}{dE} dE \quad (10)$$

where $\frac{d\Phi_{B6}(E)}{dE}$ is the average differential neutron flux in position B6 obtained by dividing the differential neutron fluence in position B6 by the related cumulative plasma duration and $\frac{d\Phi_{Earth}(E)}{dE}$ is the reference differential terrestrial atmospheric neutron flux at sea level [32], described by the following parametrized model [29]:

$$\frac{d\Phi_{Earth}(E)}{dE} = \sum_{j=1}^{8} a_j exp\left[-\left(\frac{log(E)-b_j}{c_j}\right)^2\right] \quad (11)$$

where the 24 parameters a_j, b_j and c_j are given in [29].

Based on the above Eqs. (8-11), Table VII gives the RDF of the RTSER test bench and of the CERN test bench without B_4C shielding induced by the neutron environment of position B6 during D-T plasma pulses. This table shows that, in this neutron environment, the RDF of these test benches is about 10^7. This gives a worst-case estimate of the degradation of the reliability of electronic circuits containing SRAM memories, in a neutron environment representative of those areas of a modern tokamak building where a lot of electronic equipment or equipment containing electronics may be installed. Table VII also shows that, although the CERN test bench is more sensitive to neutron-induced bit-flips (see average bit flip rate in table VI), it has a slightly lower RDF than that of the RTSER test bench.

The RDF model defined by (8) can be generalized as the ratio between the SEE rate in a given artificial environment and the

SEE rate in the reference natural terrestrial ground-level neutron environment adopted by the JESD98A standard:

$$RDF = \frac{SER_{artificial}}{SER_{reference}} \quad (12)$$

This generalized RDF model will be used for a broader study of the sensitivity of general modern electronics to neutron-induced SEEs. This study will be carried out on a panel of components representative of the elementary functions present in general modern electronics (e.g. memories, power devices, FPGAs, etc.), covering different technologies, technological nodes and specific (technology-dependent) single event effects [33]. The components of this panel will be tested under thermal neutrons and under monoenergetic neutrons (up to 20 MeV) to obtain their parameters $\sigma_{ThN}^{bf}(E)$ and $\sigma_{FN}^{bf}(E)$ and then to calculate their RDF values for any artificial neutron environment.

Let's denote by $RDF_{wc}^{artificial}$ the worst-case RDF in a given artificial neutron environment, obtained among all the elementary components of the panel. For each electronic system, it is conservatively assumed that the neutron-induced SEEs in elementary electronic functions hosted by an electronic system propagate without attenuation to the upper level, causing errors or failures of the electronic systems hosting these functions. The $RDF_{wc}^{artificial}$, multiplied by the reliability of a given electronic system in the natural terrestrial ground-level neutron environment, provides an estimate of the worst-case reliability of that electronic system in the considered artificial neutron environment, without the need for neutron SEE testing of that electronic system.

This approach is of interest for facilities having large quantities and diversity of commercial off-the-shelf (COTS) electronic systems exposed to neutrons, such as tokamaks, and also high energy physics accelerators such as the LHC at CERN, which face the same SEE problem as tokamaks, with neutrons having roughly the same energy range (and also with higher energy hadrons). More generally, it may also be of interest to any nuclear facility (including fission power plants) wishing to install electronics in radiation-shielded areas. Such an approach will allow to optimize local shielding against thermal neutrons (directly on electronics cabinets) and, if necessary, shielding against high-energy neutrons in the building structure surrounding the room housing electronics cabinets, without further neutron irradiation studies, which will be especially useful when neutron qualification is difficult (e.g. for large quantities and diversity of electronics) or not feasible (e.g. for COTS electronics).

V. Conclusion

In this study, we took the opportunity of the final D-T plasma operation of the JET tokamak in 2023 to conduct a unique and comprehensive characterization of the soft error rate for 40 nm and 65 nm bulk CMOS SRAMs exposed to machine-induced neutron pulses combined with pulse-resolved neutron spectrometry. This original experiment allowed us to assess the impact of machine operation on the reliability of electronics, thereby simulating the realistic conditions that circuits will face in the partially radiation-shielded environments of future fusion reactors. The experimental results revealed bit flip rates of 493 h^{-1} $Gbit^{-1}$ for 65 nm SRAMs and of 2342 h^{-1} $Gbit^{-1}$ for 40 nm SRAMs, under a residual machine-induced neutron flux of ~3.15×10^5 $cm^{-2}s^{-1}$ at circuit level. To further support this characterization, we developed and validated a general methodology for predicting SER in such a mixed-field D-T neutron radiation environment, which consists of both thermal and fast neutrons (up to 14 MeV). The results from this extensive data set for the two SRAM technologies highlight the utility of this approach in enhancing our understanding and preparing for the challenges associated with future tokamaks and high-energy physics accelerators.

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