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Elaboration of NbN ADC Circuits on Large Area Wafers for HyperSCAN

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HAL Authorization

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Aim of HyperSCAN

Hyperfrequency Superconducting Converter from Analog to Numerics

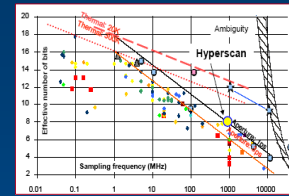
HyperSCAN is a six partners project* on wide band-pass $\Sigma\Delta$ Analog-to-Digital Converter operating at microwave telecoms carrier frequencies.

➤ Very high clock frequency (~150 GHz) and 9K operation are expected, thanks to submicron size (0.7 μ m) self-shunted NbN-Ta_nN-NbN SNS Josephson junctions patterned accurately using a 8-inch C-MOS platform.

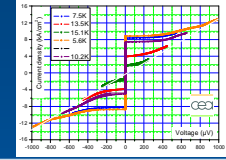
➤ We describe the circuit multilayer deposition conditions for development of planarized submicron JJ on 8-inch Si wafers.

➤ Based on VHDL description of the architecture, circuit blocks modelling and implementation, on devoted wiring connexions, the ADC NbN circuits are expected to operate with good margins at 9K inside a compact cryocooler.

* labelled by French ANR & by Minalogic

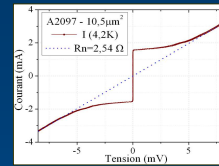


HyperSCAN ADC targeted performances at 9K



Typical I-Vs of a NbN junction in a wide temperature range up to 15K

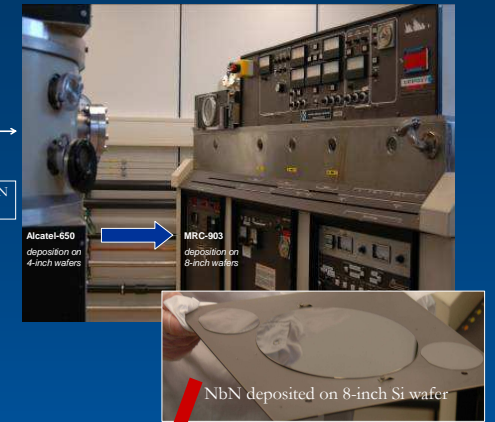
Elaboration of stack layers and NbN-TaN/NbN junctions on 8-inch Si wafers



Typical $R_n I_C = 3.9$ mV obtained at 4.2K from NbN-TaN/NbN junctions on 3-inch wafers (equipment Alcatel-650)
See: R. Setu, E. Baggetta, J.-C. Villégier, Journal of Physics: Conference Series 97, 2008, pp 012077-012083, and talk 4EX07.

Transfer of the elaboration by DC-Mag sputtering of NbN, NbTiN layers and NbN-TaN/NbN junctions from 3-inch (Alcatel-650 equipment) to 8-inch Si wafers (MRC-903 equipment)

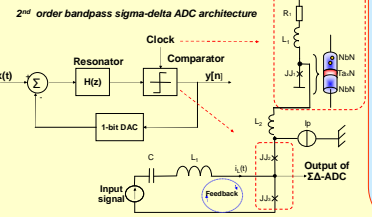
Layer	Thickness	Deposition and planarization conditions
NbTiN (5- <i>IR</i>)	650 nm +/- 5%	DC-Mag sputter deposition from a Nb ₅₀ Ti ₅₀ target (to be optimized)
Mo (RE)	40 nm +/- 5%	Sputtering deposition @200°C, I.H.V. 3.40Um/sq
SiO ₂ (3- <i>BR</i>)	300 nm +/- 5%	Planarization by 400°C TeOS PECVD deposition + CMP
NbN (4- <i>W</i>)	500 nm +/- 5%	DC-Mag Sputter deposition from a Nb target Electrical contact on 3 ϕ junction is obtained by oxide CMP stop on NbN
SiO ₂ (2- <i>J</i>)	450 nm +/- 5%	Planarization by 400°C TeOS PECVD deposition + CMP
NbN (3- <i>CJ</i>)	180 nm +/- 5%	DC-Mag reactive sputtering from a Nb target/ $\phi=0.7\mu$ m junction are defined thanks to DUV lithography using an ASM300 stepper (@ 240nm)
TaN Barrier	8 nm +/- 5%	DC-Mag reactive sputter deposition from a Ta target
NbN (2- <i>BE</i>)	270 nm +/- 5%	DC-Mag reactive sputter deposition from a Nb target
SiO ₂ (1- <i>GP</i>)	300 nm +/- 5%	Planarization by 400°C TeOS PECVD deposition + CMP + via
NbTiN (G- <i>Plan</i>)	550 nm +/- 5%	DC-Mag sputter deposition from a Nb ₅₀ Ti ₅₀ target (to be optimized)



NbN deposited on 8-inch Si wafer

Architecture, design and test of the NbN ADC and circuits blocks

Top-down modelling to reproduce ideally classical architecture performance



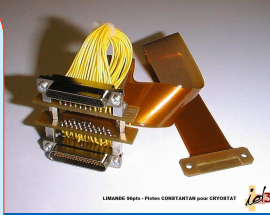
VHDL-AMS code: sigma delta bandpass ADC modelling

Architecture
Terminal ta, b: electrical.
Quantity vin across in through ta to ground;
Signal clk_compa, bit => 0;
Constant Di: Time => 0.0834ps;
Constant Prio: real => 2.075e-15;
Begin

--- Clock system
Process (clk_compa) begin
if clk_compa = '1' then
clk_compa <= '0' AFTER 4.17ps; -- T2 => F = 120Ghz else
clk_compa <= '1' AFTER 4.17ps;
end if;
End Process;

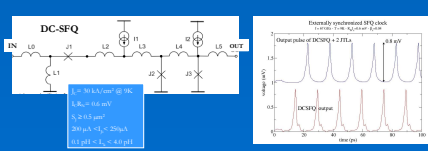
--- Input Signal with amplitude = $\Phi_p/2$ (T)
vin <= Prio(2.0's.34e-12'sin(2.0'MATH_PI*30'Hz*t));
--- Resonator
Resonator1: entity work.ResonatorC (behaviour)
generic map (Di, Prio, Di, 1.0e-12) -- L = C => 30Ghz; to port map (ta => ta, tb => tb);

--- Comparator and ADC output (+1)
Compa1: entity work.Compa1 (behaviour)
generic map (clk_compa, Di)
port map (ta => tb, tb => ground);
End;

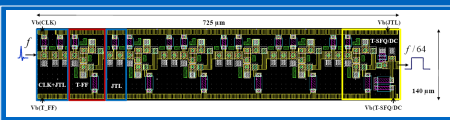


Preparation of a mixed flexible and semi-rigid connexions attached to the 9K chip carrier

Sigma-Delta band-pass ADC modelling using VHDL-AMS description



Simulated pattern at 67GHz of a SFQ clock generator triggered externally



Preliminary comparison of NbN versus Nb
(see: E. Baggetta INAC-Grenoble 2007 thesis and R. Setu UJF-Grenoble 2007 thesis supported by CNET, Thales Alenia Space, CEI)

A 45 JJ frequency divider (F/64) circuit demonstrator is applied to a relaxed $\Phi=2.5\mu$ m, 4.5kA/cm², NbN technology at 9K & compared to a Nb circuit at 4.2K (4.5kA/cm² junctionity).

Main advantages observed in 9K NbN self-shunted technology over 4K Nb are:

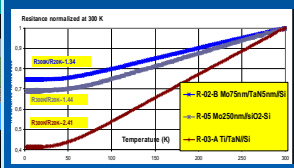
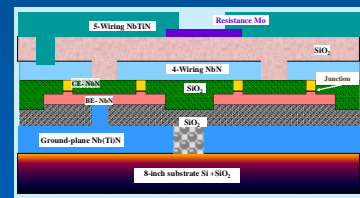
- A 30% gain in circuit compactness due to self-shunted NbN-TaN-NbN junctions
- More than 50% gain in F_{max} (due to large $R_n I_C$ and to TaN capacitance negligible)
- More than 300% gain in the cryocooling power required @ 9K versus 4K

Summary

The high accuracy obtained in patterning submicron (0.7 μ m) planar NbN-TaN-NbN junctions thanks to the stepper and the large $R_n I_C \approx 0.6$ mV product observed at 9K (see talk 4EX07) made the 400°C compatible, processing of 9K-NbN-ADCs chips on 8 inch Si wafer feasible at low cost.

The architecture and the wiring connexions of HyperSCAN chip have also been designed to take benefit of the speed and of the strongly reduced overall power dissipation in operating NbN RSFQ functions in a cryocooler at 9K in regard to a 4K cooled operating Nb chip.

NbN ADC circuit multilayer parameters on 8-inch Si wafers

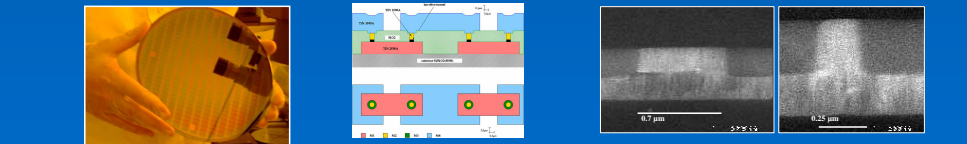


Resistivity versus temperature for Mo, Ti et TaN layers sputtered on Si wafers (MRC-903)

Film/Substrate	Sheet Resistance @ 300K (ohms/sq)	Tc (K)	RR R_{300K}/R_{2K}	XRD (on Nb(111) Angle/Width (°) Intensity(cps/θ)
Nb/SiO ₂ /Si	0.37	9.21	4.61	45.4 / 0.60 130
Nb/SiO ₂ /Si 350°C / r=80nm	0.36	9.24	5.32	45.4 / 0.58 150
Nb/SiO ₂ /Si 400°C / r=80nm	0.36	9.19	5.98	45.3 / 0.5 200
NbN/SiO ₂ /Si 400°C / r=50nm	8.4	>15K	TBM	TBM

Characterization of first Nb and NbN DC-Mag sputtered films ($I_{C,RR} = 10$) on 8-inch Si+SiO₂ wafers (equipment MRC-903)

Evaluation of critical technological parameter using a circuit test vehicle



The critical dimensions, i.e. $\phi=0.7\mu$ m nitride junction technology process has been proved feasible by applying the high accuracy, low spread lithography and CMP planarization at the CMOS CEA-Leti platform on 200mm Si wafers (see N. Hudack UJF-Grenoble 2002 thesis and related publications).



Simplified test-vehicle process stack applied on 8-inch to planarized 0.7 μ m JJ followed by post-processing of via, Wir-3 and contacts done on 3 inch diced wafers.

Partial view of two chips (1x1 cm²; 64 pads) test vehicle: Series-parallel arrays of 0.7 μ m and larger junctions (at left); resonators and anti-aliasing filters (at right).

Project granted by ANR06-TCOM-026 & through Minalogic