



HAL
open science

Design and elaboration of 9K NbN ADC circuits

M. Aurino, S. Bouat, J-C. Villégier, C. Socquet-Clerc, D. Renaud, C. Bornier, P. Febvre, Patricia Desgreys, Patrick Loumeau, M. Maignan

► **To cite this version:**

M. Aurino, S. Bouat, J-C. Villégier, C. Socquet-Clerc, D. Renaud, et al.. Design and elaboration of 9K NbN ADC circuits. ASC 2010 - Applied Superconductivity Conference, Aug 2010, Washington, United States. . <hal-04925498>

HAL Id: hal-04925498

<https://hal.science/hal-04925498v1>

Submitted on 2 Feb 2025

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

M.Aurino, S. Bouat, J.-C. Villégier(*), CEA, INAC, Superconducting Devices Group, 38054-GRENOBLE-Cdx-9 -Fr, C. Socquet-Clerc, D. Renaud, CEA, LETI-Minatec, 38054-GRENOBLE-Cdx-9 -Fr, C. Bornier, ID3-Semiconductors, 38120 LE FONTANIL -Fr; P. Febvre, IMEP-LAHC, Univ. de Savoie, 73376 LE BOURGET DU LAC-Fr, P. Desgreys, P. Loumeau, I-TELECOM -ParisTech, 75634 PARIS -Fr, M. Maignan, Thales Alenia Space, 31000-TOULOUSE, Fr

Aim of HyperSCAN

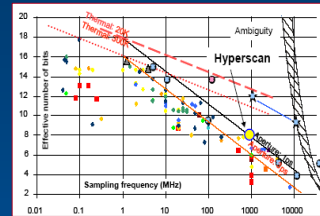
Hyperfrequency Superconducting signals Converter from Analogue to Numerics

HyperSCAN is a project* on wide band-pass $\Sigma\Delta$ Analog-to-Digital Converter operating at microwave telecoms carrier frequencies and 9K.

- > High clock frequency (~120 GHz) are targeted, thanks to self-shunted NbN-TaN-NbN SNS JJ with $R_n I_C > 1.5mV$ at 9K
- > The nitride technology is based on 8-inch Si wafers and planarized $0.5\mu m^2$ (diameter 700 nm - $3\sigma = 40nm$) JJ patterned using the low spread lithography and CMP planarization of LETI-CMOS platform.
- > NbTiN wiring & ground-plane have reduced penetration depth in comparison to NbN.
- > A band-pass Sigma-Delta ADC circuit designed with VHDL-AMS has been implemented with a modulator clock frequency of 120 GHz and decimation filters based on a comb design leading to SNR of 59 dB overall performances.
- > A flexible and compact cryo-package has been produced to stabilize temperature at or near 9K (+/- 0.05K), reducing the overall power dissipation in operating NbN RSFQ functions.

* labelled by French ANR-TCOM & by Minalogic

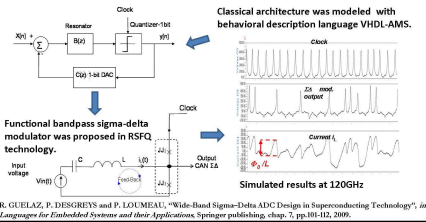
HyperSCAN targeted performances @ 9K



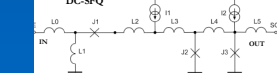
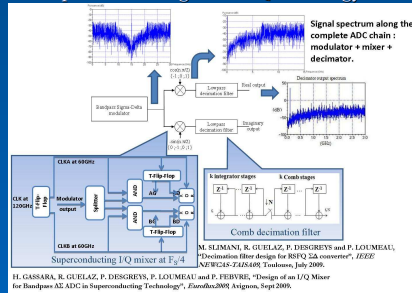
Architecture, design and test of the NbN ADC sub-circuits

Bandpass sigma-delta modulator design

- Bandpass Sigma-delta modulator architecture was designed:
 - with NbN technological values provided INAC
 - following a top-down methodology with specific modeling for Josephson junction.
- Simulated SNR is 59 dB taking into account real pulse shape and clock noise due to comparator switching.

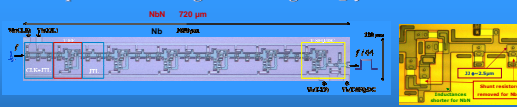


Complete ADC design in RSFQ technology



$J_c = 30 kA/cm^2$ @ 9K
 $I_c R_n = 4.6 mV$
 $I_c R_n = 1.5 \mu s$
 $200 kV_c = 250 \mu s$
 $R_1 \approx R_2 = L_1 = 4.9 \mu H$

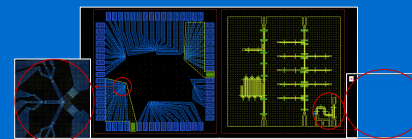
Comparison of NbN gates vs Nb gates @ $J_c = 4.5kA/cm^2$



A 45 JJ frequency divider (F/64) circuit is applied to a relaxed $\phi = 2.5\mu m$, $4.5kA/cm^2$, NbN technology at 9K for comparison to a Nb circuit at $4.2K$ ($4.5kA/cm^2$ Hypres foundry).

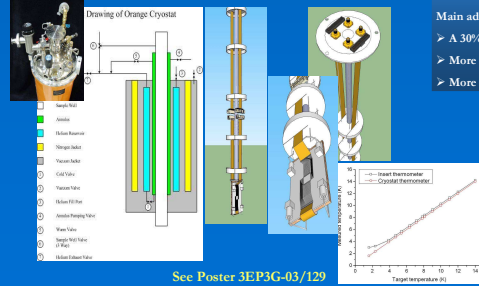
- Main advantages observed in 9K NbN self-shunted technology over 4K Nb arc:
- > A 30% gain in circuit compactness due to self-shunted NbN-TaN-NbN junctions
 - > More than 50% gain in F_n (due to large $R_n I_C$ and to TaN capacitance negligible)
 - > More than 300% gain in the cryocooling power required @ 9K versus 4K

Two chips ($1x1 cm^2$; 64 pads) of test vehicle : arrays of $0.7\mu m$ junctions (left); resonators and anti-aliasing filters



Flexible & semi-rigid connexions in Orange Cryostat.

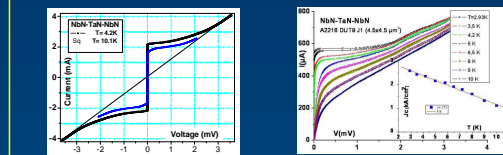
Chip carrier temperature controlled at +/- 0.05K @ 9K



See Poster 3EP3G-03/129

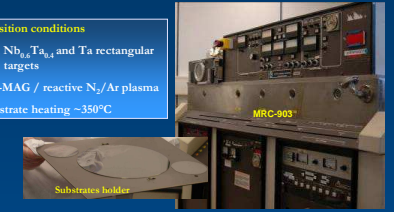
Deposition of superconducting & Nb(Ti)/TaN/NbN JJ layers on 8-inch Si wafers

NbN/TaNx/NbN junctions produced with $R_n I_C$ up to 1.6 mV @ 10K



NbN, Nb_{0.6}Ti_{0.4}N, TaN_x films sputtered on 8-inch Si-SiO₂

- Deposition conditions
- > Nb_{0.6}Ti_{0.4}N and Ta rectangular shape targets
 - > DC-MAG / reactive N₂/Ar plasma
 - > Substrate heating ~350°C

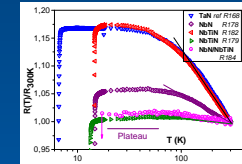
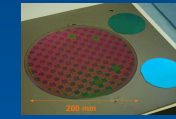


NbN/TaNx/NbN & NbTiN/NbN non-hysteretic SNS junctions produced first on 3-inch wafers and UV-contact lithography (Acatel system) with $R_n I_C$ up to 3.9 mV @ 4.2K / 1.6mV @ 10K with barriers composition and thickness (5-10nm) controlled at the metal-insulator transition

Superconducting properties & resistivity vs temperature for NbTiN and TaN layers on 8-inch Si (MRC-903)

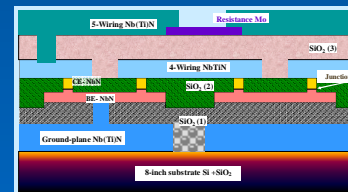
Base-Electrode thickness (nm)	Barrier composition / thickness (nm)	Top-Electrode thickness (nm)	T _c (K)	R/R ₀
NbN 200	TaN10.5% / 4	NbN / 250	15.9	1.44
NbN/NbN	TaN30%	NbN	15.1	2
214 / 148	12	143		
Nb / NbN	TaN30%	NbN	15.1	2.6
283 / 150	8	150		
Nb / NbN	TaN34%	NbN	14.9	2
279 / 161	12	147		
Nb / NbN	TaN34%	NbN	14.9	2.6
276 / 161	8	144		
NbTiN/NbN	TaN34%	NbTiN	14.4	0.85
150 / 150	8	150		

Films uniformity and reproducibility better than 5% on 200mm



Processing junctions & circuits applying the 8-inch/0.3μm rules of C-MOS platform

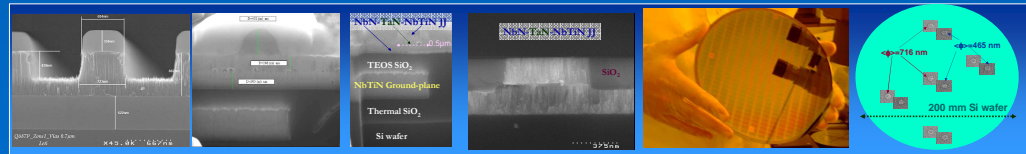
NbN ADC circuit multilayer made on 8-inch Si wafers



NbN ADC circuit processing steps

LAYER	Thickness	DEPOSITION AND PLANARIZATION CONDITIONS
NbTiN (5-WIRE)	650 nm	DC-MAG SPUTTER (Nb _{0.6} Ti _{0.4} N TARGET)
Mo (RE)	40 nm	SPUTTERING @ 200°C, IKW, 3.40H/MSQ
SiO2 (3-BR)	300 nm	CMP ON SiO ₂ (TEOS PECVD @ 350°C)
NbN (4-WL)	500 nm	DC-MAG SPUTTER DEPOSITION FROM A Nb TARGET
SiO2 (2-L)	450 nm	CMP ON SiO ₂ (TEOS PECVD @ 350°C)
NbN (3-CE)	180 nm	DC-MAG SPUTTER (Nb TARGET) @ 0.7 μm JUNCTION BY STEPPER LITHOGRAPHY (ASM300-248nm LINE)
TaN (BARRIERE)	8 nm	DC-MAG SPUTTER (Ta TARGET)
NbN (G-RE)	270 nm	DC-MAG SPUTTER (Nb TARGET)
SiO2 (1-CP)	300 nm	CMP ON SiO ₂ (TEOS PECVD @ 350°C)
NbTiN (G-PLANE)	550 nm	DC-MAG SPUTTER (Nb _{0.6} Ti _{0.4} N TARGET)

Low spread $\phi = 700nm$ ($3\sigma = 40nm$) NbN junction achieved on 200mm Si wafers using stepper lithography and CMP planarization



Summary and perspectives

- > High accuracy patterning of $\phi = 0.7 \mu m$ planar NbN-TaN-NbTiN junctions, thanks to the stepper and to the large $R_n I_C > 1.5mV$ observed at 9K (see talk 1EY01) made the processing of 9K-NbN-ADCs chips on 8 inch Si wafer feasible at low cost.
- > Architecture and cryo-test set-up have been developed & adapted to take benefit of clock frequencies >100GHz & of the reduced overall power dissipation for operating NbN RSFQ functions at about 9K (+/- 0.05K stabilized) in regard to 4K cooled Nb chips.
- > A complete 9K ADC chip is under-development to address applications foreseen in telecoms, astronomy & in medical imaging.