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A New Time-Based Converter Model Applied to Converter Automated Design

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Abstract—This paper presents an accurate virtual prototyping modeling technique for power converter using a time-based approach that overcome the simplification made in analytical models, and constitutes a better alternative for simulator-based models in the domain of validity. The key importance of the approach lies on its simple implementation and genericity, the electrical waveforms are obtained directly from the circuit equation and control sequences giving higher degree of freedom for the modeling process and making it less fastidious compared to analytical model. The model is intended for direct prototyping, hence, a precise wide-band-gap semiconductors model that include information about the thermal cycling is included. A case study for 3-Level multiplex inverter is conducted and experimentally validated with 15kW prototype.

Index Terms—Design Automation, Multi-level Inverter, Optimization.

I. INTRODUCTION

Power electronics converter design by optimization is a well-established and proven technique that assists engineers in making data-driven decisions throughout different design phases, from the early design stage where client requirements are negotiated, to the final design optimization that best respect the objectives trade-offs. The key criteria when formulating the optimization problem resides in defining the model level that achieve the desired accuracy and select the search algorithm that is compatible with the design variables and ensure convergence within acceptable computation time.

A review of the modeling techniques used in power electronics optimization was conducted in [1], the author emphasized the common trend of simplifying the system by representing the time-based electrical waveforms through one or multiple algebraic values, and totally discarding the system dynamic.

Power converter design optimization based on continuous analytical models was conducted in [2]–[4], The model consist of the relaxation of design variables leading to a Pareto of imaginary converters based on fictive components. This

approach offers the main advantage of fast computation time, However, it necessitates extensive post-processing to translate the Pareto design into real-world without compromising the performances. Analytical models based on discrete commercially available devices were used in [5], [6] to obtain a Pareto of feasible designs with existing bill of material. Although, they are very useful for direct prototyping, the development of the analytical equations can be fastidious when multiple converter based on different control strategies are analyzed.

Software-based optimization such Pspice, Psim etc. is used when accuracy is of higher priority [7], [8], the model allows to take into consideration multi-physics phenomena, by coupling multiple software and link them inside an optimization routine. the main drawback of this approach is the computation time, circuit-simulator have transient period before steady state, and in certain case, where the input variables doesn't constitute a realistic design, the convergence is never achieved, which make the approach tedious and hardly robust.

This paper presents a semi-analytical time-based model of power electronic converter suitable for design optimization. The approach achieve the same accuracy as circuit-simulator software, all while eliminating the drawbacks related to the long simulation time, software linking and convergence issue. the derived model waveforms are then utilized to develop precise component performances model with the goal of achieving a Pareto front with optimal designs as close as possible to real prototypes. The proposed model is used to elaborate a power converter design decision tool in Matlab environment, and the optimization will be carried using design variables based on a large library of commercially available components to guarantee feasible designs. The paper is outlined as following. Section II presents the time-based modeling approach. Section III presents the Performances model and experimental validation. Section IV shows the optimization problem results and finally section V synthesize our main findings.

II. PROPOSED TIME BASED MODEL

This section presents the time-based modeling approach for power converter systems. The converter equations are utilized to derive the current and voltage waveforms, which are then used to assess the components losses, performances and constraints

A. Converter model

In power inverter applications, the operating point specification of active power, voltage and current represents the low frequency references that the control needs to achieve. Therefore, the DC-link bus will be modulated accordingly using the active switches that produce output stair waveforms voltage corresponding to the inverter level, in 2 Level inverter the output voltage vary between $+V_{DC}/2, -V_{DC}/2$, in 3 level inverter, the output voltage vary between $+V_{DC}/2, 0, -V_{DC}/2$ and so on. the rectangular output voltage is characterized by a low frequency (LF) component that corresponds to the waveforms targeted by the control loop, and a high frequency (HF) component inherited from the active switches modulation of the DC-link bus. The proposed model aim to reconstruct the inverter current and voltage waveforms from their HF and LF components using the topology equation and control laws. Fig 1 illustrates the philosophy with the green arrows representing the LF components that are imposed by the load and the red arrows representing the HF components caused by the PWM modulation.

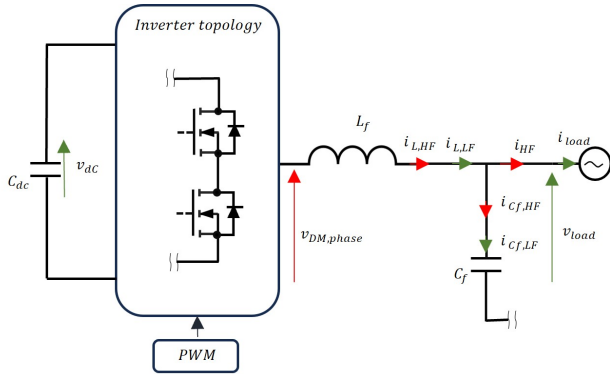


Fig. 1: Power inverter with sine filter :current's LF and HF contributions

The modeling approach is illustrated for 3-level multiplex inverter, also known as Sparse Neutral Point Clamped, with output sinus filter shown in Fig 2. the topology equations and control strategies are presented in [9].

The inverter voltage waveforms shown in Fig 3 are derived as follows : First, the reference voltage in Fig 3 (b) is obtained from the load specifications, taking into consideration LF voltage drop on the inductor. This voltage is then utilized to generate the PWM sequences based on the selected control strategy in order to obtain the inverter output phase voltage in Fig 3 (a). By suppressing the common mode component of the phase voltage we obtain the differential voltage in Fig 3 (c), and from the latter the inductor HF voltage is determined

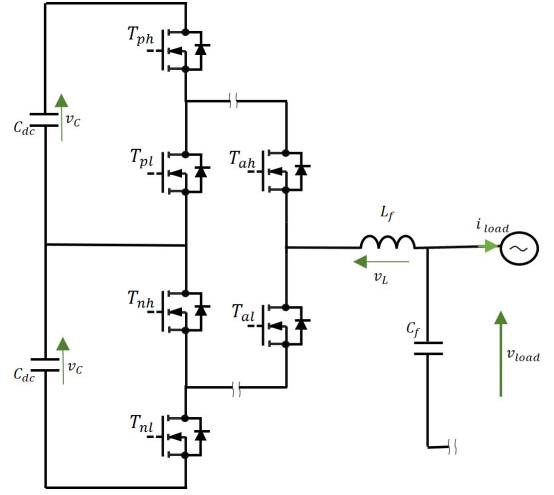


Fig. 2: 3-L multiplex inverter with sinus output filter

as shown in Fig 3 (d). Knowing the inductor HF voltage, the HF current component is derived either by using the flux density waveforms taking into consideration the material saturation curve $B(H)$, N of turns and the core parameters or by simply using the inductor value with the assumption of operating in linear region. The total inductor current is therefore constructed as shown in Fig 4 and used to derive the capacitor, semiconductors and load current.

The derivation and integration operations are done numerically in Matlab using the waveform data, eliminating the necessity to develop analytical equations. Moreover, the space vector modulation (SVM) control function takes the waveforms to generate the PWM, which facilitates the integration of the multiple possible control sequences introduced in [9]

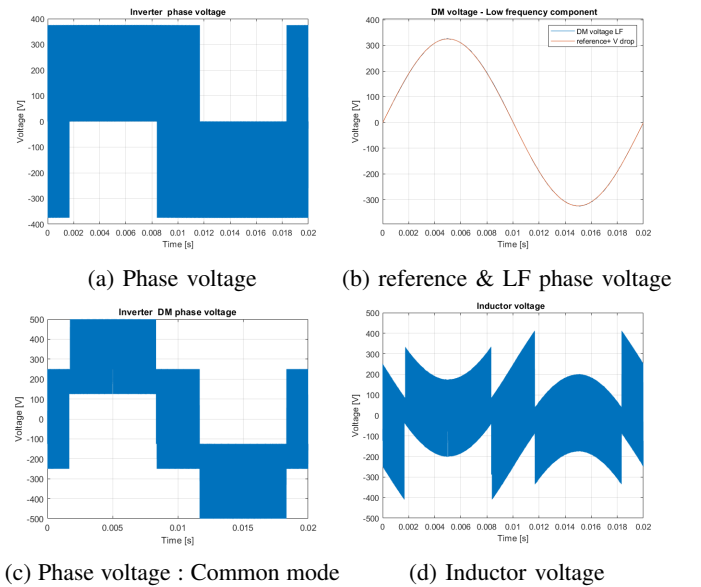
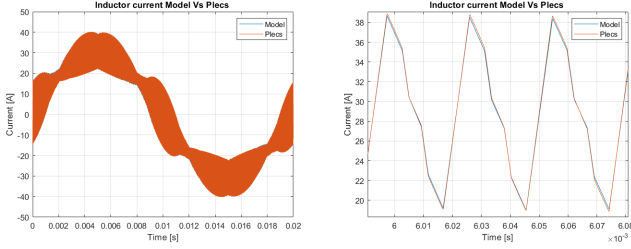


Fig. 3: 3-L multiplexed inverter voltage waveforms - Operating point specifications : $P = 15kW, PF = 1, V_{rms} = 230V, V_{DC} = 750V$

B. Validation with PLECS

The presented approach gives similar results to circuit simulator software in the domain of validity. Fig 4 shows the inductor current waveforms obtained by the model compared to the steady state waveforms of PLECS.



(a) Inductor current Model Vs PLECS (b) Zoom on inductor current PLECS

Fig. 4: results comparison Model and PLECS

The model's validity relies on the assumption of a feasible design with an efficient closed-loop control. The assumptions translate in a balanced sinusoidal output waveforms that meet the reference and stable dc-link capacitor voltage with no currents in the neutral wire. In the automated design program, which will be elaborated in the following sections, a set of constraints on the output voltage ripples, DC-link voltage ripple, and the inductor voltage drop is defined to ensure the validity of the hypothesis.

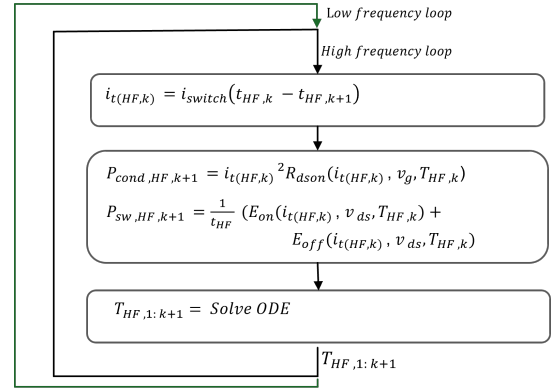
III. PERFORMANCES MODEL

A. Semiconductor model

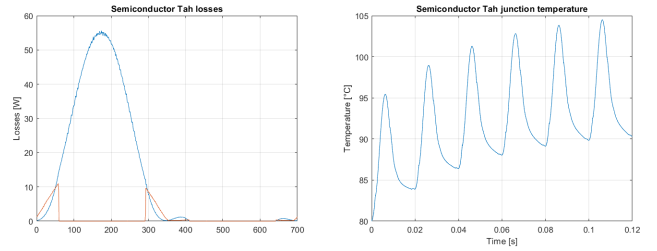
A dynamic electro-thermal model for semiconductors is elaborated to fairly assess the performances of the various references in our library, and to provide information about the temperature ripple, maximum junction temperature rise, switching and conduction loss that are critical to ensure a reliable design. Semiconductors conduction loss are straightforwardly obtained from the R_{dson} equation. However, estimating switching losses precisely using analytical equations is difficult. As a result, various numerical and nonlinear models have been introduced in literature [10]–[13]. A datasheet-based behavioural model of semiconductors based on temporal resolution of half bridge ordinary differential equation (ODE) was introduced in [13] and used in this work. The loss model utilizes the time-based current and voltage waveforms of the semiconductors. At each switching sequence, the conduction and switching losses are evaluated based on the corresponding current, temperature, and blocking voltage. However, solving the ordinary differential equations (ODE) at such frequency is computationally expensive. To address this, the switching loss of each semiconductor reference will be mapped across its operating current and voltage at different temperatures and stored in look-up tables prior to the optimization, reducing computational overhead. On the other hand, the thermal behavior of the semiconductors can be modeled using the transient thermal impedance curve given in the datasheets, the later is

fitted into 4 branch Cauer network, and used to estimate the temperature evolution after each switching event. The heatsink model was not included in this study, therefore, we assume a uniform temperature of $80^{\circ}C$ at the thermal interface material.

Semiconductor electro-thermal loss model is illustrated in Fig. 5 (a), the loss are evaluated at each high frequency period and the junction temperature evolution is obtained by solving Cauer thermal network described through a set of ordinary differential equation. 3-L multiplex inverter semiconductor T_{ah} Fig. 2 losses and junction temperature are shown Fig. 5 (b)-(c). Data about the maximum junction temperature, and temperature ripple will be displayed on the Pareto's points to help in the decision-making process.



(a) code structure



(b) losses over LF period

(c) Temperature evolution

Fig. 5: Semiconductor electro-thermal model

B. Inductor model

The inductors are not catalogue based components, their design depends on the selected magnetic material, core size, winding type, dimensions, and material. For simplicity, this work only considers toroidal cores. The magnetic core loss are obtained using the flux density time-based waveform based on improved generalized Steinmetz equation. The Winding loss are estimated using the fast Fourier transformer of the inductor current based on Dowell equivalent sheets resistance. The detailed inductor model can be found in [14]. Thermal considerations are addressed using constraints on core loss density and current density.

C. Capacitor model

Capacitors are catalogue based, Their loss are obtained using the capacitor current waveforms and the equivalent series

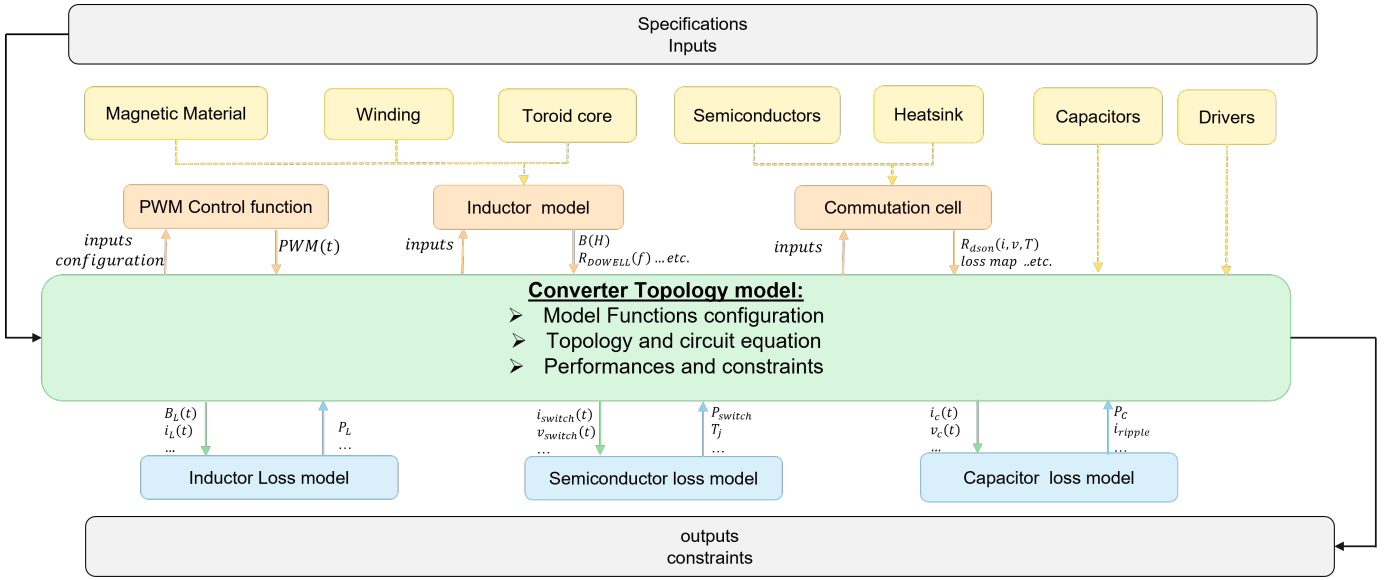


Fig. 6: Optimization problem formulation using the Time-based model

resistance. Thermal constraints are addressed by ensuring that the capacitor current harmonics are below the the maximal allowable current vs frequency curve given in the datasheets.

D. Experimental validation

The presented model was validated with experimental measurements of 15kW 3-level multiplex inverter prototype shown in Fig. 7. The measurements were conducted under the following operating conditions: $V_{DC} = 750V$, $V_{load} = 230V_{rms}$, $\cos(\phi) = 1$, $f_{sw} = 70kHz$

Table I summarizes the measurement data and the simulation results, both conducted using the same configuration and components.

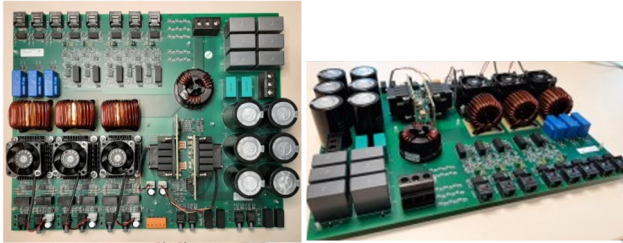


Fig. 7: 3-Level multiplex 15kW prototype

TABLE I: Experimental & model data

Entity	Experimental data	model data	error
Converter efficiency	98.5%	98.77%	0.27 %
Inductor losses	13W	14.8W	13 %
Semiconductor losses	120W	124W	3.33 %

IV. OPTIMIZATION RESULTS

A. Problem formulation

Power converter automated design tool was build using the time-based model. Fig 6 shows an overview of the system formulation, that can be seen as a set of generic independent blocks described through Matlab functions. The green block represents the topology model elaborated in the previous sections and its configurations, such the control fixed parameters , number of commutation cell, DC bus etc. this function is linked to the other blocks through a set of standardized inputs and outputs. Performance model represented by the blue blocks, takes the time-based waveforms data, and component library information to return the losses. Other blocks like the Inductor model and Commutation cell utilize the components dedicated libraries to provide the electrical characteristics of the components.

B. Design variables

Design variables are based on a library of commercially available devices, their paralleling is limited to 6 to guarantee feasible a designs. The variables include ; switching frequency that varies from $10kHz$ to $100kHz$, multiple control strategies, component reference, and their number connected in series and parallel. Different semiconductors variable will be assessed in the multiplexed commutation cell, as they don't have the same electrical stress.

Component library :

- Semiconductor's library : 32 references of SiC and GaN devices, each characterized with their loss-map, $R_{ds on}$, Z_{th} and other corresponding data.
- Magnetic material library : 21 reference of alloys composite, each reference has data about $B(H)$ curve coefficients, loss coefficients etc.

- Winding library : +200 reference of litz and solid wires. With their material being either *Cu* or *Al*
- Capacitor library : 17 reference of electrolytic capacitors and 20 film capacitors.
- Magnetic core library : a list of standard toroidal core sizes.

Table II represents the system constraint that validate the model assumption, other constraints related to device components are also considered.

TABLE II: Optimization Constraints

Entity	Symbol	Unit	Value
Load voltage ripple	\tilde{V}_{load}	V_{rms}	4
DC-link voltage ripple	\tilde{V}_{dc}	%	4
Max Temperature	$T_{j,max}$	C	120
Inductor core loss density		mW/cc	750
Inductor current density		A/mm^2	6 "Cu" & 3 "Al"

C. Optimization results

The optimization process was carried using Grid Elitist Multi-objective genetic algorithm presented in [6]. The optimization objectives are price, loss, and volume. Table III represents the design specifications. The optimization Pareto of the 3-Level multiplex inverter is shown in Fig. 8.

TABLE III: Optimization specification

Entity	Symbol	Unit	Value
Active power	P_a	kW	15
Power factor	$\cos \phi$		0.85
Voltage ref	v_{ref}	V_{rms}	230
DC Bus	V_{DC}	V_{rms}	750
Grid frequency	f_g	Hz	50
Heatsink Temp	T_{hs}	C	80

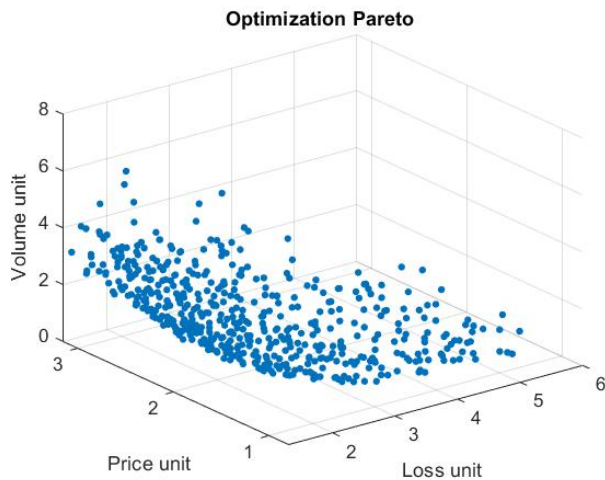


Fig. 8: 3-Level multiplex optimization pareto

Each data set represents a feasible design with its specific bill of materials and performance. The Pareto front accounts

numerous potential optimal designs, making its exploitation a challenging task. To assist designers in navigating these various points in post-processing, we display the different performances of the components as shown in Fig 9- 10. Fig 9 represents the maximum junction temperature of the semiconductor T_{ah} and Fig 10 its corresponding temperature ripple, that is very high in the Pareto region of minimal price at important loss, which make those designs not suitable for certain applications. By displaying critical data on Pareto we guide the designer to make his final choice without requiring further analysis.

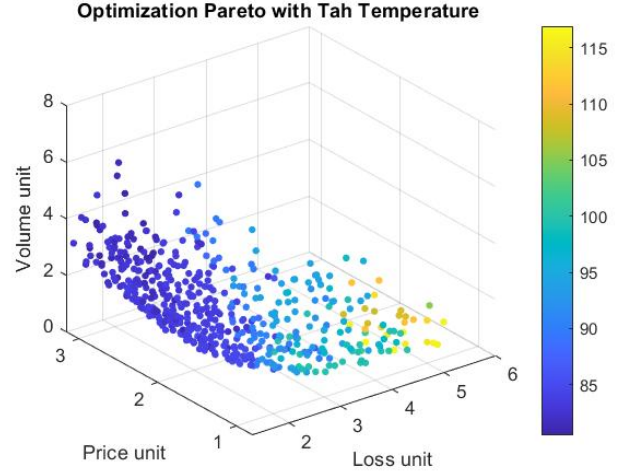


Fig. 9: 3-Level multiplex optimization pareto

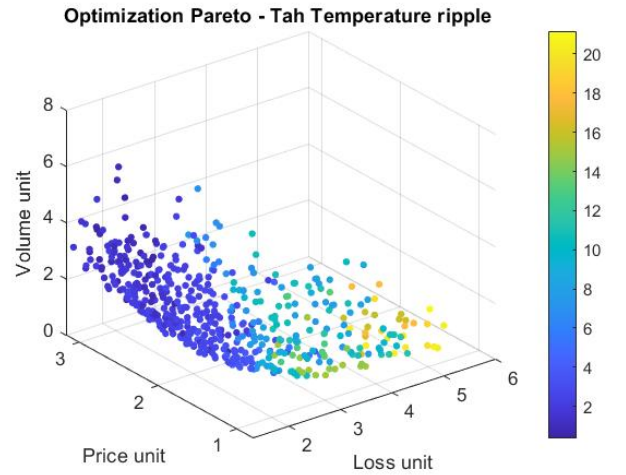


Fig. 10: 3-Level multiplex optimization pareto

V. CONCLUSION

The proposed semi-analytical time-based methodology gives an accuracy comparable to that of circuit simulator software and eliminates certain drawback which make it suitable for final design optimization where accuracy is of higher priority. The wide band gap semiconductors are the

key components when designing power electronics inverter, as they know an important technological advancement compared to other passive components that are already mature, hence, a rigorous modeling is necessary to fairly assess and compare various devices. The Matlab-tool was presented in the case of 3-Level multiplex inverter, and it can easily be generalized to include other topologies, only the topology function needs to be changed, other functions are coded in generic approach.

REFERENCES

- [1] M. Mirjafari and R. S. Balog, "Survey of modelling techniques used in optimisation of power electronic components," *IET Power Electron.*, vol. 7.
- [2] M. Delhommeais, J.-L. Schanen, F. Wurtz, C. Rigaud, and S. Chardon, "First order design by optimization method: Application to an interleaved buck converter and validation," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 944–951.
- [3] A. Stupar, T. McRae, N. Vukadinovic, A. Prodic, and J. A. Taylor, "Multi-objective optimization of multi-level DC–DC converters using geometric programming," *IEEE TRANSACTIONS ON POWER ELECTRONICS*, vol. 34, no. 12.
- [4] A. Voltaire, J.-L. Schanen, B. Sarrazin, and C. Gautier, "Predesign methodology of voltage inverters using a gradient-based optimization algorithm," *IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS*.
- [5] D. O. Boillat, F. Krismer, and J. W. Kolar, "Design space analysis and – pareto optimization of LC output filters for switch-mode AC power sources," *IEEE TRANSACTIONS ON POWER ELECTRONICS*, vol. 30, no. 12.
- [6] T. Delaforge and S. Mariethoz, "Design automation of power electronic converters a grid elitist multiobjective genetic algorithm," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 2892–2899.
- [7] M. S. Zaman, J. K. Mills, C. H. Amon, and O. Trescases, "Multiphysics optimization of thermal management designs for power electronics employing impingement cooling and stereolithographic printing," *IEEE TRANSACTIONS ON POWER ELECTRONICS*, vol. 36, no. 11.
- [8] C. Versèle, O. Deblecker, and J. Lobry, "Multiobjective optimal choice and design of isolated dc-dc power converters," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.
- [9] D. Cittanti, M. Guacci, S. Miric, R. Bojoi, and J. W. Kolar, "Analysis and performance evaluation of a three-phase sparse neutral point clamped converter for industrial variable speed drives," *Electrical Engineering*.
- [10] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for mosfets in a half-bridge," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3700–3710, 2019.
- [11] A. Hu and J. Biela, "An analytical switching loss model for a sic mosfet and schottky diode half-bridge based on nonlinear differential equations," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. P.1–P.11.
- [12] D. Zieba and J. Rabkowski, "Problems related to the correct determination of switching power losses in high-speed sic mosfet power modules," *Bulletin of the Polish Academy of Sciences Technical Sciences*, vol. 70, no. 2, p. e140695, 2022.
- [13] D. Timothe, P. Marco, and D. R. Michael, "Accurate analytical eGaN® HEMT parameterizable matlab® model based on datasheet from manufacturer and its applications in optimal design."
- [14] T. Delaforge, "Optimal sizing of passive components in power converters using discrete methods," PhD thesis, Université Grenoble Alpes, February 2016. [Online]. Available: <https://theses.hal.science/tel-01286290>