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# Reduced probability of noise introduced malfunction in RSFQ circuits by implementing intrinsic $\pi$ -phaseshifter

O. Mielke, T. Ortlepp, P. Febvre and F.H. Uhlmann

**Abstract**—The Rapid Single Flux Quantum electronics family is based on the magnetic flux quantum which is exchanged between adjoining superconducting loops by a switching event of a Josephson junction. This digital circuit family is characterized by a low switching energy, which makes it susceptible to noise introduced bit-errors. For industrial applications a certain noise immunity is required which is still a challenge especially for circuits of higher complexity. Our theoretical analysis showed a significant impact of the phase offset caused by a  $\pi$ -phaseshifter. It can be utilized as a kind of noiseless current source increasing the robustness of RSFQ electronics even for circuits fabricated in mature Nb-technology. We experimentally investigated the influence of the  $\pi$ -phaseshifter on the bit-error rate of a toggle Flip-Flop. We designed dedicated test circuits with and without a phaseshifter for a stability comparison. Our presented experiments show significant variances in the bit error rate confirming the improved immunity against noise. There are only slight differences in the layout of both cells, thus it can be concluded that this advantage is based only on the influence of the phaseshifter. Design and fabrication were performed by FLUXONICS Foundry. **Index Terms**—thermal noise, circuit design, bit-error rate,  $\pi$ -phaseshifter, RSFQ

## I. INTRODUCTION

The Rapid Single Flux Quantum (RSFQ) electronics is an naturally digital circuit family where the information is represented by the magnetic flux quantum  $\Phi_0 = h/2e$  with the Planck's constant  $h$  and the elementary charge  $e$  [1]. There are three sets of parameters defining the functionality of standard RSFQ circuits namely inductances, bias currents and the critical currents of the Josephson junctions. Based on them three basic blocks for transmission, decision and storage can be constructed

[2]. A stored datum is represented by the presents or absence of a flux quantum in a superconducting loop. The Josephson junction is the active element allowing the controlled exchange of flux quanta between adjoining loops. This information transfer is distinguished by a short voltage pulse thus RSFQ is pulse driven electronic. Consequently the capability of temporary data storage is essential for every logic device to avoid timing problems caused by the short duration of the voltage signal.

A loop which is able to store a flux quantum is a naturally tristable system [3], thus a bistable characteristic has to be created artificially. The conventional methodology is to implement a bias current source to remove one of the three stable states. Often this current has to be injected between the junction pair of a comparator which is a spot very sensitive to any parameter variations. This is a drawback for the resulting device restricting the region of operation. An alternative approach which avoids this negative influences based on the implementation of phase shifting elements to establish a bistable characteristic as mentioned in [4].

The first realizations of RSFQ circuits with a phase shifting element delivered promising results in terms of an improved stability against parameter variations associated to the fabrication process [5]. Nevertheless until now there were no investigations concerning the influence of phase shifting elements on the noise susceptibility of an RSFQ basic cell done. In this work we analyze and compare the noise immunity of a bistable logic device with and without phase shifting element. We will focus on approaches which can be realized in a standard Nb fabrication process.

## II. PHASE SHIFTING ELEMENTS

Phase shifting elements can be accounted as a fourth novel component of RSFQ electronics. There are several approaches leading to such an additional element, a detailed overview is given in [6]. Some of them can be easily integrated into standard mature Nb fabrication processes whereas others require new technologies. A well known way to create a phase shift is a constant

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current flowing through an inductance. This technique was already used in the early stages of RSFQ electronics [7]. To implement it into a standard RSFQ circuit an external negative bias source is required.

Another concept, which is based on a trapped magnetic flux in a superconducting ring, was proposed in [8]. The corresponding circulating current creates an total phase shift of  $2\pi$  inside the loop. That means if one connect it in  $180^\circ$  opposite directions a phase shift of  $\pi$  is build. Thus this structure is called  $\pi$ -phaseshifter. It was already implemented and successfully demonstrated in an RSFQ circuit [9]. The structure, as illustrated in Fig. 1, was implemented into a toggle Flip-Flop (TFF) substituting the storing inductance. The advantage of this technique is that neither a technology modification nor an enhancement of the external test setup, in terms of modified external bias sources, is required.

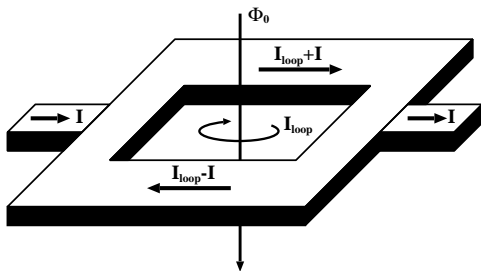


Fig. 1. Topology of a  $\pi$ -phaseshifter with a frozen magnetic flux quantum inside.

More concepts to create a certain phase shift are based on  $\pi$ -junctions. They behave like Josephson junctions with a negative critical current  $I = -I_c \sin(\varphi)$ . That means the current-phase relation has a constant phase shift of  $\pi$  compared to a Josephson junction  $I = I_c \sin(\varphi - \pi)$ . Currently there are two different approaches known suitable for an application in RSFQ electronics. Both of them require a special fabrication technology. Based on the d-wave symmetry of YBCO it is possible to create a superconducting ring with an intrinsic phase offset of  $\pi$  as experimentally shown in [10]. A successful implementation of those  $\pi$ -rings in RSFQ electronics fabricated in a HTS-LTS hybrid technology was demonstrated in [5].

A lumped element  $\pi$ -junction can be fabricated using a ferromagnetic material within the junction barrier. Depending on the thickness of this barrier a standard Josephson junction or a  $\pi$ -junction can be constructed [11].

Regardless of which strategy for creating a phase shift is used a great benefit for the stability of the operating point of a storage device can be expected as shown

in [3]. The goal of this work was to separate the influence of the phase shifting elements. Thus only the approaches applicable for standard Nb-technology were investigated. For this purpose different types of a TFF were designed and fabricated on the same chip.

### III. TOGGLE FLIP-FLOP REALIZATIONS WITH DIFFERENT KIND OF PHASE SHIFTING ELEMENTS

The TFF is a well known bistable logic cell and it has often been the subject of studies. It was the first demonstrated RSFQ basic cells [7] and it is today the device with highest ever measured clock frequency of 770GHz [12]. Also various experiment and simulation studies concerning the bit-error rate (BER) for high temperature superconductors were reported in [13].

We are going to compare the influence of different kinds of phase shifting elements on this standard device. For this purpose a TFF-frame with two output was designed. The input and output ports are connected to Josephson transmission lines to avoid interactions with adjoining cells. The layout was optimized for the  $1\text{kA}/\text{cm}^2$  fabrication process of FLUXONICS Foundry [14] and was designed in a way that the phase shifting element in the core can be adapted easily. The differences between the types have been reduced as much as possible to ensure that variations of the behavior are mainly caused by the phase shifting element. Three types of TFFs were designed whose schematic diagram is illustrated in Fig. 2. While version B and C have completely identical parameter, in version A some changes were necessary to ensure a stable functionality.

The core of the TFF is composed of two comparators (J4, J2) and (J5, J3) coupled by the inductance  $L$ . An incoming flux quantum, which enters the cell by passing through J1, triggers a pairwise switching of J2/J5 or J3/J4 depending on the state of the device. This state is represented by the magnetic flux stored in the loops J2-L-J3 and J4-L-J5.

The micrograph of the standard TFF layout and the TFF with a  $\pi$ -phaseshifter is shown in Fig. 3.

### IV. SIMULATION BASED ANALYSIS

We accomplished simulation studies by utilizing the circuit simulator program J-SIM [15] with the noise model implemented by J. Satchell [16]. The equivalent circuit of the TFF is more extensive than shown in Fig. 2 since the parasitic inductances are not shown. Furthermore there is no model for a phase source implemented in JSIM thus the  $\pi$ -phaseshifter has been constructed by other. We used the equivalent circuit illustrated in Fig. 4 like described more detailed in [6]. The current sources

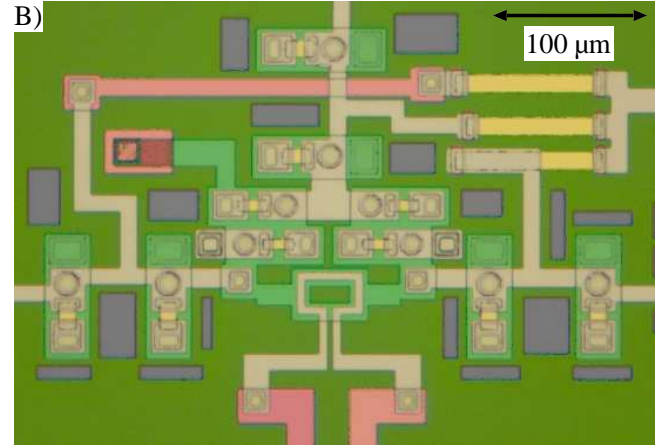
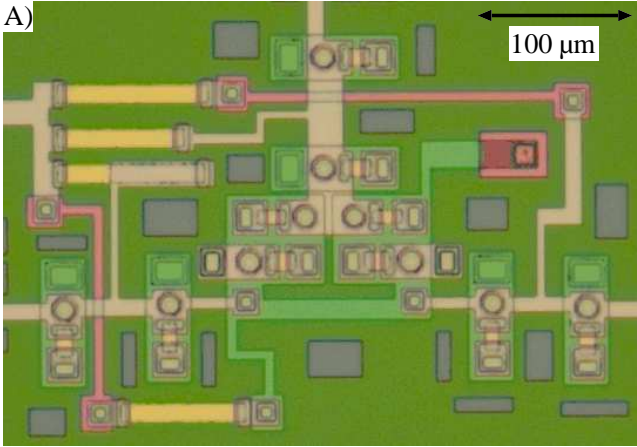


Fig. 3. Micrograph of the standard TFF layout (A) and the TFF with a  $\pi$ -phaseshifter (B) according to the diagram illustrated in Fig. 2.

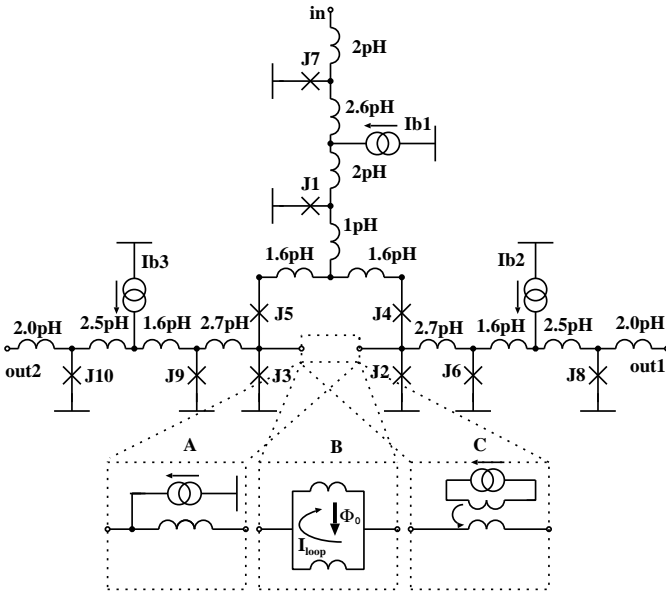


Fig. 2. The schematic diagram of the TFF with different kinds of phase shifting elements creating the storing capability. The critical current of the junctions are  $200\mu\text{A}$ :J6/J7;  $250\mu\text{A}$ :J7/J8/J10 those are identical in every realized type. In version B and C all of the junctions are identical  $225\mu\text{A}$ :J1;  $150\mu\text{A}$ :J4/J5;  $125\mu\text{A}$ : J2/J3. In version A the critical current of the junction need to be varied to establish a stable functionality of the cell ( $175\mu\text{A}$ :J1/J5;  $200\mu\text{A}$ :J4;  $300\mu\text{A}$ :J2; $325\mu\text{A}$ :J3).

are estimated by a resistor and a 2.5 mV voltage source. This source is assumed to be noiseless, but the Johnson noise generated by the resistors was considered.

#### A. Fabrication yield analysis

We compared the TFF realizations in terms of the immunity against parameter variations associated to the fabrication process based on the Monte Carlo Method. Therefore 5000 parameter-sets containing normal distributed random values with a standard deviation of  $\sigma$  around the design center were simulated and checked

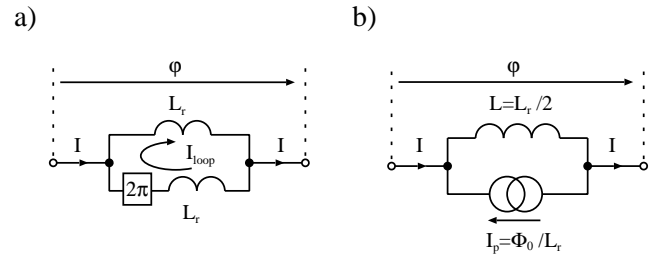


Fig. 4. a) The schematic diagram of the  $\pi$ -phaseshifter and b) the equivalent circuit used for simulation studies with J-SIM.

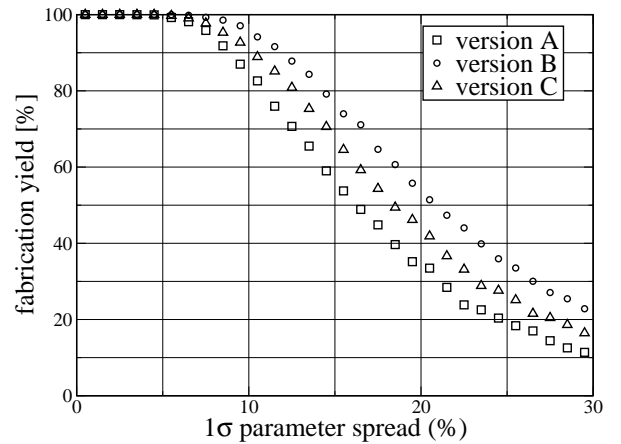


Fig. 5. Simulation of the expected fabrication yield for different types of a TFF realizations. The critical current, bias current and global inductance are normal distributed around there design value with a certain standard deviation  $\sigma$ .

concerning a correct operation automatically. For the inductances a global scaling coefficient was assumed while all other parameters were separately calculated. The results of this investigation are shown in Fig. 5.

As a result of the analysis we found an enhanced stability against parameter variations by implementing a phase shifting element. Furthermore we found a difference in robustness with respect to the phase source. The

reason is that in version C also the element which defines the function, namely the current source which establish the phase shift, is influenced the deviation caused by the fabrication. This is in contrast to the  $\pi$ -phaseshifter (version B) which generates the intend phase shift as long as both branches of the loop in Fig. 4a have the same inductance  $L_T$ .

### B. Bit-error rate analysis

We compared the TFF realizations also in terms of their noise susceptibility. There for the BER was evaluated. The critical currents and the inductance values were assumed with their design value, while the bias current of the TFF was varied. The increment was chosen in a way to have at least 30 steps within the transition region between function and no-function. 10.000 clock cycles with a clock frequency of 5GHz were simulated per step. In Fig. 6 the ratio of the number of switching errors and the number of clock cycles namely the bit error rate (BER) is illustrated. The error rate as a function of the bias current  $I_b$  is well described by the error function according to

$$\text{BER} = 0.5 + 0.5 \cdot \text{erf} \left( \sqrt{R/8k_BTB} (I_b - I_m) \right). \quad (1)$$

The parameter  $I_m$  is the bias current where the error rate

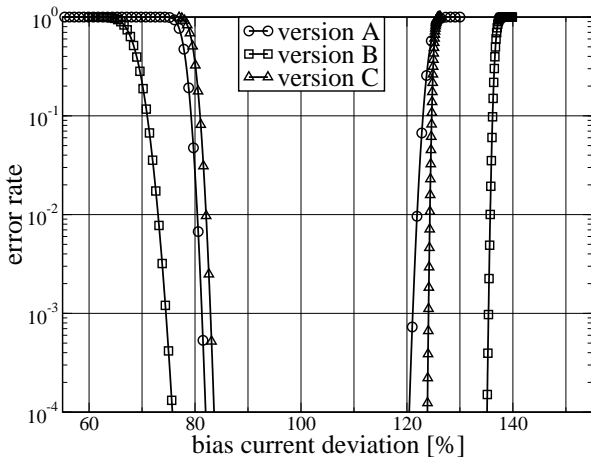


Fig. 6. The bias current dependency of the bit-error rate of different TFF realizations. The curve was evaluated by simulations

becomes  $\text{BER}=0.5$ . The slope of this function depends on the factor  $\sqrt{\frac{R}{8k_BTB}}$ , with the bandwidth  $B$  of the system, the resistance  $R$ , the Boltzmann constant  $k_B$  and the Temperature  $T$ . This slope is an indicator for the susceptibility of the circuit to noise. As smaller the factor is, as higher is the slew rate of the curve and as lower is the noise influence. In Fig. 6 the noise temperature of 4.2 K was used in simulations. Thus the different slopes are a result of different circuit characteristics.

The transition from no-function to function for rising current values  $I_b$  shall named as falling slope while the backward transition will called rising slope. The simulations shows nearly the same slew rate for the falling slope in each version. In contrast to the rising slope which is clearly sharper in TFF version B/C then in version A. This is an indicator of the advanced circuit robustness against thermal noise influence caused by phase shifting elements.

### C. Sensitivity analysis

To detect the component with largest influence on the circuit behaviour a sensitivity analysis was done for each on-chip noise source. These are the resistors used for shunting the junctions and those for bias current distribution. It can be expected that a certain noise power will influence the circuit behavior in different ways depending on the spot the power is inserted. For example it is well known that a comparator is especially susceptible to noise. To gain a quantitative information about that sensitivity, the number of switching errors in a certain operation point was analyzed. According to Fig. 7 the bias current value  $I_b$  was set to obtain  $\text{BER} \approx 1\%$ . The concrete number of switching errors was calculated ten times with  $10^5$  clock cycles each and averaged to minimize random fluctuations. The noise temperature was set to 4.2K for each resistor. In the second step

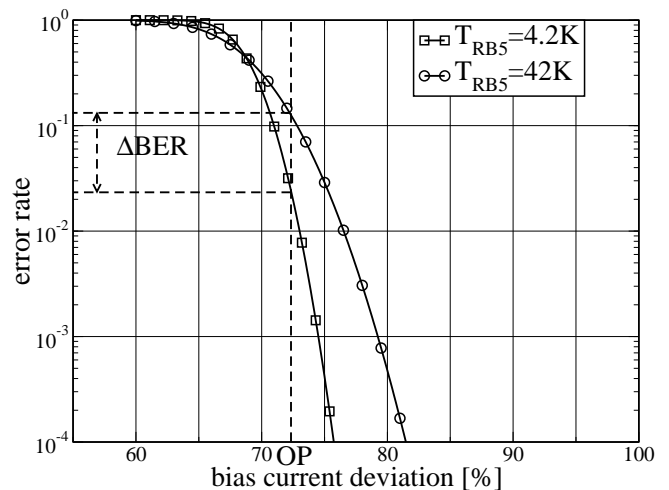


Fig. 7. Overview of the methodology for evaluating the sensitivity of a circuit to on chip noise sources

the noise temperature of one resistor was artificially tenfold increased to 42 K. Again ten simulation runs were performed and the increase of BER was calculated. This method was done for every resistor. The results are displayed in Fig. 8. For the resistors of the current sources  $I_{b1}$ - $I_{b3}$  and the shunt resistors of J7/J9 we found

no change of the BER like at junction J1, thus they are not shown. That the BER is mainly influenced by the

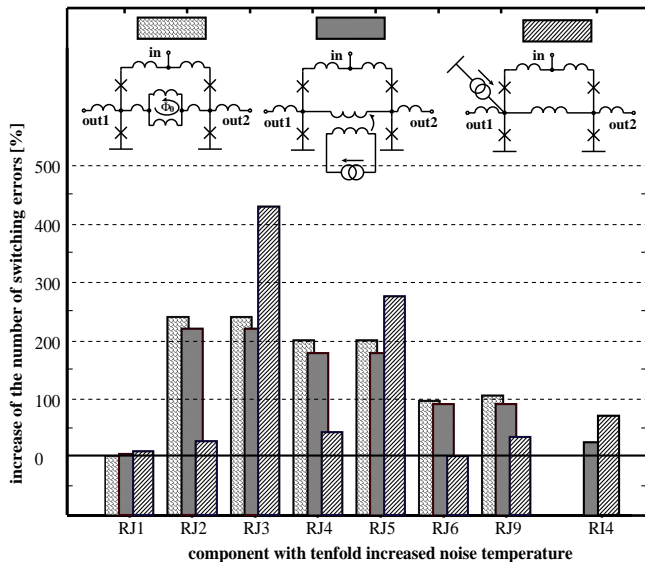


Fig. 8. Increasing of the BER in a certain point of operation by artificially tenfold increased noise temperature of a single resistor. RJ\* are the shunt resistors of the junctions according to the identifier illustrated in Fig. 2. RI4 is the resistor utilized to establish bias current  $I_{b4}$ .

shunt resistors is one new results of this analysis. While the on-chip resistors of the bias currents sources have barely influences. Furthermore the device is particular susceptible to the noise of the resistor of the comparator junctions. An important finding is that in the standard TFF (version A) obviously the comparator (J3/J5) has more influence on the cell behaviour than the other (J2/J4). Because both comparators are coupled it should be possible to change the shunt resistance of the junction J3 and J5 without to jeopardize the functionality of the cell. So we propose to optimize those shunts concerning there generated noise.

## V. EXPERIMENTAL BIT-ERROR RATES

To test the devices experimentally each TFF has been embedded in an environment composed of an input (DC/SFQ-converter) and an output (SFQ/DC-converter) interface. According to Fig. 9 four JTLs were used to avoid interactions between the interfaces and the device under test. The output signal of the RSFQ circuit boosted by a semiconducting amplifier performing a gain of 80dB. The BER analysis was performed by a DSP which is generated the 50 kHz input signal and measured the output signal of the RSFQ circuit to count the number of switching errors. A PC system is used controlling the DSP and the bias current sources. For the TFF version A and B illustrated in Fig. 3 the BER versus their bias

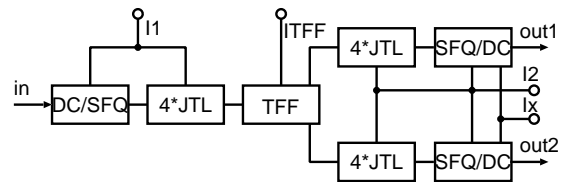


Fig. 9. Block diagram of the setup used to analyze the TFF experimentally

current  $I_{TFF}$  was measured. The transition area and the area of operation was passed through with  $1\mu A$  increment varying the value of TFF bias current  $I_{TFF}$ . For each step  $10^5$  switching events were tested. The results are displayed in Fig. 10. The analyzed circuits were fabri-

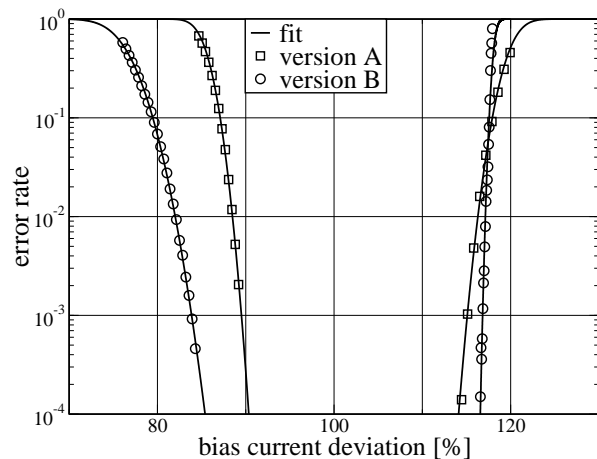


Fig. 10. The experimentally evaluated bias current dependency of the bit-error rate of TFF. The fitting curves are obtained by using Eq.(1).

cated on the same chip and we used the same setup for the experiments thus the effective noise temperature can be assumed to be the same. Based on measurements and simulations we estimated the effective noise temperature with  $T = 6.5$  K. We evaluated experimentally a wider operation region for the TFF containing a  $\pi$ -phaseshifter. Furthermore we measured a significant higher slew rate especially of the raising slope for this device. This indicates clearly an advanced robustness against thermal noise. We found a good agreement between simulations and experiments.

It is worth to mentioned that the used configuration of the  $\pi$ -phaseshifter we used it is not assured to trap a single flux quantum each time. We used a special initial current to create a magnetic field during the cool down process to encourage the implementation of a flux quantum into the  $\pi$ -phaseshifter. There is only a chance to monitor a correct function if an odd number of flux quanta is trapped inside the  $\pi$ -phaseshifter. The chance to trap a flux quantum could be varied by the amplitude of the

initial current. In the best case we trapped in 50% the attempts an odd number of flux quanta. Once initialized the functionality remains until we leave the superconducting state. To guarantee a distinct characteristic the ring has to be designed in a reasonable way to guarantee only one single flux quantum can be trapped [17]. However the positive effects of the  $\pi$ -phaseshifter is worth to work on this problem.

## VI. CONCLUSIONS

We designed and analyzed by simulations and experiments different types of a bistable device (TFF) fabricated at FLUXONICS Foundry. The differences between the TFF types have been reduced as much as possible to ensure that differences of the behaviour is caused only by the kind of the utilized phase shifting element. Thereby the realization with the  $\pi$ -phaseshifter was the best one concerning the stability versus parameter spread associated to the fabrication process and the robustness against influence of noise. A reduced probability of noise introduced malfunction compared to the standard TFF was observed for every realization containing a phase shifting element. Furthermore we simulated the sensitivity of the TFF types to each on-chip noise sources. We identified the resistors with the main influence on the bit-error rate and we show that the on-chip resistor of the current sources has barely influences. The conventional TFF realization is mainly affected by one specific comparator and we propose to optimize them concerning their generated noise.

## VII. ACKNOWLEDGMENTS

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## REFERENCES

- [1] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson junction technology for subterahertz-clockfrequency digital systems," *IEEE Trans. Appl. Superconductivity*, vol. 1, no. 1, p. 327, 1991.
- [2] D. K. Brock, E. K. Track, and J. M. Rowell, "Superconductor ICs: the 100GHz second generation," *IEEE Spectrum*, vol. 37, no. 12, p. 4046, 2000.
- [3] T. Ortlev, Ariando, O. Mielke, C. J. M. Verwijs, A. Andreski, H. Rogalla, F. H. Uhlmann, and H. Hilgenkamp, "RSFQ circuitry using intrinsic  $\pi$  phase shifts," *IEEE Trans. Appl. Superconductivity*, vol. 17, no. 2, p. 659663, 2007.
- [4] A. V. Ustinov and V. K. Kaplunenko, "Rapid singleflux quantum logic using  $\pi$  shifters," *Applied Physics Letters*, vol. 94, no. 8, p. 54055407, 2003.
- [5] T. Ortlev, Ariando, O. Mielke, C. J. M. Verwijs, K. F. K. Foo, H. Rogalla, F. Uhlmann, and H. Hilgenkamp, "FlipFlopping fractional flux quanta," *Science*, vol. 312, no. 5779, p. 14951497, 2006.
- [6] O. Mielke, T. Ortlev, B. Dimov, and F. H. Uhlmann, "Phase engineering techniques in superconducting quantum electronics," *Journal of Physics*, vol. 97, p. 12196, 2008.
- [7] V. K. Kaplunenko, M. I. Khabipov, K. K. Likharev *et al.*, "Experimental study of the RSFQ logic elements," *IEEE Trans. on Magnetics*, vol. 25, no. 2, p. 861864, 1989.
- [8] J. B. Majer, J. R. Butcher, and J. E. Mooij, "Simple phase bias for superconducting circuits," *Applied Physics Letters*, vol. 80, no. 19, p. 36383640, 2002.
- [9] D. Balashov, B. Dimov, M. Khabipov, T. Ortlev, D. Hagedorn, A. B. Zorin, F. I. Buchholz, F. H. Uhlmann, and J. Niemeyer, "Passive phase shifter for superconducting Josephson circuits," *IEEE Trans. Appl. Superconductivity*, vol. 17, no. 2, p. 142145, 2007.
- [10] D. A. Wollmann, D. J. V. Harlingen, W. C. Lee, D. M. Ginsberg, and A. Leggett, "Experimental determination of the superconducting pairing state in YBCO from the phase coherence of YBCOPb dc SQUIDs," *Physical Review Letters*, vol. 71, no. 13, p. 21342137, 1993.
- [11] V. V. Ryazanov, V. A. Oboznov, A. Y. Rusanov, A. V. Veretenikov, A. A. Golubov, and J. Aarts, "Coupling of two superconductors through a ferromagnet: Evidence for a  $\pi$  junction," *Physical Review Letters*, vol. 86, no. 11, p. 24272430, 2001.
- [12] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-Flip-Flop operating up to 770 GHz," *IEEE Trans. Appl. Superconductivity*, vol. 9, no. 2, p. 32123215, 1999.
- [13] M. Jeffery, P. Y. Xie, S. R. Whiteley, and T. V. Duzer, "Monte Carlo and thermal noise analysis of ultrahighspeed high temperature superconductor digital circuits," *IEEE Trans. Appl. Superconductivity*, vol. 9, no. 2, p. 40954098, 1999.
- [14] "FLUXONICS Foundry for design and fabrication of RSFQ circuits", <http://www.fluxonicsfoundry.de>.
- [15] E. S. Fang and T. Van Duzer, "A Josephson integrated circuit simulator (JSIM) for superconductiv electronics application," *ISEC'89*, p. 407410, June 1989, Tokyo.
- [16] J. Satchell, "Limitations on HTS single flux quantum logic," *IEEE Trans. Appl. Superconductivity*, vol. 9, no. 2, p. 38413844, 1999.
- [17] B. Dimov, D. Balashov, M. Khabipov, T. Ortlev, F.-I. B. A. B. Zorin, J. Niemeyer, and F. H. Uhlmann, "Implementation of superconductive passive phase shifters in high-speed integrated rsfq digital circuits," *Supercond. Sci. Technol.*, vol. 21, no. 4, p. 45007, 2008.