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# Inductance extractions for low- and high-T<sub>c</sub> technology SFQ circuits in absence of superconducting ground plane

C. J. Fourie<sup>1</sup>, R. Collot<sup>2</sup>, P. Febvre<sup>2</sup>, N. Bergeal<sup>3</sup>, J. Lesueur<sup>3</sup>, J. Kunert<sup>4</sup> and H.-G. Meyer<sup>4</sup>

1) Department of Electrical and Electronic Engineering, Stellenbosch University, South Africa

2) Laboratoire Hyperfréquences et Caractérisation – UMR 5130 CNRS, University of Savoie, France

3) Laboratoire de Physique et d'Étude des Matériaux - UMR 8213 ESPCI-UPMC-CNRS, Paris, France

4) Department of Quantum Detection, Institute of Photonic Technology, Jena, Germany

## Introduction

For SFQ circuits without ground planes (such as most high- $T_c$  circuits), inductance calculation is not trivial [1, 2].

Similar calculation complexities are introduced when the ground plane is partially removed in low- $T_c$  circuits [3, 4].

With InductEx [5] verified for ground-plane-hole circuit design [4] in low- $T_c$  circuits, we now apply it to high- $T_c$  circuits.

We show that InductEx performs well for HTS monolayer SQUID structures (which can be measured), and develop a model to handle HTS monolayer RSFQ circuits.

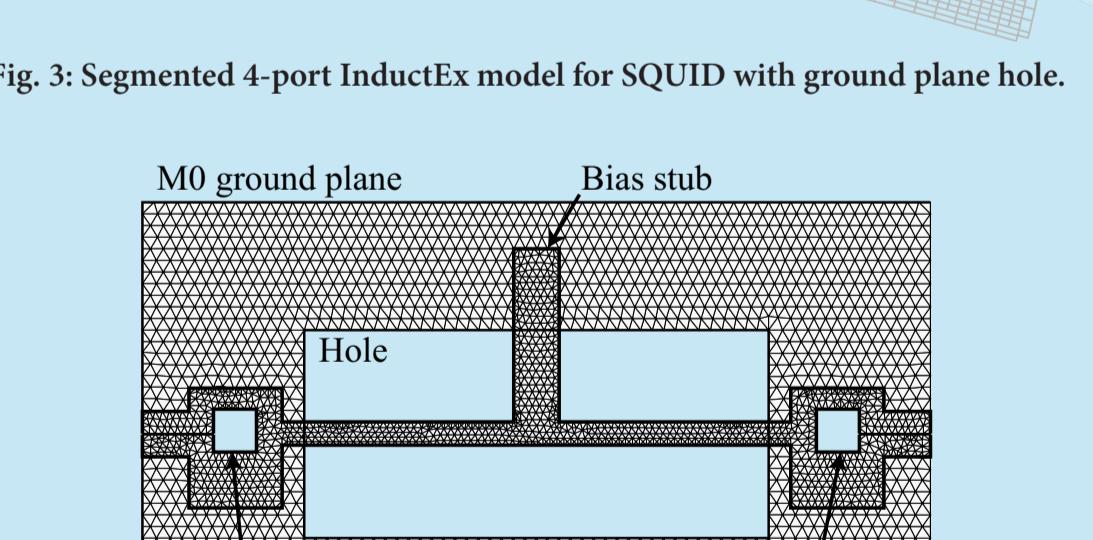
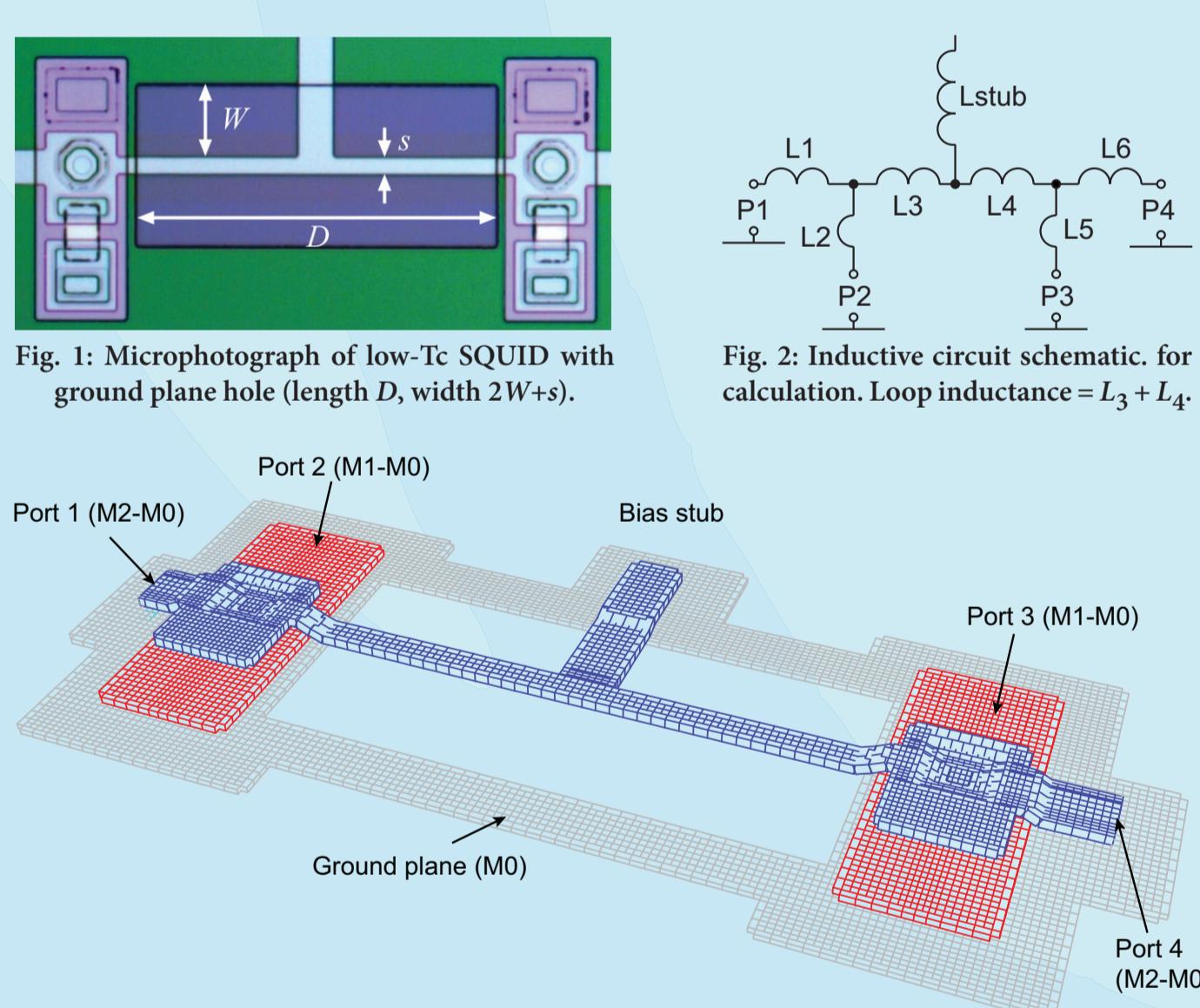
## Holes in ground plane

For low- $T_c$  circuits, such as those in the FLUXONICS RSFQ process from IPHT [6] which has a ground plane layer, holes may be used to increase inductance (or coupling).

For a SQUID with loop inductor over a ground plane hole (Fig. 1), we use a 4-port model (Fig. 2) in InductEx (Fig. 3) to calculate the loop inductance [4].

Over a range of test structures (measured through SQUID modulation), InductEx calculations agrees with measurements with an RMSE < 2.2 % [4].

We compared 3D-MLSI [7] to InductEx by building a 2-port model of the same holed structures (Fig. 5). The results are very consistent, and we proceed to use InductEx and 3D-MLSI for monolayer structures with confidence (provided that similar modeling is used!).



**InductEx Homepage:**  
[www.sun.ac.za/inductex](http://www.sun.ac.za/inductex)

## Monolayer inductance

For a monolayer high- $T_c$  process (70 nm YBCO with ion-irradiated junctions [8], we firstly establish the validity of a modeling technique through the comparison of calculations with SQUID modulation measurements.

Manufactured SQUIDs (Fig. 5) are modeled with a partial-element equivalent circuits (PEEC) technique [9] (no ground return path provided) as shown Fig. 6.

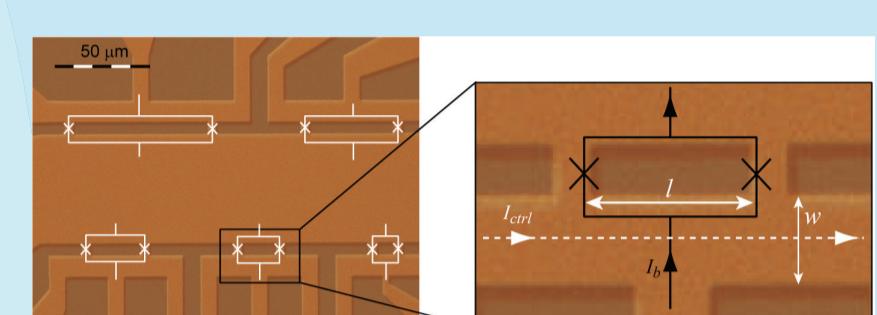
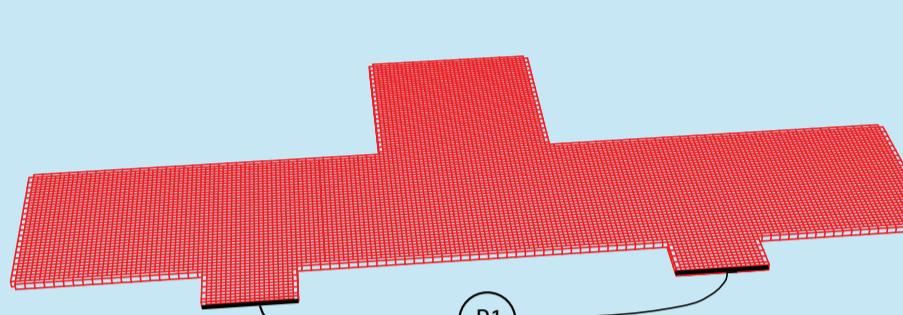


Fig. 5: Monolayer SQUIDs (with ion-irradiated junctions).



## Calculation results

3D-MLSI, InductEx and analytical calculation results for the monolayer SQUIDs are shown in Fig. 7 and Fig. 8. [8]. YBCO of thickness 70 nm and penetration depth 185 nm is used. Analytical calculations are based on the telegraphist's equation [10].

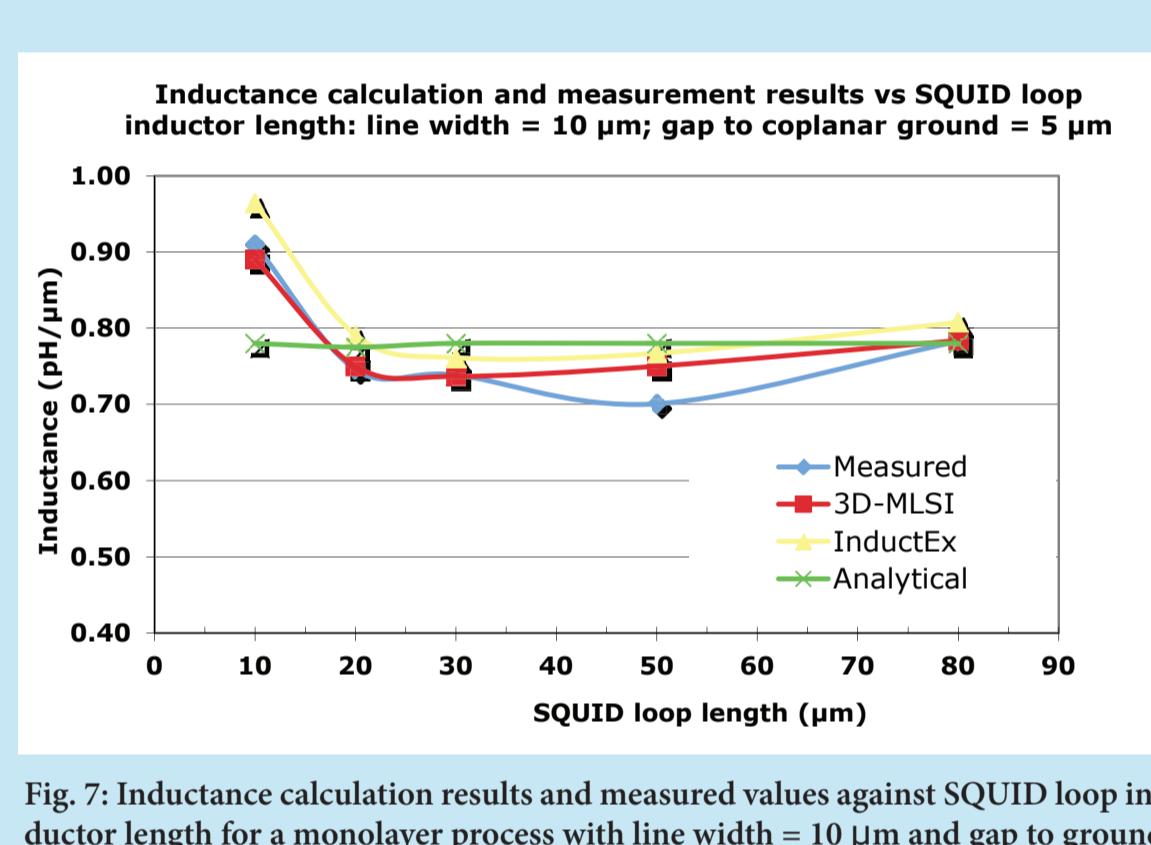


Fig. 7: Inductance calculation results and measured values against SQUID loop inductor length for a monolayer process with line width = 10  $\mu\text{m}$  and gap to ground line = 5  $\mu\text{m}$ .

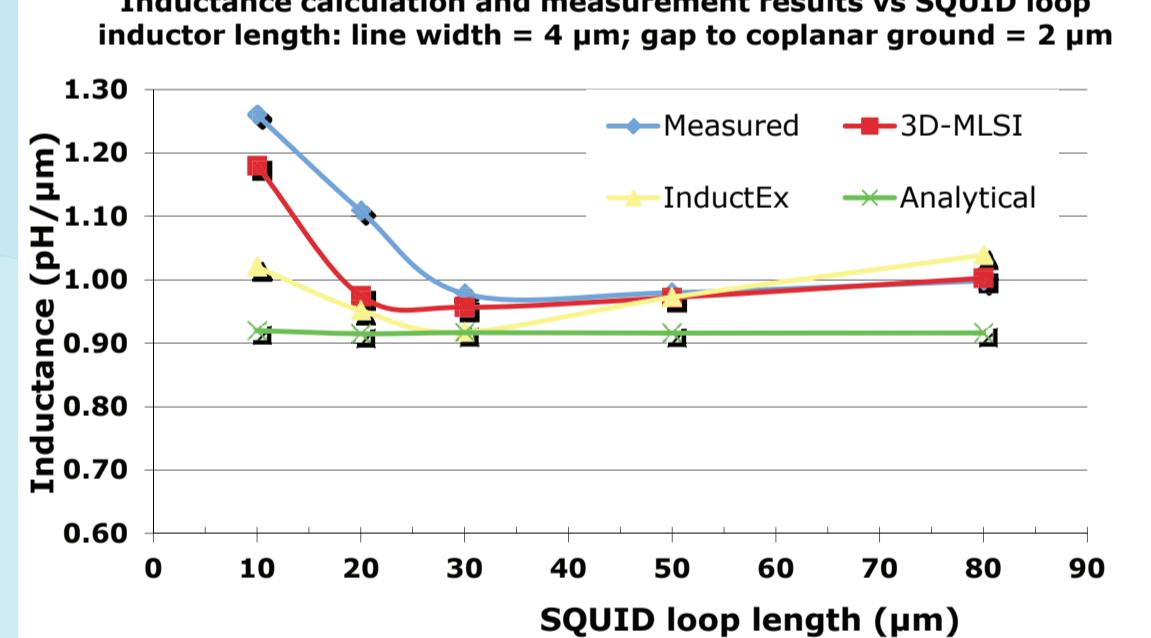


Fig. 8: Inductance calculation results and measured values against SQUID loop inductor length for a monolayer process with line width = 4  $\mu\text{m}$  and gap to ground line = 2  $\mu\text{m}$ .

## Modeling more layouts with more complex netlists

For more complex netlists, modeling with PEEC inductors is insufficient (we need to know the parasitic inductance of junction arms).

A multi-port model is first tested on a SQUID with known measurement results (Fig. 9), and gives consistent results when a port on the bias stub is connected to ground as shown (Voltage source 5).

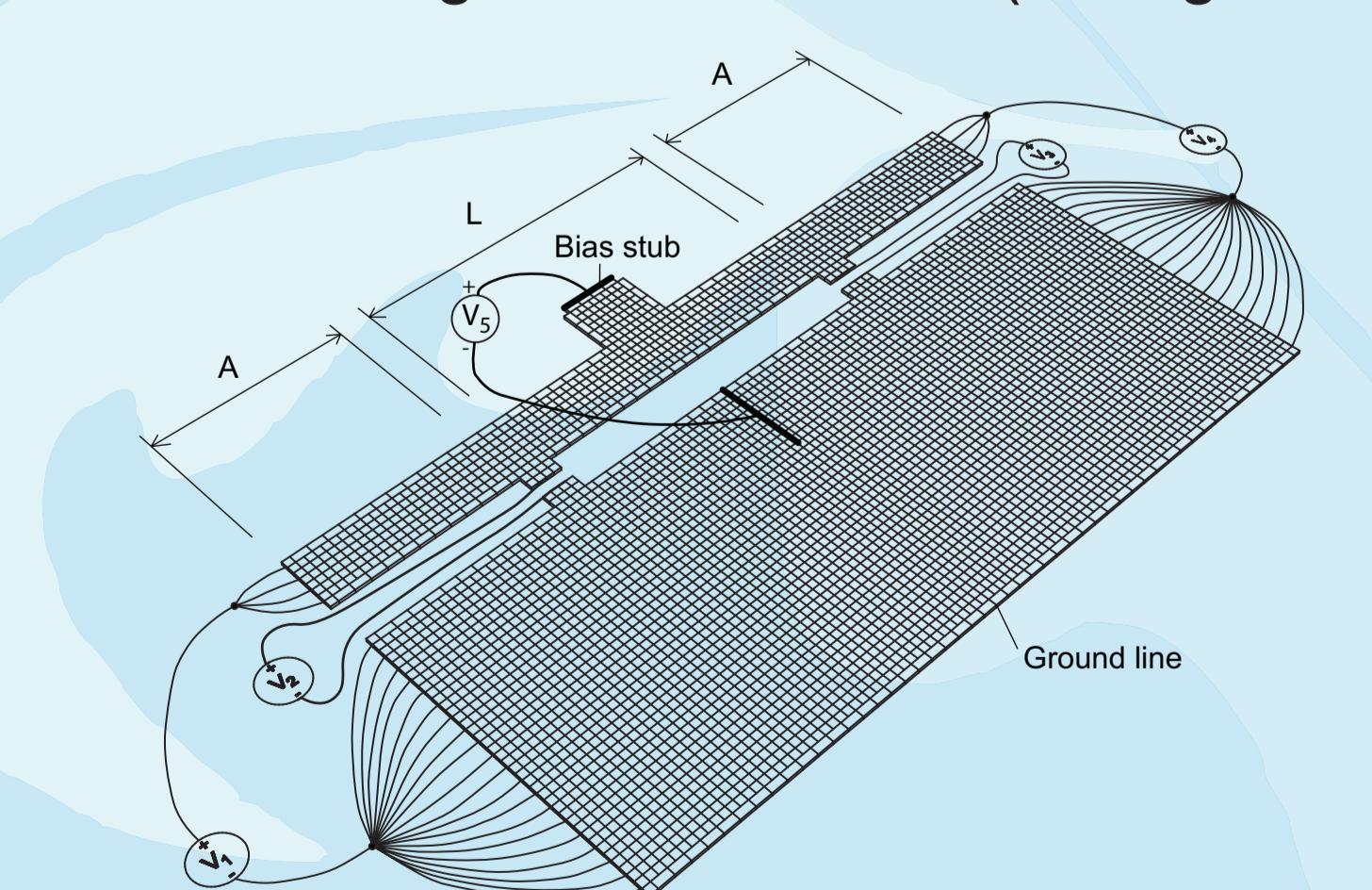


Fig. 9: Multi-port InductEx model of monolayer SQUID that is consistent with measurement results.

## Modeling an RSFQ circuit

A monolayer RSFQ circuit (DC-SFQ converter and JTL shown here) is modeled according to technique verified on SQUIDs. (YBCO layer named M1 here.)

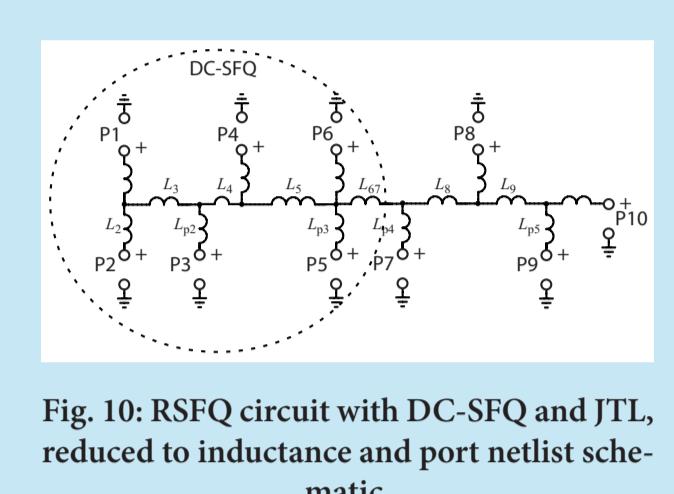
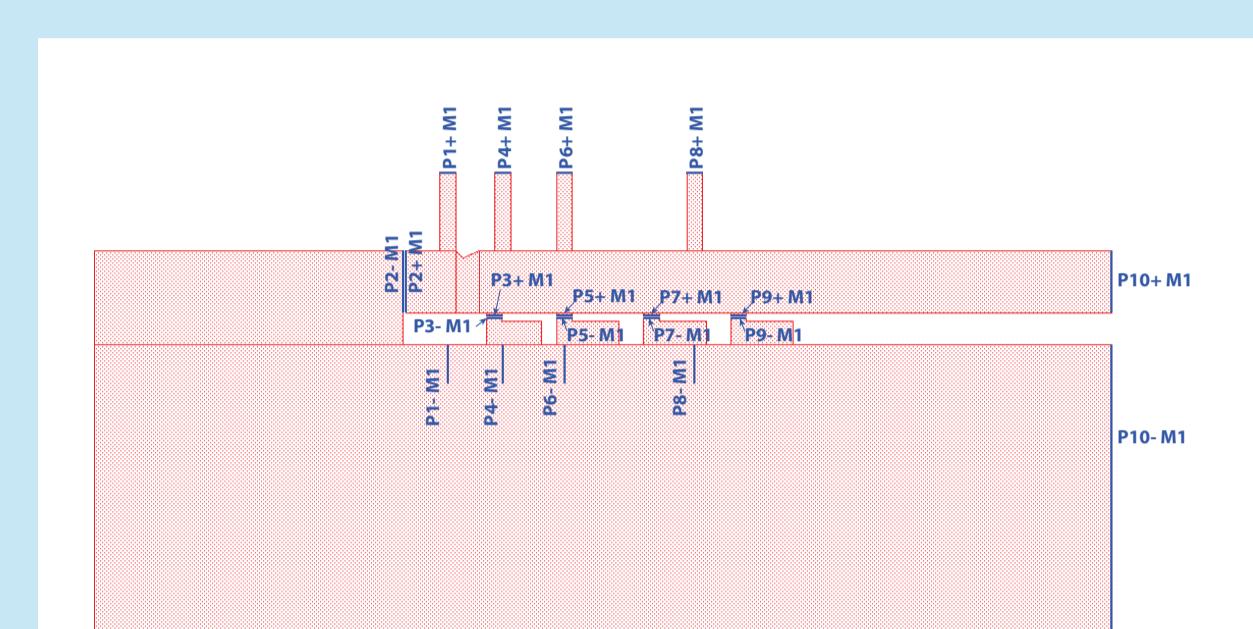


Fig. 10: RSFQ circuit with DC-SFQ and JTL, reduced to inductance and port netlist schematic.



InductEx results:  $L_2 = 4.6 \text{ pH}$ ,  $L_3 = 2.4 \text{ pH}$ ,  $L_4 = 0.50 \text{ pH}$ ,  $L_5 = 2.3 \text{ pH}$ ,  $L_{67} = 3.8 \text{ pH}$ ,  $L_8 = 1.5 \text{ pH}$ ,  $L_9 = 2.3 \text{ pH}$ ,  $L_{p(1,2,3,4)} \sim 2.6 \text{ pH}$ .

## Conclusion

We have verified numerical inductance extraction techniques for a monolayer RSFQ process with ion-irradiated junctions.

A multi-port inductance model was developed to handle RSFQ-type inductance netlists.

Calculations on first RSFQ circuits show that junction arm shape has significant effect on loop inductance (and should thus be designed carefully), and that junction arm inductance is high. Second-generation design will have to be optimized.

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