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Mutual inductances in superconductive integrated circuits

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Introduction

Inductive coupling in superconductive integrated circuits (ICs) becoming more important, especially with inductively biased circuits.

The effects coupling between bias inductors and circuit components need to be established to ensure that circuit operating margins do not deteriorate due to layout.

We analyzed the coupling between a control line and a SQUID loop for several structures manufactured with the FLUXONICS foundry at IPHT. This included coplanar lines over a ground plane.

We also analyzed mutual inductance for a YBCO ion-irradiated nanocircuits in a monolayer process [1], and conclude that coupling problems (and performance degradation) will be much more severe for circuits in such processes.

Previous work

We have already demonstrated that mutual inductance for complex layouts, such as an SFQ pulse transfer cell with isolated ground planes and ground plane holes (Fig. 1, FLUXONICS foundry [2]) can be modeled with InductEx (Fig. 2) and extracted (with calibration [3]). The difference between measurements and calculations were < 3 % for self and mutual inductances.

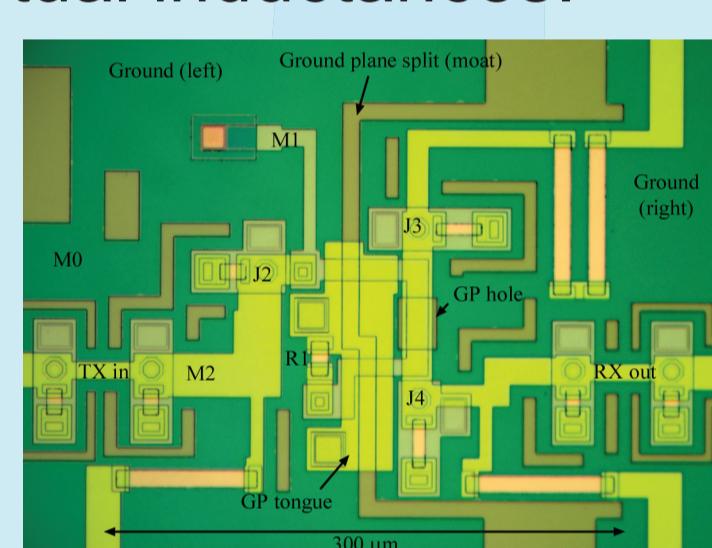


Fig. 1: Microphotograph of SFQ pulse transfer circuit [2].

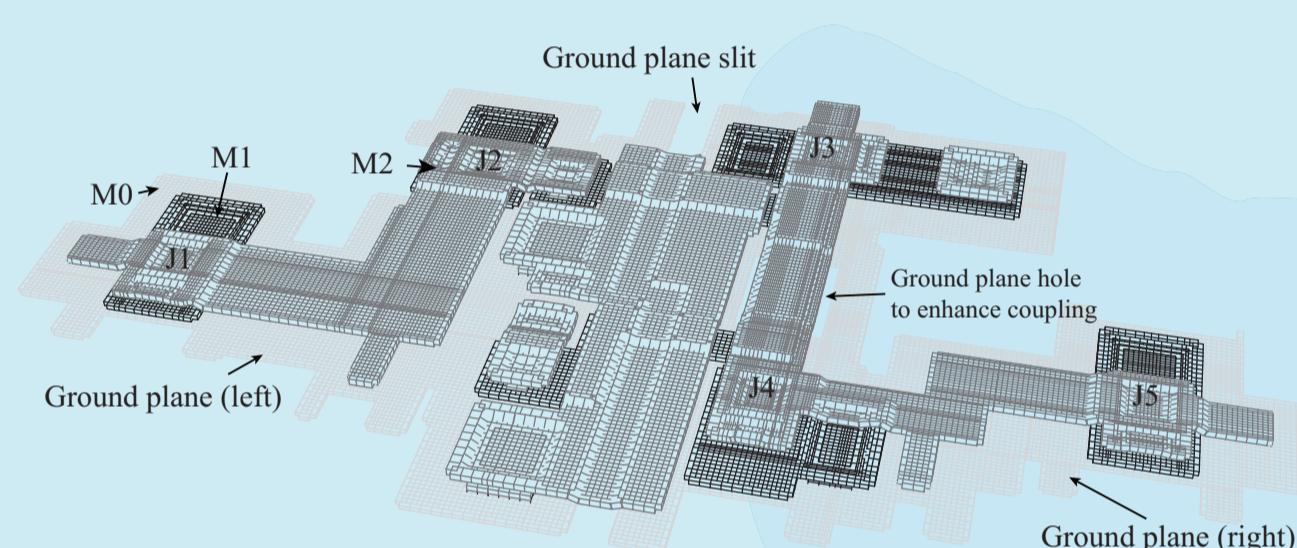


Fig. 2: Inductance calculation model of SFQ pulse transfer circuit in Fig. 1.

Monolayer inductance

For a monolayer high- T_c process (70 nm YBCO with ion-irradiated junctions, we established the validity of a modeling technique through the comparison of calculations with SQUID modulation measurements [1].

SQUIDs with coupling lines (Fig. 5) are modeled with a partial-element equivalent circuits (PEEC) technique [4] (no ground return path provided) as shown Fig. 2.

As seen in Table II, the absence of a ground plane leads to strong coupling even when lines are separated by large distances.

Table II: Calculated mutual inductance for monolayer coplanar lines in YBCO high- T_c process. The loop inductor and co-planar coupling lines have width = 10 μm , thickness = 70 nm and penetration depth = 185 nm. The SQUID loop inductance is 38 pH.

Gap s [μm]	Calculations	
	M [pH]	k
2.5	19.8	0.43
5	17.7	0.38
10	14.8	0.32
20	11.2	0.24

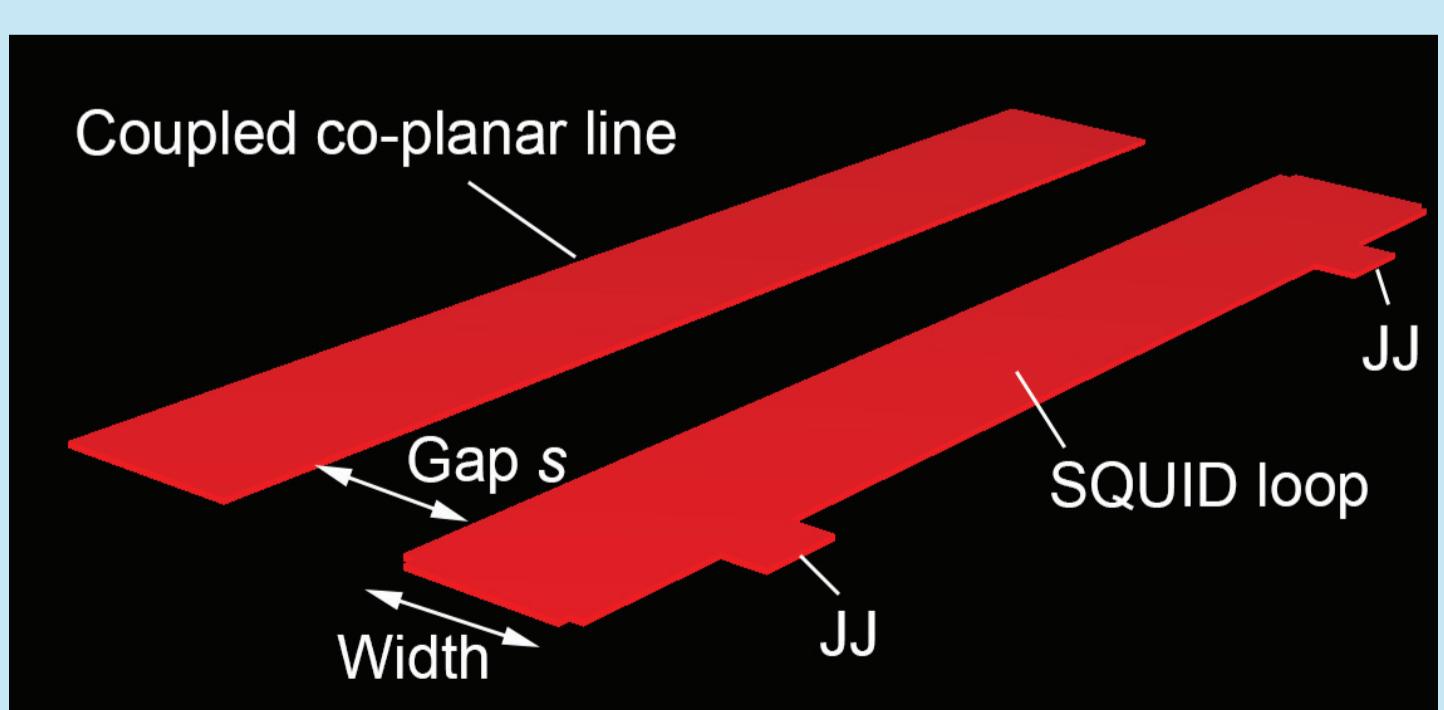


Fig. 5: Monolayer SQUIDs (with ion-irradiated junctions) and coupled co-planar line. A PEEC inductance modeling method is used with InductEx.

Stray coupling in a monolayer RSFQ circuit

For possible high- T_c monolayer RSFQ circuits [1], we investigated the coupling between bias non-perpendicular bias lines and circuit elements. As an example, consider the SFQ circuit in Fig. 6, which comprises a DCSFQ and JTL.

We used a 10-port network as shown in the schematic to model the circuit for extraction

The bias line inductance L_1 couples very strongly (k close to unity) with L_2 and L_3 (the values vary as the current injection and extraction points for port 1 are moved, so that exact values cannot be given without more experiments). Coupling factor to L_4 is ~ 0.25 , to L_5 it is ~ 0.1 , and for the rest it is negligible.

The result shows that coupling in such circuits requires careful attention.

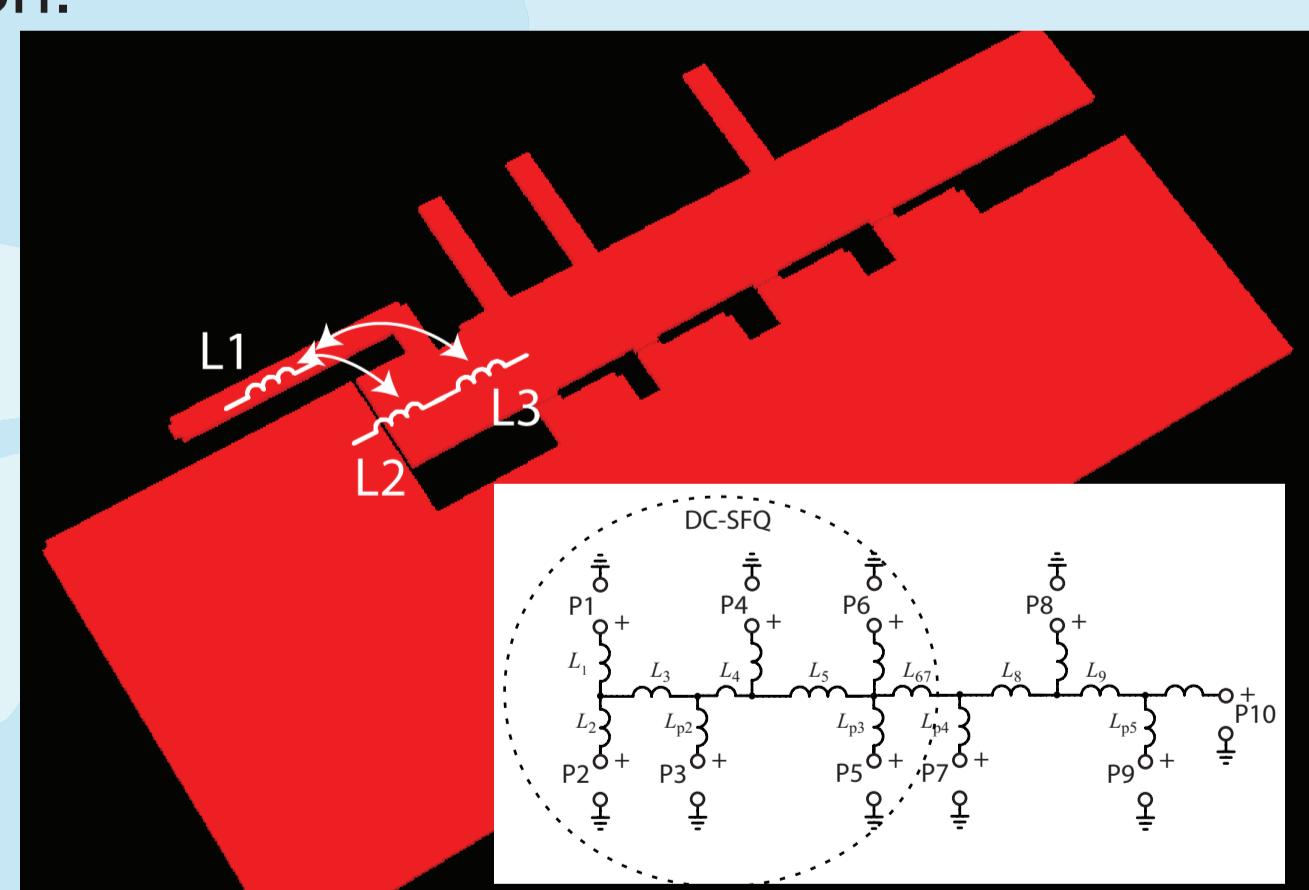


Fig. 6: Monolayer high- T_c RSFQ circuit schematic (inset) and extraction model showing physical locations of L_1 , L_2 , and L_3 and the coupling (arrows) between L_1 and L_2 , as well as L_1 and L_3 .

InductEx Homepage:
www.sun.ac.za/inductex

Conclusion

Mutual inductance in circuit layouts, even with ground plane holes or no ground planes, can be calculated. Results compare very well with measurements.

Mutual inductance (including stray coupling) in monolayer circuits with no ground plane is significant. This necessitates careful design and layout, and might render many monolayer layouts non-functional.

Acknowledgment

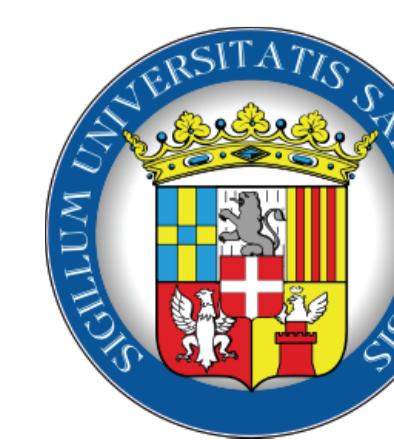
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References

- [1] T. Wolf, N. Bergal, J. Lesueur, C. J. Fourie, G. Faini, C. Ulysse and P. Febvre, "YBCO Josephson junctions and striplines for RSFQ circuits made by ion irradiation," *IEEE Trans. Appl. Supercond.*, vol. 23, 1101205, 2013.
- [2] C. J. Fourie, O. Wetzelstein, J. Kunert and H.-G. Meyer, "SFQ circuits with ground plane hole-assisted inductive coupling designed with InductEx," *IEEE Trans. Appl. Supercond.*, vol. 23, 130705, 2013.
- [3] C. J. Fourie, "Calibration of inductance calculations to measurement data for superconductive integrated circuit processes," *IEEE Trans. Appl. Supercond.*, vol. 23, 1301305, 2013.
- [4] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Dev.*, vol. 16, pp. 470-481, 1972.



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