YBCO Josephson Junctions and Striplines for RSFQ Circuits Made by Ion Irradiation

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Thomas Wolf, Nicolas Bergeal, Jérôme Lesueur, Coenrad J. Fourie, *Member, IEEE* , Giancarlo Faini, Christian Ulysse and Pascal Febvre, *Member, IEEE*

***Abstract*—We have investigated the electrodynamic properties of High-Tc Josephson junctions and strip-lines made by ion irradiation in order to evaluate the potential of such a technology for low power RSFQ superconductor digital electronics. The process is briefly presented together with the Josephson junctions characteristics in the context of high speed electronics. Line inductances of different geometries and at different temperatures have been measured through SQUID modulation. A detailed comparison with 3D numerical calculations has been made, and a quantitative agreement has been obtained that shows typical values of 4 to 8 pH per square without a ground plane, depending on line width and the gap to the ground line.**

***Index Terms*—High temperature superconductors, ion irradiation junctions, numerical inductance calculation, strip-line inductance.**

I. Introduction

SUPERCONDUCTOR digital electronics and especially the Rapid Single Flux Quantum (RSFQ) logic family remain of great research interest due to its exciting properties. RSFQ is fast, has extremely low energy consumption and its viability has been proven through the successful development of complex low-Tc electronics (for a review see [1, 2]). For many years it has been argued that refrigeration restrictions can be eased with the use of high-Tc superconductors, and some circuits have been demonstrated with success [3]. Design strategies and constraints have also been presented [4, 5]. Most reported processes use bicrystal grain boundary or ramp-edge junctions [6] (often with multiple layers [5]), but circuits with focused ion beam junctions in mono-layer processes have also been demonstrated [7].

Self-shunted junctions in high-Tc processes decrease layout complexity, but two important criteria restrict circuit layout in monolayer technologies: the ability to pattern Josephson junctions anywhere on a die, and tight control over inductance. Furthermore, large junction parameter variations over a wafer or successive wafers easily inhibit circuit operation. Moreover, thermal noise and the associated bit-error rate limit the operating margins of all high-Tc circuits, while the complicated lattice structure and short coherence length of high-Tc materials such as $YBa_2Cu_3O_7$ have hitherto prevented the establishment of reliable fabrication processes [8].

However, the advantages of speed and reduced cooling requirements in niche applications [9] as well as inductive biasing for low power RSFQ circuits [10] justify continued development of high-Tc RSFQ processes. Recently, there has been interest in ion-irradiated Josephson junction technology [11-13], which allows the implementation of complex structures suitable for high speed electronics [14]. In this paper we investigate and report on such an all-planar ion-irradiation process. With the absence of a dedicated ground plane, inductance for high-Tc striplines used in RSFQ circuits is difficult to estimate, and we present measurements of the inductance of superconducting lines in this process through SQUID modulation. We then investigate three techniques – one analytical and two numerical – to model the inductance of the SQUIDs fabricated with our process, and compare the results to the measured data. Finally we draw conclusions on the suitability of the process and inductance calculation methods for high-Tc RSFQ circuits.

II. Fabrication

Starting from a commercial 70 nm thick $YBa_2Cu_3O_7$ (YBCO) film (T_c = 86 K) grown on sapphire covered by an in-situ 100 nm gold layer, a three step fabrication is performed. Firstly, contact pads are defined in the gold layer through optical photoresist patterning followed by a 500 eV Ar^+ Ion Beam Etching (IBE). Secondly, contact lines and SQUID loops are patterned in an AZ5214 image-reversal photoresist followed by 110 keV oxygen ion irradiation. A dose of 5×10^{15} ions/cm^2 ensures that the surrounding matrix is deeply insulating. Next, Josephson junctions are fabricated. For the junctions, 20 nm slits in a 600 nm thick poly

Manuscript received September 13, 2012. This work was supported in part by the Région Ile-de-France within the framework of C'Nano IdF, by the Délégation Générale de l'Armement (DGA) through a doctoral grant by the PEPS-ST21 NANANA (Projet Exploratoire Pluridisciplinaire) of the French Centre National de la Recherche Scientifique (CNRS), and by the South African National Research Foundation, grant numbers 69006 and 78789.

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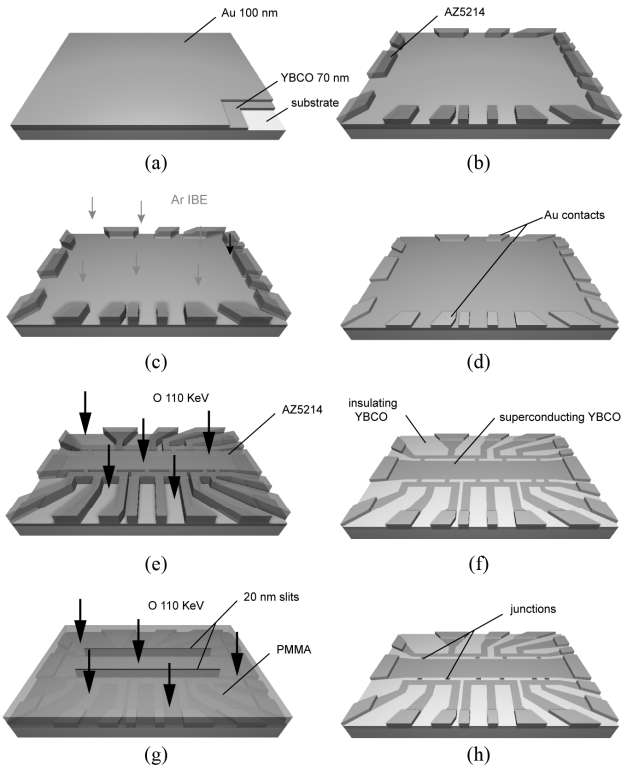

Fig. 1. Graphical illustration of the fabrication process steps: (a) 70 nm thick $YBa_2Cu_3O_7$ (YBCO) film grown on sapphire covered by an in-situ 100 nm gold layer, (b) pads defined in a AZ5214 negative photoresist, (c) 500 eV Ar Ion Beam Etching (IBE), (d) gold contacts after photoresist lift-off, (e) high dose 110 keV oxygen ion irradiation to create insulating regions in exposed YBCO, (f) patterned superconducting and insulating YBCO regions, (g) low dose 110 keV oxygen ion irradiation of Josephson junctions patterned as 20 nm wide slits in PMMA photoresist and (h) finished die.

(methylmethacrylate) (PMMA) photoresist are patterned using a LEICA EBPG 5000+ electronic beam-writer and irradiated with 110 keV oxygen ions. The process is illustrated in Fig. 1. We use a dose of 3×10^{13} ions/cm^2, which yields Josephson junctions that are suitable for operation in the temperature range 40 to 65 K, and 6×10^{13} ions/cm^2 for operation at 4.2 K. Different geometries for the SQUID loop inductors have been studied: width w of 4 μm with a 2 μm gap to the ground line, and w = 10 μm with a 5 μm gap to the ground line. For both line widths, five different lengths l were studied: 10, 20, 30, 50 and 80 μm. Fig. 2 shows the microphotograph of a sample with five different SQUIDs (width of 10 μm and lengths from 10 to 80 μm) sharing a common ground electrode, together with current injection lines.

Measurements were conducted in an Oxford Variable Temperature Insert using a four probe method for SQUID modulation and inductance measurement [15]. After measurement of the critical current as a function of temperature T, a SQUID is biased at its optimal point ($1.1 \times I_c$) while the control current is swept. This results in oscillations in the SQUID voltage (Fig. 3) with a current periodicity that can be related to the inductance of the superconducting line through the formula

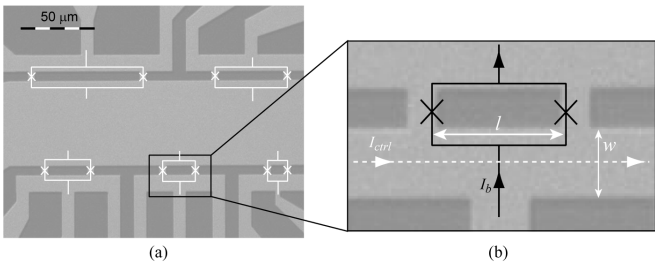

Fig. 2. (a) Microphotograph of a sample before the fabrication of the junctions. Five SQUIDs sharing a common ground electrode are seen, with length l ranging from 10 to 80 μm. The control arm has a width w. (b) Close-up of the l = 20 μm SQUID. A schematic overlay of the measurement geometry showing the bias current I_b and the control current I_{ctrl} is displayed. The junctions are symbolized by crosses. The full geometry in (b) is modeled for numerical calculations with 3D-MLSI and InductEx.

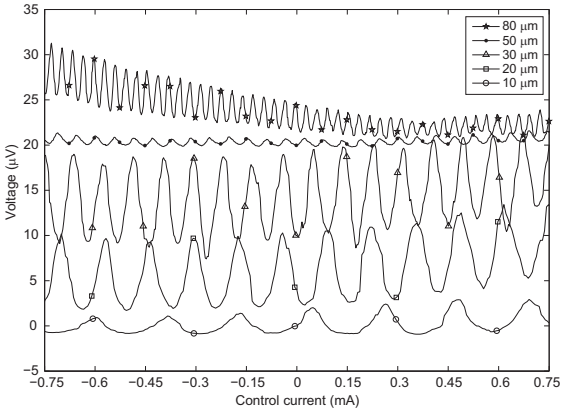

Fig. 3. Voltage modulation (shifted for clarity) for 10 μm-wide SQUIDs as a function of the control current I_{ctrl} measured at 4.2 K. From top to bottom, SQUID lengths are respectively: 80, 50, 30, 20 and 10 μm.

$$\delta I_{ctrl} = \Phi_0 / L \,, \tag{1}$$

where δI_{ctrl} is the change in control current required to sweep out one period of the SQUID voltage, $\Phi_0 = \dfrac{h}{2e} \cong 2 \times 10^{-15}$ Wb is the magnetic flux quantum and L the inductance of the superconducting line [16–19].

III. Junction Characteristics

Ion Irradiated Josephson Junctions (II-JJ) are non-hysteretic Superconductor-Normal-Superconductor (SNS) junctions. The disordered part made within the superconducting channel has a lower transition temperature T_C' than the rest of the channel (T_C), and acts as a normal metal. Between temperatures T_C and T_C', the channel is resistive (see top inset in Fig. 4), and the Josephson coupling occurs below T_C' [11]. The I-V characteristics displays a critical current (I_C) with no hysteresis (bottom inset in Fig. 4) and follows a Resistively Shunted Junction (RSJ) behavior [13]. The temperature dependence of I_C is quadratic, as expected for a proximity effect coupled JJ [11, 13]. Due to the fabrication process which uses advanced e-beam lithography and ion irradiation, these characteristics are fairly well reproducible (see Table 1

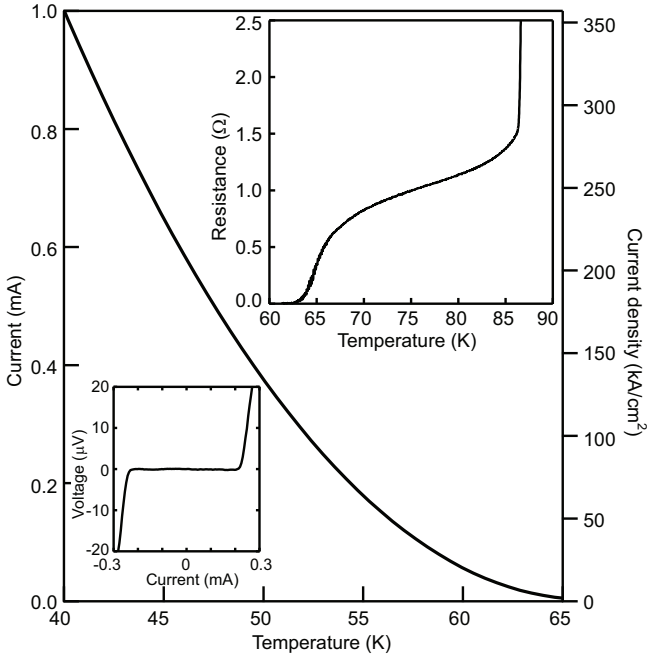

Fig. 4. Measured critical current (left axis) and current density (right axis) temperature dependence of an Ion Irradiated Josephson Junction (II-JJ). Top inset: Resistance as a function of temperature for the II-JJ. The higher transition is that of the electrodes. The lower transition corresponds to the II-JJ itself. Bottom inset: I-V characteristics of the II-JJ at $T \approx 50$K.

for measured junction characteristics). Moreover, these ion irradiation Josephson junction circuits do not suffer from the same layout constrains that grain boundary or step edge high-Tc Josephson junctions place on complex circuit designs. The ion irradiation process is also easily scalable, and therefore appears to be a good candidate for high-Tc based cryo-electronics.

IV. Inductance Calculation Models

We developed analytical and numerical inductance calculation models for the process described here to allow the extraction and verification of circuit layouts that do not adhere to simple straight-line geometries. The full range of manufactured SQUIDs was used to adjust model parameters and verify results.

A. Analytical approach

The analytical method is based on the Telegraphist's equation with the quasi-static assumption valid for the range of frequencies involved in the study. Effective dimensions are used to take into account edge effects. The topology of the normal metal coplanar structure is taken into account through geometrical parameters derived from [20, 21]. The superconducting behavior is considered through the insertion in the expressions of the geometrical parameters of the kinetic inductance connected to the superconductor London penetration depth λ. A detailed description of the formalism can be found in [22].

B. Numerical techniques

For numerical calculations we used both 3D-MLSI [23] and

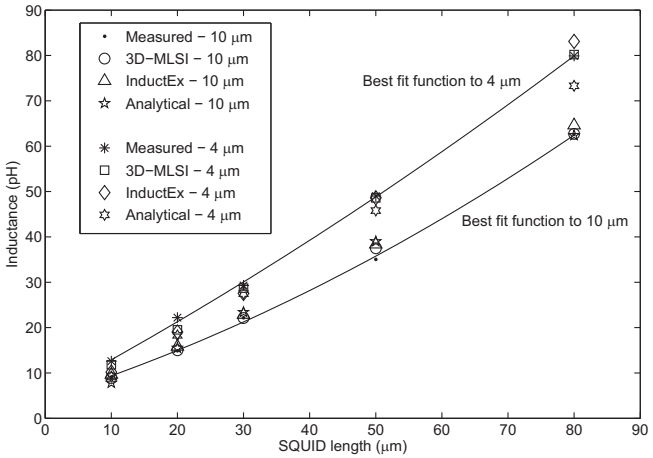

Fig. 5. Measured and calculated inductance versus SQUID loop inductor length for both 10 μm and 4 μm wide loop inductors. Best fit functions (quadratic) to the measured results are plotted, as well as analytical and numerical results with $\lambda(0) = 185$ nm.

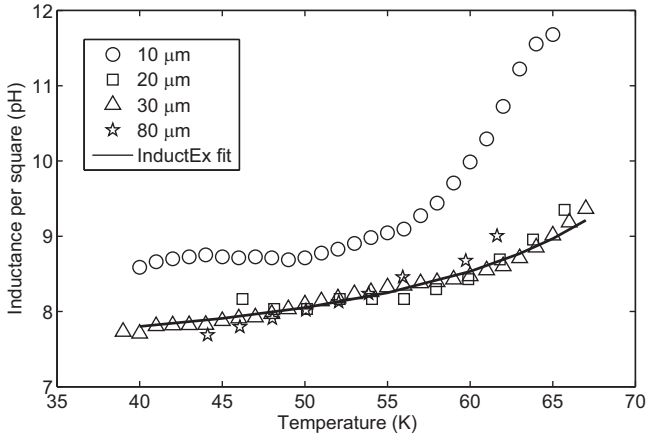

Fig. 6. Inductance as a function of temperature, with a fit line calculated with InductEx when $\lambda(0) = 185$ nm, $\alpha = 2.3$ and $T_C = 84$ K in equation (2).

InductEx [24] (verified over ground plane holes [25]) with FastHenry [26] as the field solver. Due to the distance between the SQUID loop inductors and ground conductors in the physical circuits, we modeled the SQUID loops as partial inductances [27] between the two junctions for both numerical techniques (excluding the current return path through the ground conductor). Only the YBCO layer was included in the models, while the gold layer was omitted.

V. Inductance Measurements

SQUIDs with highly irradiated junctions were measured at 4.2 K to determine the zero temperature London penetration depth $\lambda(0)$. The control current was swept from -0.75 mA to 0.75 mA, as shown in Fig. 3, and the period was obtained from the Fourier transform of the SQUID voltage data. The inductances thus measured are displayed along with calculation results in Fig. 5 as a function of the SQUID loop inductor length. We adjusted the London penetration depth for inductance calculations to minimize the difference from the best fit function on the measured data, and thereby determined $\lambda(0)$ as 185 nm (the manufacturer, THEVA, specifies a

penetration depth of 135 nm). The analytical and numerical techniques agree very well, which provides confidence in the modeling techniques.

A second set of SQUIDs with the same geometries as before, but fabricated with a different irradiation dose, was operated in the temperature range of interest for high-temperature circuits, 40-65 K, which allowed us to extract the temperature dependence of the London penetration depth. The injection current was swept up to 10 mA to give the precision needed to measure the slight variation in inductance with temperature. Fig. 6 shows the results together with a best fit from InductEx for the temperature dependence of the inductance controlled by the penetration depth. For the InductEx calculations we used the Gorter-Casimir two fluid model [17, 19]

$$\lambda(T) = \lambda(0)\frac{1}{\sqrt{1-\left(\frac{T}{T_C}\right)^{\alpha}}} \quad (2)$$

with an exponent α = 2.3, T_C = 84 K and $\lambda(0)$ = 185 nm (equal to that determined from the 4 K inductance measurements). Both α and $\lambda(0)$ agree well with values reported by other groups [17, 19, 20].

The per-square inductance of the shortest line (10 μm) in Fig. 6 is higher than that of the longer lines; due mostly to the exaggerated effects of current distribution near the junctions and manufacturing tolerances. An empirical effective length correction factor of 8/9 (determined from all the measurements and the numerical inductance calculations) equalizes the per-square inductance of the shortest (10 μm) lines in our experiments to that of the longer lines.

VI. Conclusion

The measured spreads of junction critical current over a chip, as shown in Table 1, is good at lower operating temperatures (± 20 %), and widens at higher temperatures. This is promising, considering that it is the first attempt at manufacturing, and with refinements to the process we confidently expect the I_C spreads to narrow.

The overall measurement of the mono-layer strip-line inductances gives us a value of 8 pH per square for a 10 μm wide line with 5 μm gap to the ground conductor, and 4 pH per square for a 4 μm wide line with 2 μm gap to the ground conductor. These values do not change significantly when the strip-line is changed to a coplanar wave guide geometry. Although the per-square inductances are higher than that of low-Tc circuits, the flexibility in junction placement ensures that practical ion-irradiated high-Tc RSFQ circuits can be laid out. The nano-patterning technique used here enables the miniaturization of circuit dimensions during the junction fabrication process, which can allow shorter circuit lengths with respect to stripline widths without the drawback of parasitics caused by external resistive shunts. Moreover, a factor of three inductance decrease is expected when a ground plane is added [19]. That could be realized by adapting the ion irradiation process to trilayer films [13, 28].

TABLE I
Measured Josephson junction characteristics against temperature

SQUID structure	Critical current (mA)				
	40 K	45 K	50 K	55 K	60 K
10 μm	1.19	0.81	0.47	0.23	0.074
20 μm	1.03	0.67	0.39	0.18	0.060
30 μm	0.99	0.65	0.38	0.17	0.058
50 μm	0.81	0.52	0.28	0.14	0.040
80 μm	1.03	0.70	0.42	0.21	0.083

RSFQ logic requires inductance values L such that

$$I_C L \approx \Phi_0 \approx 2.07 \text{ mA·pH}, \quad (3)$$

which is in the range 20 pH down to 13 pH for operation from 40 K to 65 K [5], while I_C ranges from 100 μA to 1 mA. Junctions fabricated with the irradiated junction technology described here fall in the same range, while per-square inductance of the mono-layer strip-lines is low enough to yield practical layout dimensions. The ion irradiation process described here can therefore be used to fabricate basic RSFQ circuits.

Despite several successful demonstrations of RSFQ electronics in high-Tc processes, it still has not found application in more complex systems. Junction placement, parameter variations and inductance layout appear to be the major limiting factors. With easier junction placement through ion irradiation, and reliable inductance calculation techniques developed, proven and reported here, complex high-Tc RSFQ circuits may yet become viable if critical current spreads can be controlled.

Acknowledgment

The authors would like to thank Y. Legall at INESS Strasbourg for the ion irradiation, and M. Khapaev at Moscow State University for assistance with 3D-MLSI.

References

[1] A. Silver, A. Kleinsasser, G. Kerber, Q. Herr, M. Dorojevets, P. Bunyk and L. Abelson, "Development of superconductor electronics technology for high-end computing," *Supercond. Sci. Technol.*, vol. 16, pp. 1368-1347, 2003.

[2] A. Fujimaki, M. Tanaka, T. Yamada, Y. Yamanashi, H. Park and N. Yoshikawa, "Bit-serial Single Flux Quantum microprocessor CORE," *IEICE Trans. Electron.,* vol. E91-C, pp. 342-349, 2008.

[3] S. Shokhor, B. Nadgorny, M. Gurvitch, V. Semenov, Y. Polyakov, K. Likharev, S. Y.Hou and J. M. Phillips, "All-high-Tc superconductor rapid-single-flux-quantum circuit operating at ~30 K," *Appl. Phys. Lett.*, vol. 67, pp. 2869-2871, 1995.

[4] H. Toepfer and H. F. Uhlmann, "Inductances in rapid single flux quantum circuits with high-Tc superconductors: a comparative study," *Physica C*, vol. 326-327, pp. 53-62, 1999.

[5] H. Toepfer, T. Ortlepp, H. F. Uhlmann, D. Cassel and M. Siegel, "Design of HTS RSFQ circuits," *Physica C*, vol. 392-396, pp. 1420-1425, 2003.

[6] D. Cassel, T. Ortlepp, K. S. Ilin, G. Pickartz, B. Kuhlmann, R. Dittmann, H. Toepfer, A. M. Klushin, M. Siegel and F. H. Uhlmann, "HTS

multilayer technology for optimal bit-error rate RSFQ cells," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 409-412, June 2003.
[7] K. Saitoh, T. Utagawa and Y Enomoto, "Temperature dependence of a high-Tc single-flux-quantum logic gate up to 50 K," *Appl. Phys. Lett.*, vol. 72, no. 21, pp. 2754-2756, May 1998.
[8] S. Anders *et al.*, "European roadmap on superconductive electronics – status and perspectives," *Physica C*, vo. 470, pp. 2079-2126, 2010.
[9] M. H. Volkmann, C. J. Fourie, W. J. Perold, D. B. Davidson, D. I. L. De Villiers and H. C. Reader, "Superconducting circuits in the Square Kilometre Array radio telescope," presented at the 2011 EUCAS-ISEC-ICMC, The Hague, The Netherlands.
[10] O. A. Mukhanov, "Energy-efficient single flux quantum technology," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 760-769, June 2011.
[11] N. Bergeal, X. Grison, J. Lesueur, G. Faini, M. Aprili and J. P. Contour, "High-quality planar high-T-c Josephson junctions," *Appl. Phys. Lett.*, vol. 87, p. 102502, 2005.
[12] N. Bergeal, J. Lesueur, G. Faini, M. Aprili and J. P. Contour, "High T-c superconducting quantum interference devices made by ion irradiation," *Appl. Phys. Lett.*, vol. 89, p. 112515, 2006.
[13] N. Bergeal, J. Lesueur, M. Sirena, G. Faini, M. Aprili, J. P. Contour and B. Leridon, "Using ion irradiation to make High-Tc Josephson junction," *J. Appl. Phys.*, vol. 102, p. 083903, 2007.
[14] S. A. Cybart, S. M. Anton, S. M. Wu, J. Clarke and R. Dynes, "Very large scale integration of nanopatterned YBa2Cu3O7-delta Josephson junctions in a two-dimensional array," *Nano Lett.*, vol. 9, pp. 3581-3585, 2009.
[15] W. H. Henkels, "Accurate measurement of small inductances or penetration depths in superconductors," *Appl. Phys. Lett.*, vol. 32, pp. 829-831, 1978.
[16] H. Hasegawa, Y. Tarutani, T. Fukazawa, U. Kabasawa and K. Takagi, "YBa2Cu3O7 step-edge dc SQUID with coplanar control lines," *Appl. Phys. Lett.*, vol. 67, pp. 3177-3179, 1995.
[17] E. Il'ichev, L. Dörrer, F. Schmidl, V. Zakosarenko, P. Seidel and G. Hildebrandt, "Current resolution, noise, and inductance measurements on high-Tc dc SQUID galvanometers," *Appl. Phys. Lett.*, vol. 68, pp. 708-710, 1996.
[18] H. Fuke, K. Saitoh, T. Utagawa and Y. Enomoto, "Estimation of inductance for high-Tc dc-SQUIDs in coplanar waveguide," *Jpn. J Appl. Phys.*, vol. 35, p. L1582-L1584, 1996.
[19] H. Terai, M. Hidaka, T. Satoh and S Tahara, "Direct-injection high-Tc dc-SQUID with an upper YBa2Cu3O7-x ground plane," *Appl. Phys. Lett.*, vol. 70, pp. 2690-2692, 1997.
[20] K. C. Gupta, R. Garg and I. J. Bahl, *Microstrip lines and slotlines*, Artech House, 1979, ch. 7.
[21] J. F. Whitaker, R. Sobolewski, D. R. Dykaar, T. Y. Hsiang and G. A. Mourou, "Propagation model for ultrafast signals on superconducting dispersive striplines," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 277-285, 1988.
[22] P. Febvre, C. Boutez, S. George and G. Beaudin, "Models of superconducting microstrip and coplanar elements for submillimeter applications," in *Proc. Int. Conf. on Millimeter and Submillimeter Waves and Applications II*, San Diego, 1995, pp. 136-147.
[23] M. M. Khapaev, M. Y. Kupriyanov, E. Goldobin and M. Siegel, "Current distribution simulation for superconducting multi-layered structures," *Supercond. Sci. Technol.*, vol. 16, pp. 24-27, 2003.
[24] C. J. Fourie, O. Wetzstein, T. Ortlepp and J. Kunert, "Three-dimensional multi-terminal superconductive integrated circuit inductance extraction," *Supercond. Sci. Technol.*, vol. 24, 125015, Nov. 2011.
[25] C. J. Fourie, O. Wetzstein, J. Kunert, H. Toepfer and H.-G. Meyer, "Experimentally verified inductance extraction and parameter study for superconductive integrated circuit wires crossing ground plane holes," *Supercond. Sci. Technol.*, vol. 26, 015016, Jan. 2013.
[26] M. Volkmann and C. J. Fourie (2012). FastHenry Version 3.0wr+su. Stellenbosch University. Available: http://www.sun.ac.za/inductex..
[27] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Dev.*, vol. 16, pp. 470-481, 1972.
[28] N. Bergeal, J. Lesueur, M. Aprili, G. Faini, J. P. Contour and B. Leridon, "Pairing fluctuations in the pseudogap state of copper-oxide superconductors probed by the Josephson effect," *Nat. Phys.*, vol. 4, no. 8, pp: 608-611, Jan. 2008.