Power Consumption Reduction in Integrated Pacemakers: Design Strategies for Cortex-M0+ Processors

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Abstract— **For medical implantable devices such as pacemakers, minimizing power consumption is crucial to ensure long-lasting and reliable operation. In this context, this paper explores the design of integrated Cortex-M0+-based processors integrated into pacemakers with a focus on reducing power consumption. Indeed, the processor is the part of the pacemaker that consumes most of the battery energy due to its various operation modes. Key factors influencing its static and dynamic power consumption, including the choice of the right CMOS technology, are analysed and discussed. An approach to reduce the power consumption of the Cortex-M0+ processor is investigated involving an adjustment of the transistor geometric parameters of the standard cell libraries. Considering the TSMC65 65 nm technology, a notable 17.2 % reduction in the total power consumption of the Cortex-M0+ has been obtained while maintaining a maximum operating frequency of 100 MHz, thus highlighting a promising advancement in enhancing the energy efficiency of pacemaker systems.**

Keywords— Digital design, Cortex-M0+, implantable pacemaker, TSMC65, standard cell library.

I. INTRODUCTION

Implantable pacemaker devices play a critical role in the treatment of various cardiac rhythm disorders, ensuring the heart beats at a regular and appropriate rate [1]. Pacemakers are also designed to provide long-term cardiac rhythm management, with a battery life ranging from several years to over a decade depending on the device type and usage [1]. This long-term autonomy is crucial to ensure consistent and uninterrupted therapy for patients. Hence, energy consumption is a critical aspect during the pacemaker design, as it directly impacts the battery life [2]. The pacemaker's processor is the part that consumes most of the battery energy since it must analyse in real time, the heart activity [3]. Hence, a direct way to minimise the energy consumption of a pacemaker is to consider low-power processors during the design.

Integrated CMOS (Complementary Metal-Oxide-Semiconductor) technology can help to reduce the power consumption of digital circuits such as processors. Moreover, due to its high integration density, more functionalities can be integrated into a single chip, reducing the need for additional components. Thus, an optimal fabrication process technology can be selected to minimise the power consumption during the different working phases of a pacemaker processor, while keeping the circuit area low.

Integrated ARM-based processors for pacemaker design can be considered an appropriate choice due to its low power consumption [4]. Indeed, ARM Cortex-M0+-based processors have been specifically designed for low energy consumption applications and offer sufficient processing capabilities for handling the tasks required by a pacemaker, such as monitoring heart rhythms and delivering appropriate pacing pulses.

A previous study was conducted to compare the power consumption of the Cortex-M0+ core for three different technologies offered by STMicroelectronics: 130 nm, 65 nm and 28 nm nodes [3]. The CMOS 65 nm was selected as the best candidate due to its best compromise between power consumption and cost-effectiveness. The proposed study extends the analysis to the TSMC 65 nm technology (TSMC65) to further reduce power consumption and cost.

Additionally, important complementary investigations on the transistor's sizing are also conducted here with the objectives to reduce the power consumption while maintaining high enough the operating frequency of the processor. Notably, literature shows that combining transistor resizing with supply voltage reduction effectively achieves energy efficiency in CMOS technology [5].

Indeed, elementary parts of a digital circuit are logic gates. Most of technologies provide foundry libraries with logic gates which are called standard cells [6]. Each logic gate of a standard cell library is standardized in terms of layout size and timing (e.g. propagation delay) in order to be easily interconnected with the others standard cells of the library.

Moreover, to minimize–circuit area, a minimal channel length is generally chosen during the standard cell design stage. Indeed, for a fixed width, the smaller the channel length is, the higher the integration density and the faster the switching frequency are [7] but it can lead to a non-optimal leakage power consumption.

In this context and beyond the evaluation of the TSMC65 technology, the proposed study also assesses the static (leakage) and dynamic power consumption versus the channel length and width. Additionally, effects due to the change of the transistors size on the maximum operating frequency and on the overall power consumption of the processor are studied for a given scenario.

The main contributions of this paper are:

- Cortex-M0+ processor power consumption benchmark in the TSMC65 technology;
- Power consumption optimization analysis - This stage involves resizing transistor of standard cells to determine the optimal length (L) and width (W) to achieve a notable reduction in power consumption.

This paper is organized as follows. Section II introduces some background terminologies related to implantable pacemaker power consumption. Section III focuses on the benchmark of the Cortex-M0+ processor for different technologies including the TSMC65 one. Section IV deals with the impact of the channel length on the processor power consumption and its maximum switching frequency. The same work is done for the width in Section V. Next, Section VI discusses the results. Finally, section VII concludes the paper.

II. BACKGROUND

A. Implantable pacemaker power consumption

Implantable pacemakers have revolutionized the treatment of cardiac bradycardia (i.e., slow heart rhythm) by providing reliable and efficient means of regulating heart rhythm [8]. Leadless implantable pacemakers, surgically [9] implanted within the patient's heart, consist of several components. The CAIRDAC's pacemaker [10] illustrated in Fig. 1 comprises three main components: the therapy ASIC, the power management unit (PMU) ASIC and the CPU. The therapy ASIC is responsible for generating electrical impulses that regulate heartbeat through two electrodes. The PMU ASIC's role is to recover energy from the piezoelectrical system and efficiently manage its transfer to the battery. Finally, the CPU is a microcontroller housing the processor responsible for managing control and computational tasks.

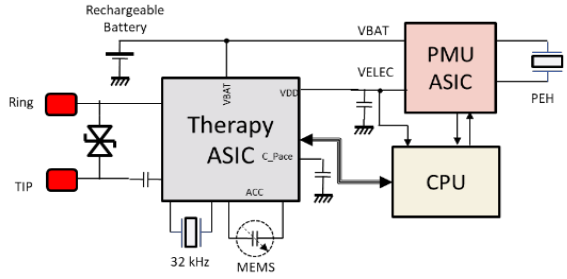

Fig. 1. CAIRDAC's implantable pacemaker architecture

One important aspect of the pacemaker design is related to the power consumption management. This is particularly important as pacemakers need to operate continuously for long period of time since it is implanted surgically [9]. A simplified current consumption scenario of a pacemaker is illustrated in Fig. 2. Current consumption, which is directly proportional to the power consumption, is provided for a pacemaker leveraging on the STM32 microcontroller family [10].

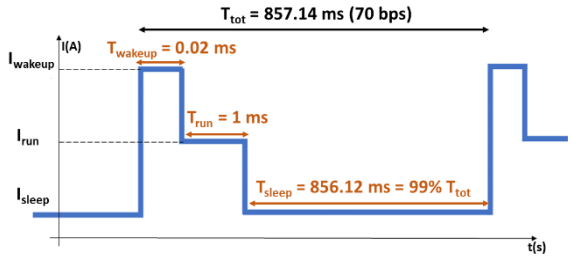

Fig. 2. CAIRDAC's pacemaker current consumption scenario

In this scenario, the total period T_{tot} is equal to 857.14 ms (= 60 s/ 70 bpm) if it is considered that the pacemaker is set to pace the heart at 70 beats per minute. T_{tot} includes:

- T_{run} with a duration of 1 ms, where the therapy algorithm is executed, consuming I_{run} (around 100 µA);
- T_{sleep} with a duration of 856.12 ms, where the device remains in sleep mode, consuming I_{sleep} current (around 380 nA), which constitutes 99 % of the pacemaker's operational time;
- T_{wakeup} with a duration of 0.02 ms, where the device is in a transition state between the sleep and the run phase where the consumed current is maximum (around 1 mA; wake-up on interrupt).

Based on Fig. 2, the average power consumption of the pacemaker can be written as follows:

$$P_{tot} = \frac{E_{idle} + E_{wakeup} + E_{run}}{T_{tot}} \quad (1)$$

where E_{idle} represents the energy consumed in mode sleep calculated in (2), E_{wakeup} represents the energy consumed when the CPU wakes up, obtained by (4), and E_{run} represents the energy consumed during the run mode calculated in (3).

$$E_{idle} = T_{sleep}\, P_{dc} \quad (2)$$

$$E_{run} = T_{run}\, (P_{dc} + P_{ac}) \quad (3)$$

$$E_{wakeup} = T_{wakeup}\, (P_{dc} + P_{ac} + P'_{ac}) \quad (4)$$

where P_{dc} (= $I_{sleep} \cdot V_{dd}$ with V_{dd} = 1.2 V the supply voltage) represents the static power consumption due mainly to the leakage current, P_{ac} (= [I_{run} - I_{sleep}] · V_{dd}) the dynamic power consumption during the running period, and P'$_{ac}$ (= [I_{wakeup} - I_{run}] · V_{dd}) the additional dynamic power consumption during the wake-up period.

Based on the current consumptions presented in Fig. 2 and the equations (1), (2) (3) and (4), the power consumption of the CAIRDAC's pacemaker is calculated and summarized in Table I. Therefore, to effectively reduce the overall power consumption of the pacemaker we should focus on several key factors specifically: P_{dc} by minimizing the leakage currents of the design, P_{ac}, by improving the efficiency of dynamic operations and optimizing the algorithm, and P'_{ac} through optimizing the wake-up mechanism and reducing T_{wakeup}. However, P'_{ac} optimisation will not be considered according to its low impact on the overall consumption. Moreover, if T_{run} is considered fixed for a specific use case and a given clock frequency, reducing the total power consumption of CAIRDAC's pacemaker mainly requires a reduction in P_{dc}.

TABLE I. CAIRDAC'S PACEMAKER POWER CONSUMPTION

P_{dc} (nW)	P_{ac} (µW)	P'_{ac} (mW)	E_{idle} (nJ)	E_{run} (nJ)	E_{wakeup} (nJ)	P_{tot} (nW)
456	120	1.2	390	120	24	623.5

B. CMOS leakage currents: Origins and implications

CMOS leakage currents, which refer to the flow of electrical current through the transistor even when it is in the off-state [11], have various origins. They are related to various physical mechanisms as illustrated in Fig. 3.

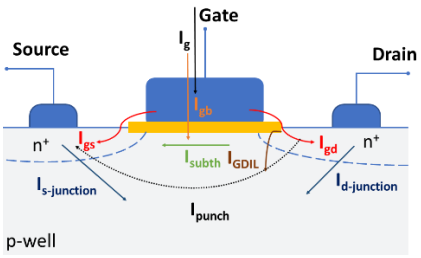

Fig. 3. CMOS transistors leakage currents

Thus, the total leakage current is the sum of several leakage currents such as sub-threshold (I_{subth}), gate-induced drain leakage (I_{GIDL}), and depletion punch-through leakage (I_{punch}). There is also gate tunnelling leakage (I_g, including I_{gs},

I_{gd}, and I_{gb}) and p-n drain and source junction leakages ($I_{s/d\text{-}junction}$) [12]. While most of leakage currents are considered negligible, sub-threshold, gate and junction leakages are the three main key components for power analysis [13]. As CMOS technology scales down, the reduction in transistor length and width leads to a significant increase in sub-threshold leakage power [14]. Therefore, optimizing the geometric parameters of transistors can effectively mitigate the impact of CMOS leakage current and enhance overall power efficiency. This is particularly true in the context of pacemakers, where the sleep mode represents 99.9 % of the operational time.

III. CORTEX-M0+-BASED PACEMAKERS: TSMC65 TECHNOLOGY BENCHMARK

A. Standard cell libraries

For processor core design, the selection of a specific standard cell library is crucial for achieving the desired performance criteria. These libraries typically use specific flavours of MOS which targets different needs, such as the need of low leakage where is it possible to find the flavours low leakage (LL), ultra-low leakage (ULL), and high threshold voltage (HVT). Other libraries use flavours targeting performance in terms of speed such as high speed (HS), and low threshold voltage (LVT) and other libraries use flavours which are a compromise between speed and leakage such as regular threshold voltage (RVT).

Standard cell libraries are related to a specific technology. For instance, in HCMOS9A (130 nm), CMOS65 (65 nm) and FDSOI-28 (28 nm) technologies from STMicroelectronics, the standard cell libraries that allow are respectively ULL, HVT, and RVT [3]. Regarding the TSMC65, it employs HVT MOS flavour and especially the library *TCBN65LPBWP7THVT*.

B. Digital design methodology

Synopsys Design Vision has been used as the synthesis tool to synthesize the ARM Cortex-M0+ IP described in Verilog language [15]. The synthesis flow is illustrated in Fig. 4a. Fig. 4b illustrates the Cortex-M0+ core chip obtained after place and route steps using the INNOVUS tool.

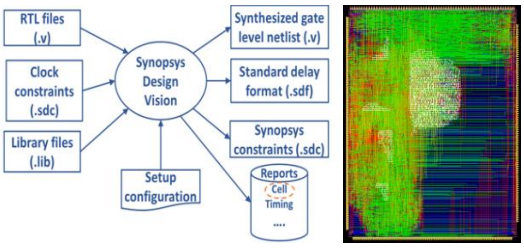

Fig. 4. (a) Digital design flow (b) post-synthesis view in HCMOS9A

The synthesis of the Cortex-M0+ was initially performed using the HCMOS9A technology, resulting in a design including 8876 logic cells, distributed as illustrated in Fig. 5.

To fairly compare the different manufacturing technologies, the logic gates with similar or approximate fan-out characteristics have been considered to estimate the power consumption of the processor core. Thus, for each technology, the average leakage power and the dynamic power have been firstly evaluated at the gate level (main gates indicated on Fig. 5). Then, results have been extrapolated at the Cortex-M0+ level. Following this methodology, all possible input logic combinations were considered for each standard cell, and the worst-case scenario has been retained.

The total static power consumption P_{dc} of a processor core has been computed using equation (5):

$$P_{dc} = \sum_{cell} P_{dc/cell} \tag{5}$$

with:

$$P_{dc/cell} = N_{cell} \frac{(I_{max0} + I_{max1})}{2} V_{dd} \tag{6}$$

where $P_{dc/cell}$ represents the power dissipation of every instance of one cell type, N_{cell} is the number of instance of cells, I_{max0} is the maximum leakage current consumed for a '0' output, I_{max1} is the maximum leakage current consumed for a '1' output.

The active power consumption of a cell P_{ac} has been determined using the same philosophy but by analysing the average current consumption for two distinct input frequencies (here 10 MHz and 100 MHz), frequencies which are applied to one or more cell inputs depending on the worst-case scenario. Then, the result is scaled to the targeted processor frequency (here 1 MHz).

These steps were repeated for each logic gate of the standard library of the targeted technology, with nominal V_{dd} values at 37°C. Finally, the overall consumption of the Cortex-M0+ has been obtained by summing the consumption of all the logic gates, as indicated in equation (5).

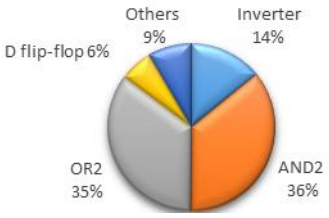

Fig. 5. Cortex-M0+ cell distribution

C. Results

Table II, presents the results obtained for the TSMC65 technology and provides a comparison with technologies from STMicroelectronics. These results are dependent on the specific standard cell library used.

TABLE II. CORTEX M0+ TSMC65 TECHNOLOGY BENCHMARK

T = 37°C		P_{dc} (nW)	P_{ac} (µW) @ 1MHz	Area (µm²)	Price (€/mm²) [16][17]
ST	**HCMOS9A** 130 nm (1.2 V)	*391*	*400*	*197 000*	*2,500*
	CMOS065 65 nm (1 V)	*210*	*54*	*40 000*	*4,500*
	FDSOI-28 28 nm (1.1 V)	*266*	*9.35*	*9 340*	*9,000*
TSMC	**TSMC65** 65 nm (1.1V)	*393*	*44.8*	*50 000*	*4,462*

Based on Table II, the static power dissipation of TSMC65 is 393 nW, which is higher than CMOS65 (210 nW). However, TSMC65 has a dynamic power consumption of 44.8 µW, which is slightly lower than CMOS65 (54 µW). The chip area for TSMC65 is 50 000 µm², which is larger than CMOS65 (40 000 µm²). Thus, the difference in area is not significant, and the larger area obtained with TSMC65 is acceptable for the pacemaker requirements. Moreover, the price for TSMC65 is 4,462 €/mm², which is comparable to

CMOS65 at 4,500 €/mm^2. In conclusion, TSMC65 technology is not the best technology at the first sight but stays a valid candidate for the Cortex-M0+-based pacemakers since its P_{ac} is the lower one (excluding the costly FD-SOI technology), RAM and ROM compilers can be obtained (which is fundamental for a processor and avoid the design of a System in Package - SiP) and a significant reduction of P_{dc} can be obtained as it will be seen in the following sections. Thus, a deep analysis of the TSMC65 is now conducted to further improve its overall power consumption.

IV. Impact of the Channel Length on the Cortex-M0+ Design with TSMC65

Standard cell libraries provided by foundries are generally not customizable. However, this study draws inspirations from the TSMC65 standard cells, promoting the redesign of a new library with optimized length and width sizes. This section focuses on varying the channel length (L) of the transistors in the overall design of the Cortex-M0+. First, an analysis of the cell GINVD8, an inverter gate with a fan-out of 8 from the TSMC65 digital library, is provided. The cell is simulated under the following conditions: V_{dd} = 1.2 V and T = 27° C with a nominal channel length (L) of 60 nm. Then, L is incremented with a 5 nm step up to 110 nm while maintaining a constant width-to-length ratio (W/L). Fig. 6 illustrates the impact of L variation on both static and dynamic power for the GINVD8 cell.

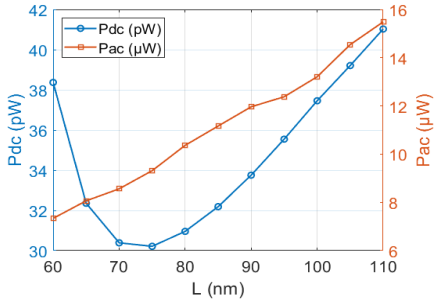

Fig. 6. Static and dynamic power versus L for the GINVD8 cell

For L = 60 nm, which is the minimal length supported by the TSMC65 technology, the static dissipation (P_{dc}) of 38.37 pW and the dynamic dissipation (P_{ac}) of 7.34 µW can be observed. As L increases, P_{dc} decreases up to L = 75 nm, where it reaches 30.21 pW. In contrast, the dynamic energy P_{ac} increase monotonically with L. Beyond L = 75 nm, both P_{ac} and P_{dc} increase. Fig. 7 shows that P_{dc} is due to the leakage current through the off-state transistor I_{leak}, which is mainly composed of I_{subth} and the gate leakages. The expression used to calculate P_{dc} is given in (7) [18].

$$P_{dc} = I_{leak}.V_{dd} \quad (7)$$

The P_{dc} evolution versus L, presented in Fig. 6, can be attributed to two primary factors influencing the leakage currents. The first one operates predominantly for small L and reflects the subthreshold leakage current (I_{subth}) due to finite value of the drain-source resistance R_{ds}, while the second factor, which becomes more significant as L increases, reflects the gate tunnelling leakage current I_g. Indeed, for larger L, the leakage current I_g becomes predominant as I_g is related to the gate oxide resistance R_{ox}, along the z-axis (see Fig. 8). Both resistors can be estimated as follows:

$$R_{ox} = \rho_{ox}\frac{e_{ox}}{W.L} \quad (8) \qquad R_{DS} = \rho_{DS}\frac{L}{W.e_{DS}} \quad (9)$$

where e_{ox} (resp. e_{DS}) represents the gate oxide (resp. channel) thickness, ρ_{ox} (resp. ρ_{DS}) denotes the gate oxide (resp. drain-source) resistivity, and L and W stand for the gate length and width. Therefore, as L increases, R_{ox} decreases, leading to a rise in the gate leakage current and consequently an increase in P_{dc}. Conversely, for smaller L values, I_{subth} predominates because when L increases, R_{ds} increases, leading to a decrease in I_{subth} and consequently in P_{dc}.

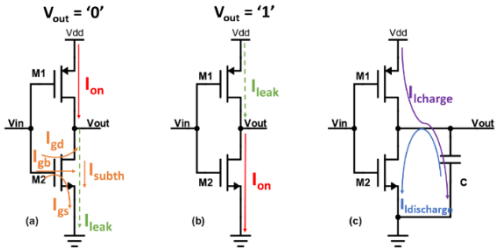

Fig. 7. (a) (b) GINVD8 Inverter cell static power dissipation and (c) dynamic power dissipation

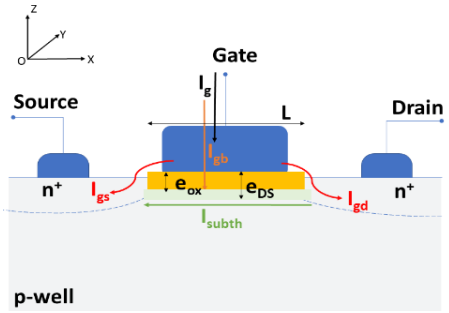

Fig. 8. CMOS geometric parameters and leakage currents

Concerning the behaviour of the dynamic power dissipation (P_{ac}) versus L, it occurs due to the charging and discharging of the output capacitance C during switching [18] as illustrated in Fig. 7. The equation of the dynamic power is given by equation (10) [18]:

$$P_{ac} = \alpha.C.V_{dd}^2.f_{sw} \quad (10)$$

where V_{dd} is the supply voltage, f_{sw} is the switching frequency and C represents the total capacitance seen at the output node of the inverter. Note that the capacitance C developed in (11) is composed of the output intrinsic capacitance (C_{out}), the input capacitance of the following logic gate which acts as load (C_L), proportional to the gate capacitances of logic gate MOS input transistors, and an extra parasitic capacitance (C_{ext}) which is due to the interconnection lines [19]. Note that C_{out} is proportional to the gate capacitance (C_{gs}) developed in (12). C_{gs} includes the nMOS gate capacitance (C_{gsn}) and the pMOS gate capacitance (C_{gp}) [19].

$$C = C_{out} + C_L + C_{ext} \quad (11)$$

$$C_{gs} = C_{gsn} + C_{gsp} = \alpha C_{OX}(W_pL_p + W_nL_n) \quad (12)$$

Except for the C_{ext} contribution (which can be estimated to 0.5 fF for the TSMC65 technology after post-layout simulations), C is also mainly proportional to L. Thus, for a

fixed switching frequency, P_{ac} is proportional to L if C_{ext} is not considered, as shown in Fig. 6.

However, it can be demonstrated that changing L has an impact on the propagation delay and also on the maximum switching frequency $f_{sw\text{-}max}$. Indeed, assuming a basic model of a MOS inverter based on a current source (inversely proportional to L) loaded by a capacitance (proportional to L), the propagation delay is also inversely proportional to L^2 and so the maximum switching frequency is proportional to L^2. Thus, moving from 60 nm to 75 nm (25 % increase of L) should lead to an increase of the propagation delay of 56 % and also a reduction of the maximum switching frequency of 56 % (for a fixed W).

Finally, all the simulations related to the inverter have been repeated for each logic gates of the Cortex-M0+ (presented in Fig. 5). From these simulations, the overall static power consumption of the Cortex-M0+, presented in Fig. 9, has been obtained. Compared with the inverter level simulations, the same trend has been observed (i.e., same evolution of P_{dc} and P_{ac}). However, the minimum P_{dc} occurs at a different L (65 nm) compared to the inverter (75 nm). This discrepancy arises from the specificity of all the simulated logic gates, each one having its own optimal L when the P_{dc} parameter is concerned. Finally, changing L from 60 to 65 nm will lead to an increase of the propagation delay of about 17 % and also a decrease of the maximum switching frequency $f_{sw\text{-}max}$ of about 17 % (this is not issue due to the native performance of the standard cells as discussed in VI).

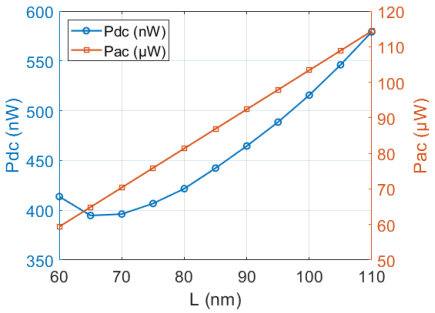

Fig. 9. P_{dc} and P_{ac} versus L for the overall Cortex-M0+ processor

TABLE III. IMPACT OF THE "L" VARIATION ON THE OVERALL CORTEX-M0+ DESIGN AT 27°C FOR THE TSMC65 TECHNOLOGY (1.2V)

L (nm)	P_{dc} (nW)	P_{ac} (µW) @ 1MHz	E_{idle} (nJ)	E_{run} (nJ)	P_{tot} (nW)
60	418	59.4	358	59.8	443
65	396 *-5.26 %*	64.9 *+9.26 %*	339 *-5.31 %*	65.2 *+9. 3%*	429 *-3.16 %*
70	400	70.4	342	70.8	438

Table III presents the values of the different Cortex-M0+ consumption parameters obtained for L = 60 nm, 65 nm, and 70 nm. E_{idle}, E_{run}, and P_{tot} are also computed at the Cortex-M0+ level. Thus, it can be seen from Table III, that an adjustment of the transistor length from 60 nm to 65 nm results in a 5.31 % reduction in the sleep mode power consumption and a 3.16 % reduction in total power consumption. This result suggests that the optimal length for improving the power efficiency is 65 nm.

V. IMPACT OF THE CHANNEL WIDTH ON THE CORTEX-M0+ DESIGN WITH TSMC65

To more enhance power consumption, an investigation on the transistor width (W) variation is done in this section. In this investigation, L has been fixed to 65 nm but the same methodology used for L is now used on W. Thus, an analysis of the GINVD8 inverter cell is firstly provided before extending the analysis to the Cortex-M0+ core.

For the inverter, its nominal NMOS width W_n is 2.04 µm, while the minimal W_n of the TSMC65 technology is 120 nm. To comprehensively explore the effects of the width variation, W_n is swept from 120 nm to 2.04 µm keeping the p-channel width W_p 1.5 times higher. Fig. 10 shows the impact of the W variation on static and dynamic power consumption of the GINVD8 cell. Decreasing W results in a reduction of both P_{ac} and P_{dc}. As already mentioned, P_{dc} occurs from the leakage current through the transistors, and reducing W leads to a reduction of P_{dc}. Regarding P_{ac}, decreasing W reduces the gate capacitance, which leads to a reduction in P_{ac}, as illustrated in Fig. 10.

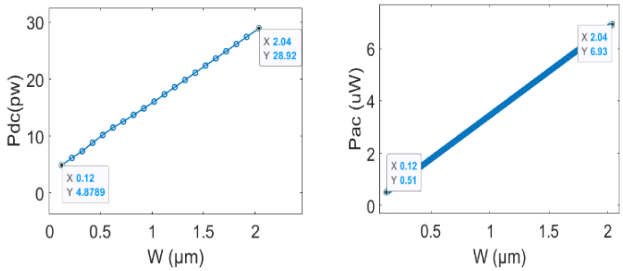

Fig. 10. P_{dc} and P_{ac} versus W for the GINVD8 inverter cell.

As predicted by equations from (7) to (10), moving from W_n = 2.04 µm to W_n = 120 nm results in a reduction of P_{dc} (83 %) and P_{ac} (92.5 %) since at the first order, P_{dc} and P_{ac} are linearly related to W.

Moreover, it can be demonstrated that changing W has no impact (on the first order) on the propagation delay and also on the maximum switching frequency $f_{sw\text{-}max}$. Indeed, assuming a basic model of a MOS inverter based on a current source (proportional to W) loaded by a capacitance (proportional to W), the propagation delay is W independent. Nevertheless, if a capacitance (C_{ext}) which represents the parasitic capacitive effect of the interconnection line between two logic cells is considered too, higher the parasitic capacitance is (compared to C_{OUT} + C_L), higher the propagation delay is and so lower the maximum switching frequency is. Fortunately, this effect for a switching frequency on the order of one MHz is neglectable for the parasitic capacitance of 0.5 fF which was obtained after post-layout simulations. Further transistor width reduction beyond 20 % is avoided as it can lead to greater variability in the transistor characteristics due to manufacturing process variations. Moreover, narrow transistors are more sensitive to threshold voltage variations due to random dopant fluctuations. These variations can cause inconsistencies in the switching behaviour, leading to potential timing errors in digital circuits.

Finally, P_{ac} and P_{dc} extractions have been repeated for each logic gates of the Cortex-M0+ (see Fig. 5). From these simulations, the overall power consumption of the cortex M0+ is presented in Table IV after a 20 % reduction of W. E_{idle}, E_{run}, and P_{tot} are also provided. The results show that a

20 % reduction of *W*, along with shifting *L* from 60 nm to 65 nm results in a 20 % reduction in P_{dc} and a 17.2 % reduction in the total power consumption.

TABLE IV. IMPACT OF THE "W" VARIATION ON THE OVERALL CORTEX-M0+ DESIGN AT 27°C FOR THE TSMC65 TECHNOLOGY (1.2V)

T = 27°C	**P_{dc} (nW)**	**P_{ac} (µW) @1MHz**	**E_{idle} (nJ)**	**E_{run} (nJ)**	**P_{tot} (nW)**
L = 60nm $W_{nominal}$	418	59.4	358	59.8	443
L = 65 nm W = -20 %	334 -20 %	56.25 -5.3 %	286 *-20 %*	56.5 -5.5 %	367 *-17.2 %*

VI. DISCUSSION

The Cortex-M0+ processor was synthesized using the TSMC65 technology for an initial frequency of 50 MHz (t_d =1/50M=20 ns). Post synthesis results provide a critical path slack time (t_s) of 11.67 ns. The critical path slack time being calculated as the difference between the total available time (t_d) and the time required for signals to traverse the critical path (t_s) [20]. Consequently, the minimum operational period is 8.33 ns and the maximal operation frequency is 120 MHz.

At the system level, during the pacemaker run time, the pacemaker's therapy algorithm needs approximately 1000 clock cycles. With faster system clock, current consumption in run mode I_{run} (see Fig. 2) will increase, while T_{run} decreases, keeping a constant product I_{run} and T_{run}. Consequently, changing the operational frequency up to 120 MHz will not affect P_{ac}. Nevertheless, reducing the operating frequency contributes to reducing the overall temperature of the chip. This help in maintaining a safe and low temperature which can significantly reduce the leakage currents, knowing that temperature has an exponential impact on leakage currents [3].

However, with a lower operating frequency, each instruction necessitates more time to be executed, potentially elongating the duration required for specific tasks. But, in the exploration of resizing transistors to reduce the global power consumption of about 17.2 % by adjusting both the width (-20 %) and the length (60 nm to 65 nm), the maximum switching frequency will be 17 % reduced (if C_{ext} is neglected). This leads to a maximum switching frequency of about 100 MHz which is not critical since this value sufficiently stays higher than the working frequency of 50 MHz defined at the beginning of the synthesis.

VII. CONCLUSION

The proposed study focuses on improving the power efficiency in Cortex-M0+-based processors for medical implantable devices including pacemakers. This work demonstrates a notable 17.2 % reduction in the total power consumption through the adjustment of transistor geometries *W* and *L* of the digital libraries used to synthetize the Cortex-M0+ processor. However, this is at the cost of a 20 % reduction of the maximum switching frequency (120 MHz to 100 MHz), which fortunately stays higher than the operating frequency used for synthesis (50 MHz). Even if addressing the challenge of designing new standard cells remains a time-consuming task, future researches will be dedicated to extending the study to the whole microcontroller. To make this possible, the Corstone-101 subsystem developed by ARM will be considered [21]. Indeed, it's a helpful tool that includes essential components to design a full microcontroller such as processor, interconnects, memories controllers and some peripherals. The Corstone-101 serves as a valuable tool to streamline our efforts, but additional components such as memories must be incorporated to ensure an effective microcontroller solution for pacemakers. Furthermore, addressing the variability of transistor characteristics and its impact on the processor performances will be a critical aspect of our future work.

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