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Unconventional Seedless Multilayers with Large Perpendicular Anisotropy for Back-End-of-Line Compatible Spintronic Devices

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An unconventional class of hard and out-of-plane magnetized seedless multilayers (SL-MLs) of the form [Co/insertion layer/Pt]$_n$, grown as a top reference layer in magnetic tunnel junctions (MTJ), was investigated. Among different nonferrous insertion layers (Ta, Cu, Mg, W, Ru, and Al), Ta produces the highest perpendicular magnetic anisotropy. A back-end-of-line (BEOL) compatible hard top reference layer using Ta-inserted SLMLs was achieved, exhibiting more than twice effective perpendicular anisotropy compared to a conventional top reference layer. Using this top reference layer, we developed three types of spintronic memory stacks: (a) top-pinned MTJ stacks that can withstand annealing up to 425 °C, (b) BEOL compatible double-MTJ memory cells with read/write mode control layer enabling a faster readout and low-voltage writing, and (c) 2-bit MTJ stacks combining spin-transfer torque and spin-orbit torque writing. The magnetic properties of these three types of memory stacks are discussed.

KEYWORDS: seedless multilayer, magnetic tunnel junction (MTJ), top-pinned MTJ, double MTJ, STT-MRAM, SOT-MRAM, multibit memory

INTRODUCTION

Conventional perpendicular spin-transfer torque magnetic random access memory (STT-MRAM) is based on out-ofplane magnetized bottom pinned MTJs.[1] Such MTJs comprise an MgO tunnel barrier sandwiched between a bottom synthetic antiferromagnetic (SyAF) reference layer of the form (Co/Pt)$_n$/Ru/(Co/Pt)$_m$/Ta/FeCoB and a top FeCoB-based free layer (FL).[2,3] In this configuration, high perpendicular magnetic anisotropy (PMA) is obtained in the reference layer since the (Co/Pt) multilayers are deposited on appropriate seed layers such as Pt, Pd, and Ru, yielding the strong face-centered cubic (fcc) (111) texture required for high PMA.[4] However, there is, nowadays, an increasing interest for emerging spintronic devices such as double-MTJ (DMTJ) STT-MRAM,[5,6] spin-orbit torque magnetic random access memory (SOT-MRAM),[7,8] and racetrack memory[9,10] primarily due to added advantages of increased STT-efficiency, improved reliability due to separate read and write current paths, and high storage density, respectively. These different spintronic device stacks require a seedless magnetically hard layer above the MgO tunnel barrier. This is quite difficult to achieve since the MgO barrier and the FeCoB magnetic electrode do not constitute a good seed layer to promote the required fcc (111) growth of a (Co/Pt) multilayer. In this paper, we demonstrate that a seedless top reference layer can be achieved by using multilayers, composed of repetitions of the form (Co/insertion layer/Pt). The insertion layer (I) can be made of a variety of non-ferrous metals, preferably Cu or Ta. Especially, the (Co/Ta/Pt)$_n$ seedless multilayers (SL-MLs) exhibit almost twice larger PMA than the conventional Co/Pt SL-MLs and are able to withstand BEOL annealing process temperatures. Using these novel SL-MLs as a top reference layer, BEOL compatible top-pinned MTJ stacks for SOTMRAM applications, double-MTJ cells for energy efficient STT-MRAM applications, as well as 2-bit MTJ stacks written by a combination of STT and SOT are demonstrated.

EXPERIMENTS, RESULTS, AND DISCUSSION

The samples were deposited on a Si wafer by magnetron sputtering under an Ar pressure of 2×10^{-3} mbar. The MgO tunnel barrier was prepared by naturally oxidizing a metallic Mg layer under an oxygen pressure of 3×10^{-2} mbar with a flow rate of 100 sccm. On top of this oxidized layer, a second Mg layer (5 Å thick) was deposited. All the samples were annealed for 10 min at different temperatures under high vacuum (5×10^{-6} mbar). The magnetization versus field hysteresis loops, M(H), were measured by vibrating sample magnetometry (VSM). Additionally, the effective perpendicular anisotropy (Keff) was calculated from the area between perpendicular and in-plane M(H) loops. The total thickness of Co, Pt, and Fe72Co8B20 layers are considered in the calculation of Keff and saturation magnetization (Ms).

Seedless Multilayers with Non-Ferrous Metal Laminations

Usually, the Pt layers used in the repeats of seedless Co/Pt multilayers are thicker than those used in seeded Co/Pt MLs[11] because a thicker Pt layer yields higher Keff as it improves the fcc (111) texture. However, because

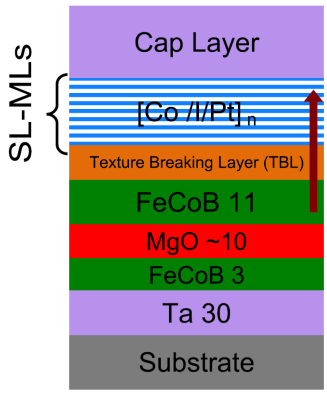

FIG. 1. Schematics of half-MTJs with seedless multilayers (SLMLs) on top. The FeCoB layer below the MgO layer is magnetically dead. Thicknesses are indicated in an angstrom (Å) unit.

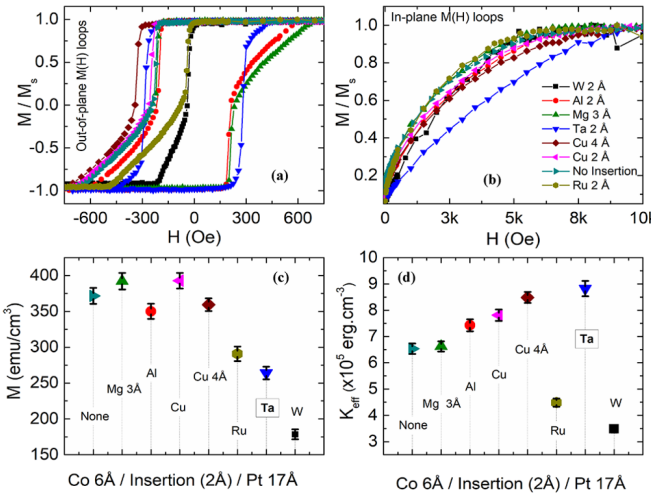

FIG. 2. (a) Out-of-plane and (b) in-plane magnetic cycles when the field is varied from positive to negative saturation; (c) Ms and (d) Keff of "Ta 30/FeCoB 3/MgO 10/FeCoB 11/W 6/[Co 6/I/Pt 17]$_5$/Ru 50 Å" MLs with different insertion (I) layers after annealing at 400 °C for 10 min. Keff and saturation magnetization (Ms) were calculated considering the total thickness of Co, Pt, and FeCoB layers.

Pt atoms are much heavier than Co atoms, depositing thicker Pt layers leads to significant Co-Pt intermixing at the Co/Pt interfaces, which reduces the Keff. These two competing effects of the Pt thickness results in a moderate value of Keff, lower than in seeded (Co/Pt) multilayers and generally too weak to be usable as a top hard layer in perpendicular magnetic tunnel junctions. To circumvent the intermixing issue while preserving Co (3d)-Pt (5d) hybridization to improve Keff, we investigated new SL-MLs formed by inserting various nonferrous metal laminations (I) between Co and Pt layers. The role of the laminations is to prevent or limit the penetration of the Pt atoms in the Co layer as they impinge on the Co surface and/or to reduce the demagnetizing energy thanks to the reduction in magnetization of the ferromagnetic layers due to intermixing. The schematic of these SL-MLs is depicted in Figure1.

Such SL-ML can be used as a reference layer above the MgO tunnel barrier of top-pinned MTJ stacks. The Co/I/ Pt MLs are ferromagnetically coupled to the FeCoB layer above the MgO barrier via a texture-breaking layer (TBL)1 typically made of Ta, W, or Mo. This TBL is intended to ensure a structural transition between the body-centered cubic (bcc) part of the stack next to the MgO barrier and the fcc top part of the stack. As an insertion layer "I", Cu, Ta, Mg, Al, W, and Ru were studied and compared with the reference MLs (Co/Pt MLs). Thicknesses of these insertion layers are tCu,Ta,Al,W,Ru = 2 Å, tMg = 3 Å, and tCu = 4 Å. The Keff values of Co/I/Pt MLs with Al, Cu, and Ta insertions are larger than those of the reference MLs without the insertion layer between Co and Pt, which is shown in Figure 2.

Since Cu has very low miscibility with Co, depositing a thin layer of Cu above Co prior to the deposition of the Pt layer helps to increase PMA by reducing the intermixing of Pt with Co. Bandiera et al. also observed this PMA enhancement for Co/Pt multilayers on Pt seed layers.[12] Due to immiscibility of Co with Cu as well as with Mg,[13,14] the saturation magnetization (Ms) values of these metal-laminated MLs are larger than in the reference MLs. On the other hand Ta, W, and Ru laminations result in lower magnetization, as they are miscible with Co.[14] It is noteworthy that the lower Ms of Ru-laminated MLs compared to reference MLs suggests possible intermixing of Co and Ru and formation of a metastable Co-Ru binary phase. However, the stabilization of this phase is unlikely, considering its positive formation enthalpy reported by Troparevsky et al.[14] Among the various metals investigated, Ta insertion produces the highest Keff and a nearly square out-of-plane M(H) loop after annealing at 400 °C as shown in Figure 2a-d. The saturation magnetization of Ta-inserted SL-MLs is significantly lower (Figure 2c) compared to the case of no insertion due to high miscibility of Ta with Co. Therefore, one possible origin of the enhancement of Keff for Ta-inserted SL-MLs is the reduced demagnetizing energy. Moreover, the in-plane magnetic cycle is almost linear as shown in Figure 2b compared to the other MLs. This suggests that there is a weaker contribution of second-order anisotropy. Such higher order anisotropy often emerges from spatial fluctuations of the first-order anisotropy over the Co/Pt interfaces associated with nanoscale roughness or intermixing.[15,16] Therefore, the Ta insertion layer most likely improves the interfacial smoothness. Interfacial smoothness is important to get the proper hybridization between Co and Pt orbitals, which contributes to the perpendicular anisotropy at (Pt/Co) interfaces.[17] To use this Ta-laminated SL-MLs as a top reference layer in

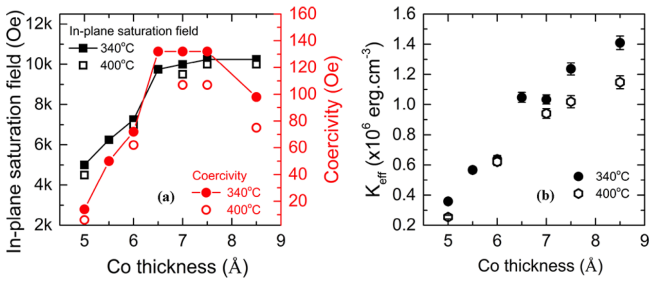

FIG. 3. (a) In-plane saturation field and out-of-plane coercivity and (b) Keff of SL-MLs (Ta 30/MgO 10/FeCoB 11/W 3.5/[Co (t)/Ta 2/Pt 11]$_5$/Ru 50 Å) as a function of Co thickness after annealing at 340 and 400 °C.

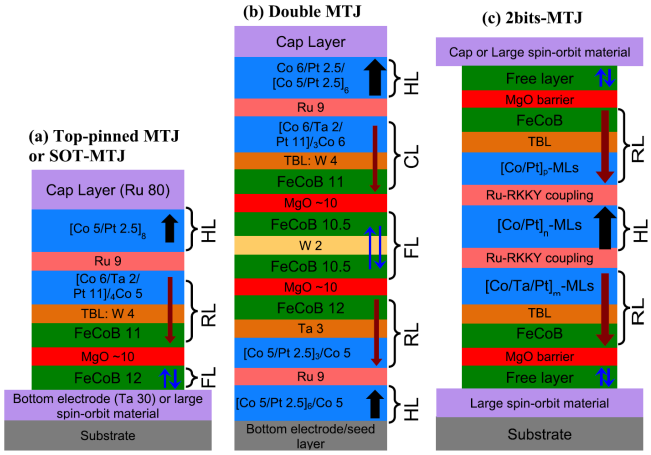

FIG. 4. Schematics of the (a) top-pinned p-MTJ, (b) double-MTJ, and (c) 2-bit MTJ stacks. The magnetization directions of the hard layer (HL), reference layer (RL), and free layer (FL) are, respectively, represented by the black, brown, and blue arrows. Similar color convention of arrows is used to explain magnetization reversals of different magnetic components of different stacks in their respective magnetic cycles depicted in Figures 5, 6, and 8. The top RL of the double-MTJ stack is called the control layer (CL). Thicknesses are in angstrom (Å).

an MTJ stack, we optimized the thicknesses of the different components of (Co/Ta/Pt) SL-MLs, namely, the W-TBL, Pt, Co, and Ta thicknesses to maximize Keff. The detailed optimization is discussed in the Supporting Information attached to this publication. The optimal thickness of WTBL, Ta, and Pt layers are, respectively, 3.5-4, 2, and 11 Å. The magnetic properties of SL-MLs with Co thickness variation using the optimum thickness of Ta-insertion (2 Å), W-TBL (3.5 Å), and the Pt layer (11 Å) is shown in Figure 3.

Figure 3a shows that the coercivity and in-plane saturation field strongly increase with Co thickness and saturate above 6.5 Å. Keff increases with increasing Co thickness up to the maximum thickness (8.5 Å) used in this study, as shown in Figure 3b. After annealing at 400 °C, a small reduction of Keff as well as of saturation field and coercivity is observed. Nevertheless, the value of Keff remains almost twice larger than in the reference- MLs shown in Figure 2d. Therefore, Ta-laminated SL-MLs are promising devices.

Top-Pinned MTJ, Double-MTJ, and 2-Bit Memory Stacks Using the SL-MLs

Figure 4 shows the schematics of three different stacks for spintronic memory devices implementing the above-described SL-MLs: (a) top-pinned MTJ stack for STT-MRAM or SOT-MRAM applications, (b) double-MTJ stack with a read/write mode control layer for STT-MRAM applications, enabling a fast readout and low-voltage writing, and (c) 2-bit memory stack, which can be written by a combination of STT and SOT. The magnetic properties of these three types of stacks are discussed below:

Top-Pinned MTJ

Hysteresis loops of the top-pinned stack, schematically shown in Figure 4a, are presented in Figure 5a. Only the descending branch of the major M(H) loops is plotted for clarity, because the ascending branch just repeats the same magnetization reversal steps as the descending branch. The magnetization reversal steps of the hard layer (HL), reference layer (RL), and the storage layer or free layer (FL) as a function of an applied field are indicated, respectively, by the black, brown, and blue arrows consistently with the schematic diagram of Figure 4a. The vertical magnetization reversal steps of the RL and HL of the stack including the minor hysteresis loops of the RL (see inset of Figure 5a) after annealing at 425 °C temperature proves magnetic stability of the stack after 425 °C annealing, which is quite remarkable. The 1.2 nm FeCoB FL deposited on Ta suffers from PMA loss due to elemental inter-diffusion upon annealing at 400 °C and exhibits a slanted magnetization reversal. However, this can be avoided by wisely engineering the FL. As an evidence, we show the M(H) plot of another similar top-pinned stack for which the FL was replaced by a composite type of FL (MgO/FeCoB/W/FeCoB/MgO). This top-pinned stack with a composite FL exhibits similar reversal steps as the previous one with sharper magnetization reversal of the FL, which is clearly shown by the red minor loop in Figure 5b.

Double MTJ

. A double-MTJ stack has two reference layers sandwiching the storage layer, as represented in Figure 4b. In

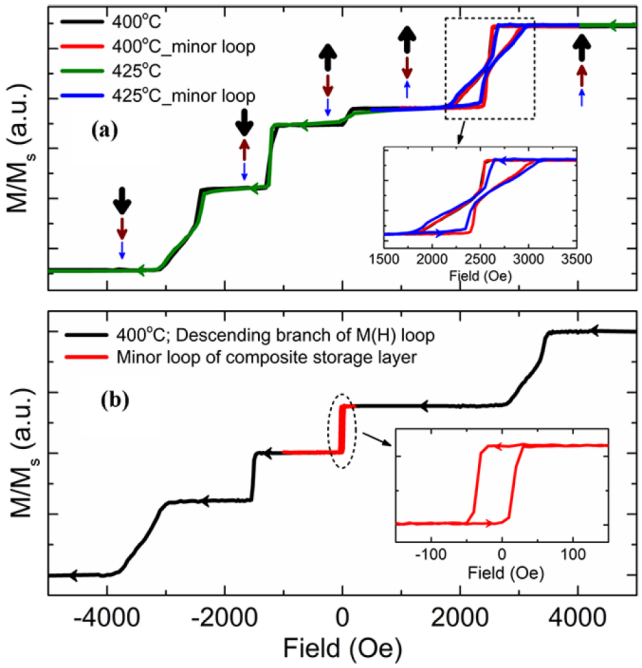

FIG. 5. (a) Descending branch of the out-of-plane M(H) loop of the top-pinned MTJ stack described in Figure 4a. The RL shows annealing stability up to 425 °C, revealed by the blue and red minor loops. The annealing stability of the FL is improved by choosing a composite free layer as shown by the red minor loop of (b). Similar to (a), the graph in panel (b) exhibits a descending branch of the out-ofplane magnetic cycle of the top-pinned stack with a layer configuration of "Ta 30/FeCoB 3/MgO 10/FeCoB 10/W 2/ FeCoB 10/MgO/W 4/[Co 6/Ta 2/Pt 11]$_3$/Co 6/Ru/Co 6/Pt 2.5/ [Co 5/Pt 2.5]6/Ru 50/Pt 20 Å".

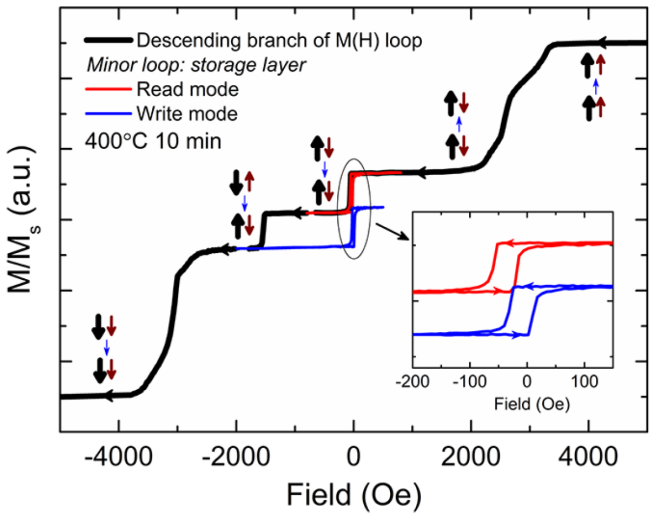

FIG. 6. Descending branch of the out-of-plane M(H) loop of the DMTJ stack presented in Figure 4b. The M(H) loops in red and blue are the minor loops of the storage layer in read and write modes, respectively.

a first concept of double MTJs, these two reference layers have fixed magnetization during memory operation.[18] Their magnetizations are set antiparallel to maximize STT efficiency. The two tunnel barriers separating the reference layers from the storage layer are prepared with different resistance-area products (RA) so that the cell still exhibits a TMR signal for the readout. Our proposed top hard reference layer can be used for this type of stack. However, here, we describe another embodiment of double-MTJ stacks in which the top reference layer above the top MgO barrier has a switchable magnetization. Thus, magnetizations of both reference layers can be set parallel to enhance the readout signal or antiparallel to maximize STT efficiency for writing. This top reference layer is called the read/write mode control layer (CL). To change between read and write mode, the magnetization of this layer is switched by a horizontal current either by spin-orbit torque or current-induced domain wall propagation in a horizontal magnetic conducting line located above the junction.19 The central component of the stack between two tunnel barriers is a composite free layer of the form FeCoB/W/FeCoB. Its magnetization is switched by STT using a vertical current. The important aspect of this double- MTJ-based memory device is the capability to modulate the STT efficiency when operating the device in either read or write modes. The magnetization of the CL must be set parallel to that of the reference layer for read mode to minimize STT influence while maximizing the TMR read signal and antiparallel to that of the reference layer for write mode operation to maximize the STT efficiency.[19] Contrary to DMTJ with fixed top reference, optimal operation is achieved here when the two tunnel barriers have a similar RA.

Figure 6 shows the descending branch of the M(H) loop of the double- MTJ stack, described in Figure 4b after annealing at 400 °C, where the arrows of different colors indicate the magnetization reversal steps upon sweeping the field from the positive to negative direction. The inset shows minor loops of the FL in read and write modes. When the magnetic field is varied from highly positive to negative, at first, both the CL and RL reverse their magnetizations in the range of 3400 to 2200 Oe. At this stage, the magnetizations of RL and CL are aligned antiparallel with their corresponding hard layers (HLs). In other words, both RL and CL are aligned along the same direction, corresponding to the read mode of the memory device. Following this reversal, the storage layer magnetization switches at -20 Oe and aligns along the negative field direction. Upon increasing the magnitude of the negative magnetic field, the CL and the top HL simultaneously reverse their magnetizations around -1.6 kOe. Following this reversal, the CL and bottom HL reverse their magnetizations, in the range of -2.7 to -3.7 kOe toward complete saturation along the negative field

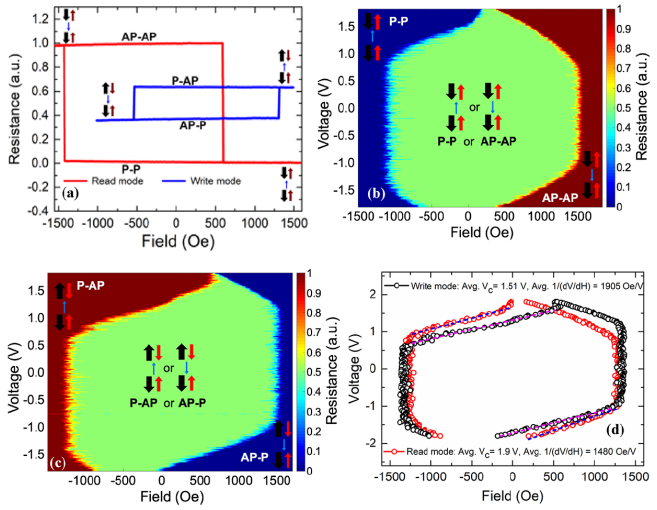

FIG. 7. (a) R(H) loops of 50 nm diameter patterned memory cell in read and write modes. Read mode exhibits four times larger TMR signal than that of write mode as expected. Voltage-field phase diagrams of a 50 nm double-MTJ memory cell in (b) read and (c) write modes, respectively. (d) Offset corrected phase boundaries of the bistable zones of phase diagrams in read and write modes.

direction. Setting the memory devices in read mode is relatively straightforward. After applying a large positive (or negative) field, decreasing (or increasing) the field to zero by default sets the device in read mode. In order to switch the device stack from read to write mode, the magnetic field should be varied from a high positive value (or negative) to a negative value (or positive) of -2 kOe (or +2 kOe) and then back to a zero field. This sets the antiparallel alignment between the RL and CL required in write mode. In write mode, when the magnetization alignment of the storage layer is parallel with RL and antiparallel with CL (P-AP), the resistance of our junction is higher compared to the AP-P alignment. AP-P alignment indicates that the storage layer's magnetization is antiparallel to the RL's magnetization and parallel to the CL's. The magnetization alignment of the storage layer in read mode is either parallel (P-P) or antiparallel (AP-AP) with both the RL and CL resulting in the lowest and highest resistance states, respectively. By contrast, in write mode, the storage layer's magnetization is antiparallel to one of the reference layers and parallel to the other.

Therefore, TMR in read mode is always larger than that in write mode, as shown by R(H) loops of a nanopatterned DMTJ cell in Figure 7a. The details about the fabrication process can be found in our previous work.[20] Moreover, the spin torques originating from the RL/MgO and MgO/CL interfaces subtract in read mode, while they add up in write mode. This allows reading at higher voltages than in conventional STT-MRAM, meaning a faster readout, while minimizing the risk of read disturbance. On the contrary, write mode has higher STT efficiency, and therefore, writing can be performed with lower voltage than in conventional STTMRAM. It can be seen from the voltage-field phase diagram of Figure 7b,c that the average critical voltage for switching in read mode (1.9 V) is larger than that in write mode (1.5 V). The experimental setup and method of measuring the voltage- field phase diagram together with a detailed explanation can be found in our previous work.[20,21] The slopes of the upper-left and lower-right boundaries of the bistable region in the stability phase diagram have two contributions, one is associated with Joule heating of the cell and another with STT, where the latter is inversely proportional to the STT efficiency prefactor $s_{t\|} = \frac{\alpha}{dV/dH} RA$, where α is the damping constant and RA is the resistance-area product of the DMTJ cell.[21] As the average inverse slope ($\frac{1}{dV/dH}$) of phase boundaries in write and read modes are respectively 1905 and 1480 Oe/V, this indicates a significant enhancement of STT efficiency in write mode compared to read mode. The STT modulation of patterned memory devices made of double-MTJ and single-MTJ stacks is discussed in more detail in another article.[22] Despite the benefit of STT modulation and, in particular, the higher STT efficiency in write mode, the large thickness of double-MTJ may lead to complications in etching of the stack, thus limiting the process yield. Therefore, special focus was given on how to reduce the total thickness and design a magnetically stable thin-double-MTJ stack. By employing a Ru/W-based multifunctional Ruderman-Kittel-Kasuya-Yosida (RKKY) coupling layer, the bottom conventional thick synthetic antiferromagnetic (SAF) layer is replaced with a thin SAF layer.23 Therefore, as represented in the schematic in

Figure 8a, the total thickness of the thin-double-MTJ stack is reduced by 5.6 nm compared to the conventional double-MTJ stack drawn in Figure 4b. Notably, the Ru/W bilayer is called multifunctional because it simultaneously ensures the function of an antiferromagnetic RKKY coupling layer, B absorbing layer, and transition from fcc to bcc parts of the stack, the detailed description of which can be found in our previous report.[23] The descending branch of the hysteresis loop of the thin DMTJ as well as the minor loops of the FL and RLs are shown in Figure 8b. The colored arrows indicate the magnetization reversal steps of the different components of the stack. It is clear from the M(H) loop that the different components of the stack possess magnetically stable properties after 400 °C annealing.

2-Bit MTJ

The third type of spintronic device, which can be envisaged, is a two-bit memory cell. A multilevel STTM-

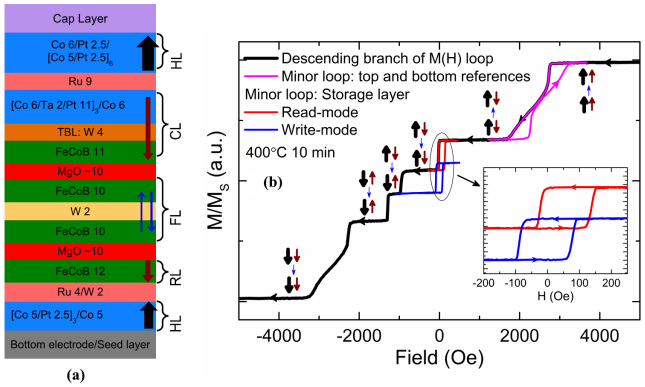

FIG. 8. (a) Schematic of the thin double-MTJ stack. The magnetization directions of HL, RL (and CL), and FL are, respectively, represented by the black, brown, and blue arrows. Thicknesses are in angstrom (Å). (b) Descending branch of the outof- plane M(H) loop of thinner DMTJ in which the bottom SAF layer below the bottom MgO of conventional DMTJ is replaced by "[Co 5/ Pt 2.5]$_3$/Co 5/Ru 4/W 2/FeCoB 12 Å". The figure includes minor loops of the top and bottom reference layers as well as (in inset) the storage layer in read and write modes.

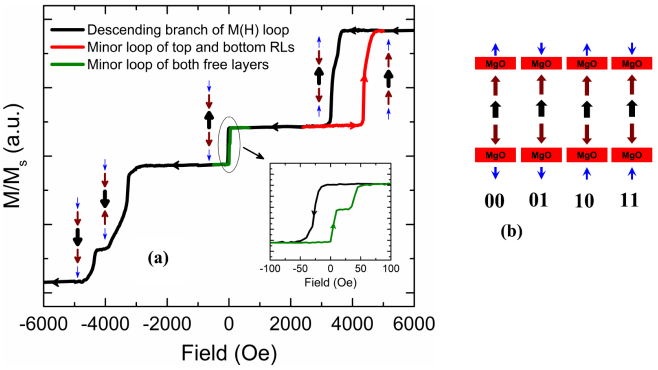

FIG. 9. (a) Descending branch of the out-of-plane M(H) loop of the 2-bit memory stack [as shown in the schematic in Figure 4c] comprising "Ta 10/Pt 30/Co 5/W 2/FeCoB 8/MgO 10/FeCoB 11/W 3.5/[Co 6/Ta 2/Pt 11]$_3$/Co 6/Ru 9/Co 6/Pt 2.5/[Co 5/Pt 2.5]6/Co 5/Ru 9/[Co 5/Pt 2.5]$_3$/Co 5/Ta 3/FeCoB 12/MgO 10/ FeCoB 14/W20/Pt 30 Å" after annealing at 340 °C for 30 min. Depending on the storage layers' magnetization orientations, four different resistances can be produced as described in (b). Assuming bottom MgO is thicker and possesses higher RA product compared to that of top MgO, the four different storage layer configurations corresponding to 00, 01, 10, and 11 will, respectively, give rise to higher resistances.

RAM configuration has already been proposed in previous reports.[24–26] However, they all suffer from two steps of writing, which consumes more energy and limits the writing speed. A novel stack configuration of a multilevel memory cell is shown in Figure 4c. In this configuration, there are two storage layers: one at the top and another at the bottom of the stack and interfaced with two MgO barriers with different RA products. On the opposite sides of the two MgO barriers, there are two reference layers that are antiferromagnetically coupled with a single hard layer located in the middle of the stack. Depending on the magnetization orientations of the storage layers with respect to the reference layers, it is possible to obtain four different resistance levels, which are schematically represented in Figure 9b. The top and bottom storage layers can be independently written by STT and SOT, respectively.

In order to write both the storage layers by STT, they must be designed in such a way that the current required to write one storage layer does not flip the second storage layer. In the case of writing the top storage layer by STT and the bottom storage layer by SOT, the design has to be adapted so that the top storage layer possesses lower STT switching current than the bottom storage layer. The bottom storage layer can also be written by a combination of SOT and STT.[27] It is noteworthy that SOT can also be used to write both storage layers, if the technological challenges of four terminal device fabrications are overcome with efficient SOT switching of the top layer. The magnetic cycle of the stack, described in Figure 4c is shown in Figure 9a. Coming from high positive fields, at first, both the top and bottom RLs' magnetizations reverse at 3.5 kOe and become aligned opposite to the HL magnetization. Following this reversal, the magnetizations of both storage layers flip upon a small negative field of about -25 Oe. Increasing the magnitude of the negative field further, at -3.3 kOe, the bottom RL and the HL magnetizations simultaneously flip followed by the reversal of the bottom reference magnetization at -4.35 kOe leading to complete saturation along the negative field direction. The inset shows the minor loop corresponding to the reversal of both storage layers. The two steps of minor loops indicate that the top and bottom storage layers have different coercivities, therefore different PMAs, due to the differences in the free layers, their growth, and in the adjacent MgO layers.

CONCLUSIONS

In summary, we demonstrated novel seedless (Co/Ta/Pt)- based multilayers whose perpendicular anisotropy and thermal stability upon annealing are significantly improved compared to those of conventional Co/Pt SL-MLs, even after annealing at BEOL process temperature. Using a Ta-inserted SL-ML, a top-pinned stack that is able to withstand 425 °C annealing was realized. Moreover, a BEOL compatible double-MTJ stack was designed employing the SL-ML as a control layer. The memory cells patterned out of this stack show high voltage reading in read mode together with lower voltage writing in write mode operation. In addition,

by using a novel Ru/W RKKY coupling layer, the total thickness of the double-MTJ stack was reduced by 5.6 nm to address the etching challenge of the double-MTJ stack. Finally, we have also demonstrated a 2-bit memory stack utilizing the SL-ML, where the four resistance states can be independently written by STT or SOT or a combination of both. Hence, the proposed SL-MLs constitute a promising solution for different spintronic memory devices or logic applications requiring a top hard reference layer.

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