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Salim Dahmani, Adama Seck Elhadji, Cyril Buttay, Bruno Allard, Hassan Maher, et al.. Characterization and modeling protocol for GaN-on-Si power transistors. The 11th IEEE Workshop on Wide Bandgap Power Devices & Applications (WIPDA), IEEE, Nov 2024, Dayton, OH, United States. pp.1-6, 10.1109/WiPDA62103.2024.10773354 . hal-04885692

HAL Id: hal-04885692

<https://hal.science/hal-04885692v1>

Submitted on 14 Jan 2025

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Characterization and modeling protocol for GaN-on-Si power transistors

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Abstract—Designing a monolithic circuit around a GaN/Si High electron mobility power transistor requires accurate characterization and device modeling. The characterization aims to provide adequate parameters to the transistor model.

In particular, the characterization protocol presented in this paper enables to capture a wide range of current, from very low currents (a few hundred picoamperes to a few nanoamperes) when the transistor is off (sub-threshold), to high currents (several hundred milliamperes to a few amperes) when the transistor is on. A special care is given to detecting any drift in the component characteristics which may be caused by the characterization step.

A modeling procedure is also presented, to build a SPICE parametric model of the transistor. An R^2 criterion is used to validate the resulting models.

Index Terms—HEMT, LTSpice, Characterization, Behavioral model, Power electronic

I. INTRODUCTION

A new HEMT (High Electron Mobility Transistors) technology is being developed at the Nano Technology and Nanosystems Laboratory (LN2) in Sherbrooke. The ultimate goal of the technology is to enable the manufacturing of simple, all-GaN integrated circuits (ICs). To this end, a design kit is needed to enable IC design: models of manufacturable components, based on their geometric parameters, electrical circuit diagrams associating these components, and design steps for the corresponding circuits.

As the component models are intended for circuit simulation, SPICE-type models are chosen. Several models are

proposed in the literature. The static and dynamic models used in this article offer a tradeoff between models of various commercial transistors (EPC and GaN System), and articles such as [1], which presents a segmented transistor model (divided into distinct parts according to the evolution of V_{gs} and V_{ds}). [2] studies the difference between two transistor structures based on their detailed models. Other models are presented in [3]. Y.Hu [4] presents a parameter identification method based on the GA-LM optimization algorithm for models inspired by the work of H.Li [5], which highlights non-segmented models. Non-segmented models are useful to avoid any discontinuity in the static characteristic. All these modeling approaches have almost similar static and dynamic characteristics, and have been adapted for our application to have a single model parametric by transistor width W , and thus build switching circuits using only one behavioral model by varying this parameter W .

While models equations are detailed in the literature, the characterization steps required to identify the parameters of these models are often described much more briefly, if not overlooked. As HeMT transistors tend to have very large current dynamics, low parasitic capacitances (in the picofarad range), and may be sensitive to drift in performance when stressed, it is important to clarify how the experimental data is acquired. In this paper, a special care is given to describing the characterization procedure.

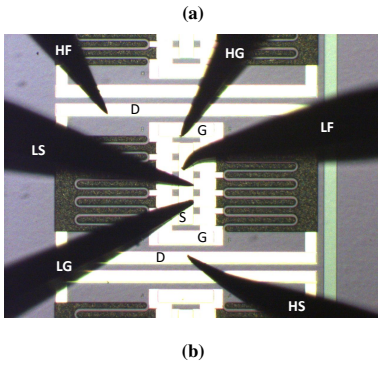
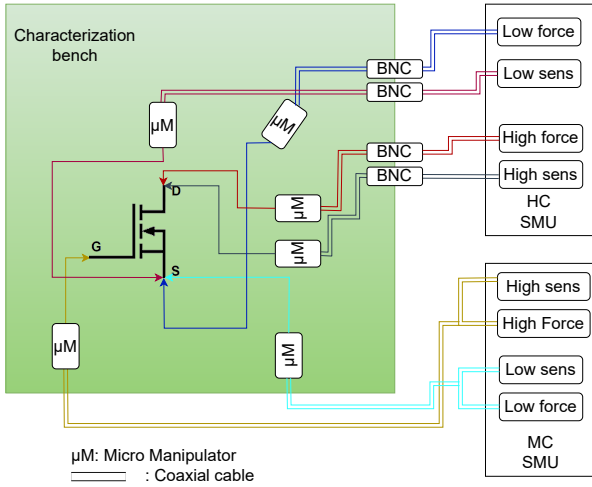


Fig. 1: (a) Connection for static characteristics $I_{ds} = f(V_{gs})$ and $I_{ds} = f(V_{ds}, V_{gs})$. (b) photograph of the transistor with the probes.

II. EXPERIMENTAL CHARACTERISTICS

This section describes the various procedures for experimental characterization of transistors. In all cases, the measurements are carried out using a Keysight B1505A curve tracer, combined with a probe station for adequate connection with the components under test, on wafer (with the wafer substrate connected to the transistor source).

A. Static measurements

To avoid wire and contact resistances, a 4 point probes measurement is used to extract the static characteristics Fig. 1. The negative terminal (cold point) of the transistor's gate bias is connected to the source using a dedicated probe. Output characteristics (OC) $I_{ds} = f(V_{ds}, V_{gs})$ as in Fig. 2(a), and transfer characteristics (TC) $I_{ds} = f(V_{gs})$ for a fixed V_{ds} as in Fig. 2(b) are obtained.

Pulse measurements (*Period* 20ms, *Pulse Width* 150μs, *Measurement Delay* 130μs and *Integration Time* 20μs) are carried out for high current levels, to avoid transistor self-heating, but the results are affected by noise (several tens or hundreds of microamperes) at low currents. Low-current measurements (a few hundreds nanoamperes to a few microamperes) require long acquisition times (tens or hundreds

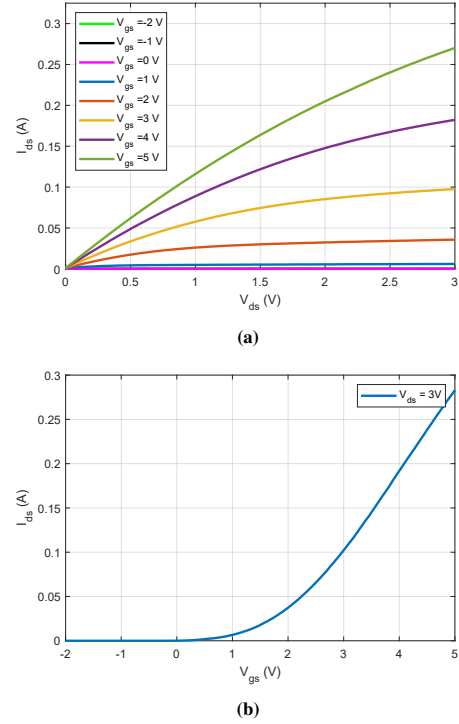


Fig. 2: (a) Measured output characteristics. (b) Measured transfer characteristics $V_{ds} = 3V$.

of milliseconds), which are incompatible with pulse measurements. A two-stage characterization is thus defined for high-dynamic measurements (covering both low and high current levels, while limiting self-heating): a first measurement is carried out in continuous mode, with a current compliance (limit) set at 10mA (Fig. 3(a), blue curve), and a second in pulse mode, enabling higher current levels (several hundred milliamperes or more) to be reached without damaging the transistor (Fig. 3(a), orange curve). The two data sets are then concatenated, starting from the point where the difference between the two measurements is smallest ($\min(\text{abs}(I_c - I_p))$).

B. Capacitance measurements

HEMT transistor capacitance are typically of the order of a few picofarads to a few hundred picofarad, values comparable to those of the coaxial cables used to connect the tracer feature to the characterisation bench. In order to verify the accuracy of the measurements and the absence of any effect of the connectors, a printed circuit board comprising capacitors of 1, 10, 33, 100, 220 and 1000 pF at 1% tolerance is used. Measurements are made for various oscillator frequencies, after performing the connector compensation procedure ("open circuit" and "closed circuit") provided by the curve tracer. From these measurements, we can conclude that:

- 1) Measurement limits are of the order of 0.05 pF (Fig. 4)
- 2) A frequency of 100 kHz allows for measuring capacitances between 10 pF and 1 nF with values within their tolerances, and the closest measurement to the actual value of 1 pF

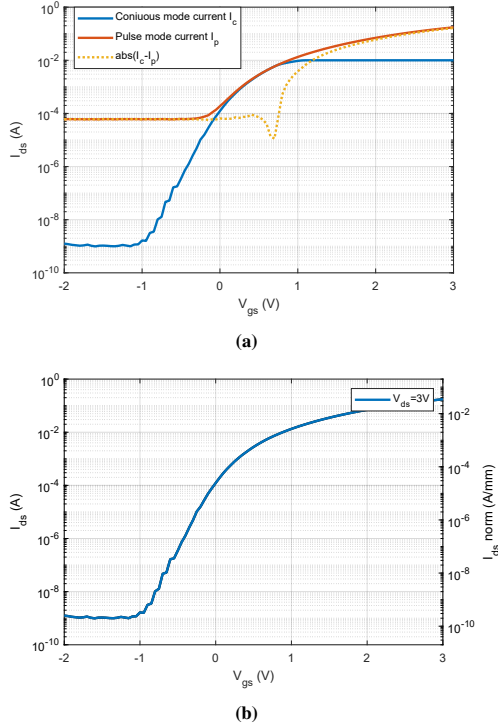


Fig. 3: (a) Measured drain current in DC (continuous) and pulsed mode for $V_{ds} = 3$ V. (b) Reconstructed transfer characteristics.

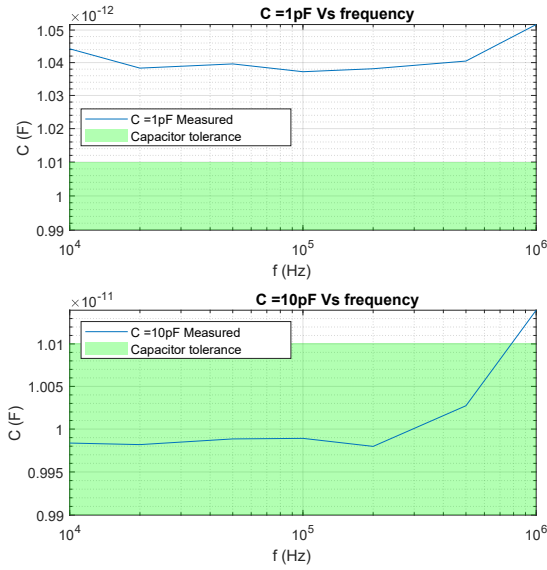


Fig. 4: Measurements on reference capacitors (1 pF and 10 pF) as a function of frequency. The green area correspond to the rated tolerance on the capacitors (1 % tolerance).

Using the Keysight B1505A, guarded measurements are conducted to characterize the internal capacitance of the transistors, following the connections illustrated in Fig. 5

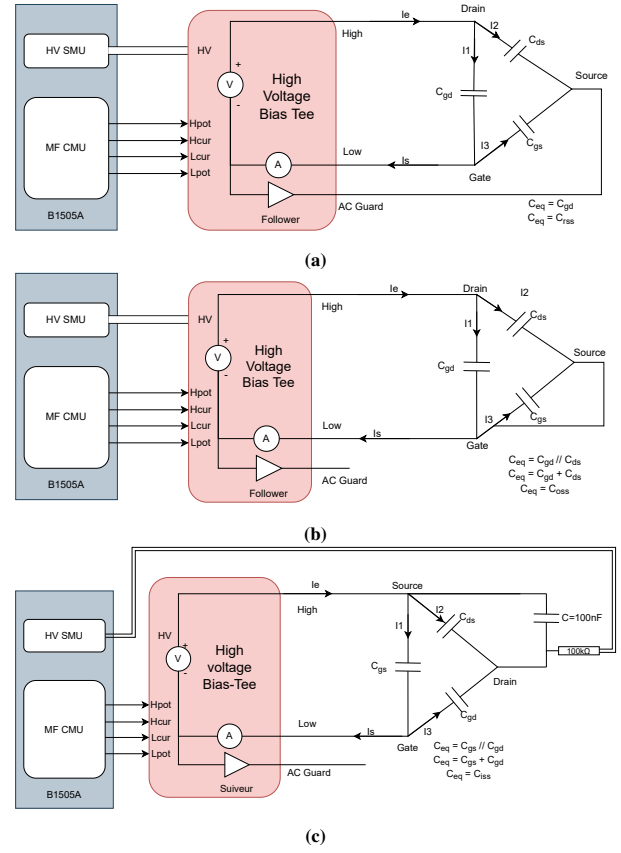


Fig. 5: Connection for internal capacitance measurements: $C_{r_{ss}}$ (a), $C_{o_{ss}}$ (b) and $C_{i_{ss}}$ (c)

III. MODELING AND PARAMETER IDENTIFICATION PROTOCOL

A. Behavioral Model

Inspired by the work of Y.Hu [4] and S.ghosh [6], the core of the behavioral model of a HEMT consists in a nonlinear current generator that represents the behavior of the transistor's channel. This current generator is surrounded by several parasitic elements that model the intrinsic capacitive and resistive effects of the component. As shown in Fig. 6, it is made up of the following parts:

- Current Generator:** This models the drain-source current (I_{ds}) as a function of the voltages applied to the transistor terminals (V_{gs} and V_{ds}). The generator is nonlinear to reflect the actual behavior of the transistor.
- Internal capacitances:** The model includes several parasitic capacitances that represent the intrinsic capacitive effects of the HEMT:

- Gate-source capacitance (C_{gs})
- Gate-drain capacitance (C_{gd})
- Drain-source capacitance (C_{ds})

These capacitances are typically nonlinear and depend on the applied voltages.

- Access resistors:** The model incorporates parasitic resistances to represent the access resistances to the terminals

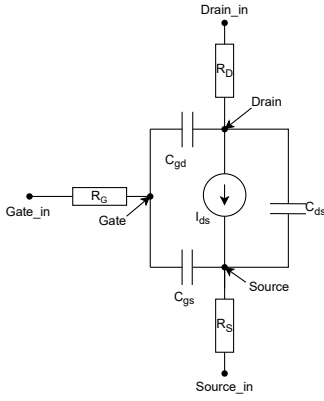


Fig. 6: Model structure

(on-chip metallization):

- Source resistance (R_S)
- Drain resistance (R_D)
- Gate resistance (R_G)

B. Models

1) *Transfer characteristics model*: H.Li [5] proposes an expression describing the transfer characteristic $I_{ds} = f(V_{gs})$ at fixed V_{ds} . The latter model has been adapted to introduce a parameter W corresponding to the channel width, in order to be able to propose a parametric model (1). For the transistors tested here, W is either 5, 10, 15 or 20 mm.

$$I_{ds}(W, V_{gs}) = A \times W \times \log \left(1 + e^{\frac{V_{gs} - V_{th}}{B}} \right) \quad (1)$$

Identifying this expression with the transfer characteristic measurement presented in Fig. 2(b), yields the parameter V_{th} (transistor threshold voltage), as well as both empirical parameters A and B .

2) *Output characteristics model*: As with the transfer function, the empirical output characteristic model proposed by Y.Hu [4] and used in the models of transistors from EPC or GaN System is adapted to incorporate the W parameter:

$$I_{ds}(W, V_{gs}, V_{ds}) = k_1 \times W \times \log \left(1 + e^{\frac{V_{gs} - V_{th}}{B}} \right) \times \frac{V_{ds}}{1 + (k_2 + k_3 \times V_{gs} + k_4 \times V_{gs}^2) \times V_{ds}} \times \alpha(V_{gs}) \quad (2)$$

$$\alpha(V_{gs}) = (k_5 \times V_{gs}^3 + k_6 \times V_{gs}^2 + k_7 \times V_{gs} + k_8) \quad (3)$$

with $k_{1...8}$ being the empirical parameters to be identified with the experimentally acquired output characteristics from Fig. 2(a).

3) *Access resistance*: Based on the component geometry (number of fingers, finger length, finger width and contact thickness, not detailed here for the sake of brevity), we can calculate the value of the contact resistances:

$$R_{metal}(W) = 1.883 \times (10^{-3}) \times W + 0.131 \quad (4)$$

$$R_D = 0.33 \times R_{metal}(W) \quad (5)$$

$$R_S = 0.67 \times R_{metal}(W) \quad (6)$$

Concerning R_G , based on the work of B.Hassan [7], and the geometry of the gate, R_G can be calculated:

$$R_G(W) = 33.31 \times (10^{-3}) \times W \quad (7)$$

4) *Capacitance model*: Internal capacitances are modeled by considering the work of Y.Hu [4] adapted to our application. The chosen model represents the various capacitance depletions "jumps" in the $C(V)$ characteristic as exponential terms:

$$C(W, V_{ds}) = W \times \left(m_1 \times \left(1 - \frac{1}{1 + e^{-\left(\frac{V_{ds} - m_2}{m_3}\right)}} \right) + m_4 \times \left(1 - \frac{1}{1 + e^{-\left(\frac{V_{ds} - m_5}{m_6}\right)}} \right) + m_7 \right) \quad (8)$$

with $m_{1...7}$ being empirical parameters obtained from fitting the equation with the experimental $C(V)$ curves for each of the parasitic capacitances C_{gs} , C_{gd} and C_{ds} .

Note that to represent nonlinear capacitances in LTSpice, it is necessary to use an expression of the charge $Q = \int C dV_{ds}$ rather than expressing directly the capacitance:

$$Q(W, V_{ds}) = -W \times \left(m_1 \times m_3 \times \log \left(e^{-\frac{V_{ds} - m_2}{m_3}} + 1 \right) - V_{ds} \times m_7 + m_4 \times m_6 \times \log \left(e^{-\frac{V_{ds} - m_5}{m_6}} + 1 \right) \right) \quad (9)$$

C. Curve Fitting and Parameter Identification

Fig. 7 describes the procedure to identify the parameters (A, V_{th}, B) of the transfer function (1), using the NLSF method (*Nonlinear Least Squares Fitting*). Applying this identification to transistors of all channel widths W (5, 10, 15 and 20 mm), allows to derive constant threshold voltage V_{th} B values (Fig. 8) regardless of W .

Identifying first V_{th} and B through (1) has the advantage of being more accurate and of accelerating the subsequent identification of the k_i parameters from (2), with 8 parameters to optimize instead of 10.

Because R_D and R_S are estimated from the transistor geometry (and not characterized experimentally), their effect must be removed from the measured output characteristic. Therefore, before fitting the parameters, the experimental OC is processed to remove the resistive voltage drop across R_D and R_S :

$$I_{ds} = f(V_{ds} - (I_{ds} \times (R_D + R_S)), V_{gs}) \quad (10)$$

The match between measured data and fitted model visible in Fig. 8 is found to be satisfying as $R^2 > 0.99$, and the discrepancies are within the typical variation of one transistor to another on the same wafer.

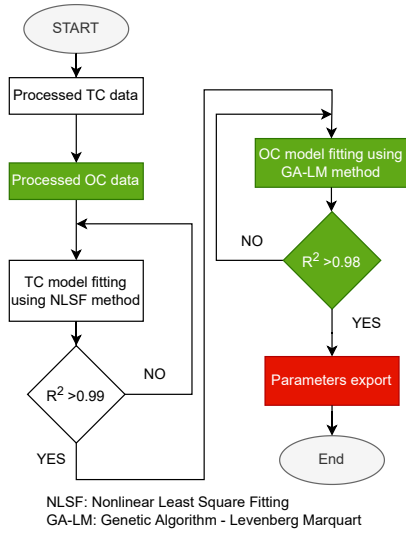


Fig. 7: Static fitting process

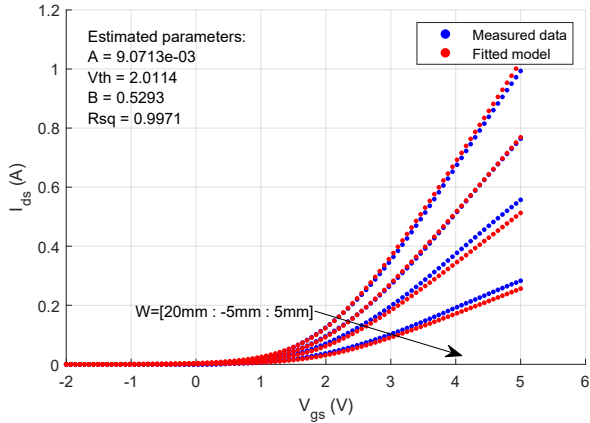


Fig. 8: Fitted transfer characteristics and measured data

In order to identify all the parameters of the output characteristics and capacities ($k_1 \dots k_8$), ($m_1 \dots m_7$), several optimization methods were investigated. The chosen solution is the GA-LM method (*Genetic Algorithm-Levenberg Marquardt*) using the built-in Matlab function `ga` for the optimization linked to the genetic algorithm, then the function `lsqcurvefit` with the algorithm *Levenberg-Marquardt* as argument, what provides parameters that best approximate the measured data ($R^2 > 0.98$) with execution times averaging 30s for static parameter extraction and 90s for capacitance parameter extraction.

Note that while the experimental characterization step yields C_{oss} , C_{rss} and C_{iss} characteristics, it is the C_{gs} , C_{gd} and C_{ds} capacitances that have to be integrated into the behavioral model. Fig. 10 shows the simple transformation which is applied to the experimental data before fitting (8) for C_{gs} , C_{gd} and C_{ds} .

As an example, the full LTSpice model listing is provided in appendix.

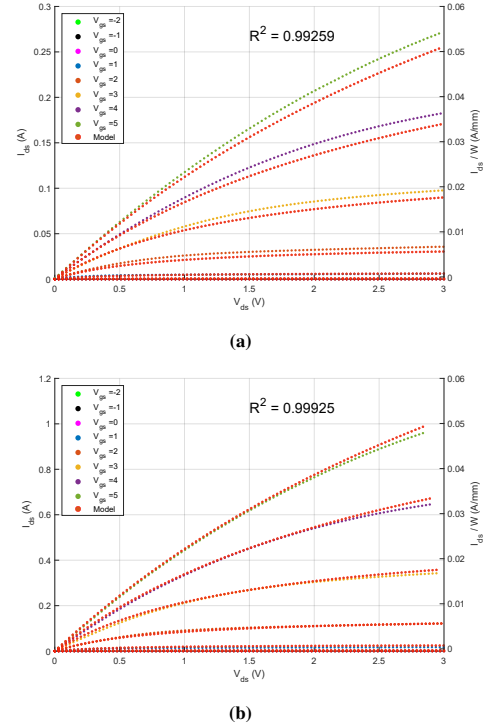


Fig. 9: Fitted Output Characteristics for different channel width: $W = 5$ mm (a), and $W = 20$ mm (b)

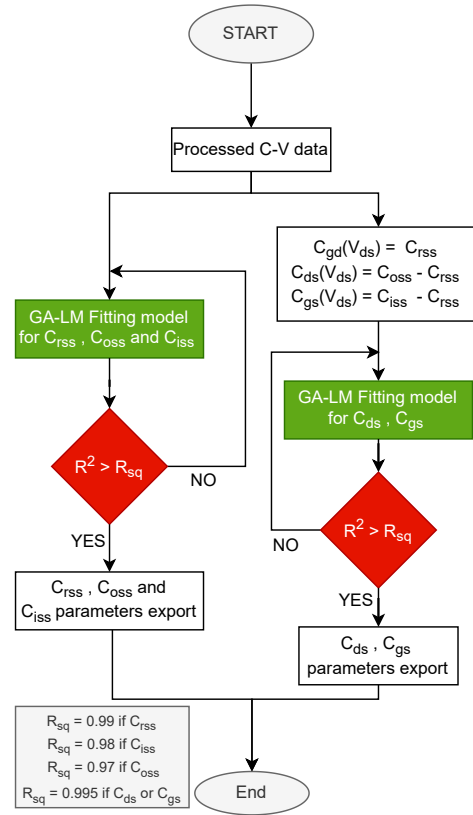


Fig. 10: Capacitance fitting process

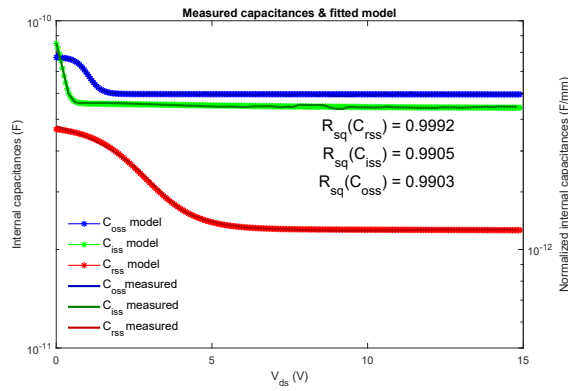


Fig. 11: Fitted capacitance measurement

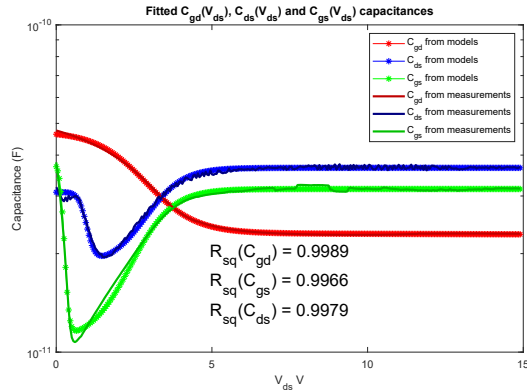


Fig. 12: Fitted internal capacitance

IV. CONCLUSION

This paper presents a robust measurement protocol for acquiring all the data needed to identify the complete SPICE model of GaN transistors. A detailed description has been given to allow readers to reproduce the protocol. The method used to identify model parameters is based on built-in Matlab functions, and produces an accurate model parameterized according to transistor channel width.

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APPENDIX

```
.subckt C_TLN2_bis gate_in drain_in source_in

* Initial parameters and expressions from matlab
.param W=20 Vth=2.01138231813701 R_metal=1
+ .882914254703328*(1e-3)*W+0.130976543972235
* Access resistances expressions
+ Rg = 0.0333083399662351*W
+ Rd = 0.33*R_metal
+ Rs = 0.67*R_metal
* Ids(Vds.Vgs.W) parameters
+ A1=0.00690199586454018 A2=0.529265287935854
+ A3=2.94486884470684 A4=-1.07664952030675
+ A5=0.105116251630319 A6=-0.00240584222464247
+ A7=0.158934238445223 A8=-1.45463849250308
+ A9=4.28628414230330
* Internal capacitances parameters
+ m1gd=1.20809827280968e-12 m2gd=2.58031760073394
+ m3gd=0.798773278669305 m4gd=4.91501170943199e-14
+ m5gd=6.96521824371346 m6gd=14.9128880710339
+ m7gd=1.12730200493839e-12 m1ds=9.09892943630172e
+ -13
+ m2ds=3.08198838128302 m3ds=-0.588334791808129
+ m4ds=6.16269073451083e-13 m5ds=0.943016729717256
+ m6ds=0.133628399386407 m7ds=9.18413785128724e-13
+ m1gs=1.34717733636361e-12 m2gs=0.22251688000679
+ m3gs=0.0719671225128173 m4gs=1.03662198020512e-12
+ m5gs=2.73677023968697 m6gs=-0.643237387475968
+ m7gs=5.38893294967622e-13

* Access resistances
Rg gate_in gate {Rg}
Rd drain_in drain {Rd}
Rs source_in source {Rs}

* Convergence resistances
Rdsconv drain_in source_in {1000000Meg}
Rgsconv gate_in source_in {1000000Meg}
Rgdconv drain_in gate_in {1000000Meg}

B1 Drain Source I=
+ if(
+ v(drain,source)>0,
+ A1*W*log(1+exp((v(gate,source)-Vth)/A2))*v(drain
+ ,source)/(1+(A3+A4*v(gate,source)+A5*v(gate,source)
+ **2)*v(drain,source))*(A6*v(gate,source)**3 + A7*(v
+ +gate,source)**2 + A8*v(gate,source) + A9),
+ -A1*W*log(1+exp((v(gate,drain)-Vth)/A2))*v(
+ +source,drain)/(1+(A3+A4*v(gate,drain)+A5*v(gate,
+ +drain)**2)*v(source,drain))*(A6*v(gate,drain)**3 +
+ +A7*(v(gate,drain)**2 + A8*v(gate,drain) + A9)
+ )

* Internal capacitances
C_GD gate drain Q = W*(m1gd*m3gd*log(exp(-(V(drain,
+gate) - m2gd)/m3gd) + 1) - V(drain,gate)*m7gd +
+m4gd*m6gd*log(exp(-(V(drain,gate) - m5gd)/m6gd) +
+1))

C_GS gate source Q = -W*(m1gs*m3gs*log(exp(-(V(drain
+,source) - m2gs)/m3gs) + 1) - V(drain,source)*m7gs
++ m4gs*m6gs*log(exp(-(V(drain,source) - m5gs)/m6gs)
+ + 1))

C_SD source drain Q = W*(m1ds*m3ds*log(exp(-(V(drain
+,source) - m2ds)/m3ds) + 1) - V(drain,source)*m7ds
++ m4ds*m6ds*log(exp(-(V(drain,source) - m5ds)/m6ds)
+ + 1))

.ends
```