Automatic Model Generation of Power Printed Circuit Boards Based on Open Standards

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***Abstract*—Printed Circuit Board technology is increasingly used to design power electronic converters. Advanced electronics Computed-Aided Design (eCAD) tools allow us to describe the implementation of such a converter fully. Here, we investigate the automatic generation of electrical and thermal models from eCAD designs, using an open standard data exchange format (IPC-2581). We implement a simplification method because PCB designs have many intricate details (in particular, they may contain thousands of micro-vias). This allows to build 3D FEM models which can be simulated in a reasonable time, with very little assistance from the designer.**

I. Introduction — Simulation for the Design of Power Electronics Circuits

Designing a power converter is a complex task, because it requires to address many objectives at the same time: the resulting object must achieve the desired conversion efficiency, operate reliably, be as small and lightweight as possible, and remain within budget. From a designer point-of-view, this means identifying the suitable circuit topology, the best set of components and operating conditions (switching frequency, current and voltage ripple, etc.), but also designing a thermal management system and filters for electromagnetic compatibility.

Because of the relative simplicity of power electronics circuits (typically a handful of power semiconductor devices, plus some passive components and gate drive circuits), circuit simulation may seem well suited to the design of power converters. However, this is not the case: Ref. [1] shows that although numerical modelling and simulation tools are very accurate for the design of power transformer or for the prototyping of control algorithms, they fail at simulating the switching waveforms of a moderately complex Dual Active Bridge converter. A first cause is the limitation of circuit simulators and devices models. A second cause is the difficulty in generating circuit models (including circuit parasitics, such as stray inductance or capacitance), or reduced-order thermal models, because of the heterogeneity of standard manufacturing technology (there is no unified description of a converter: modules, busbars, driver PCBs are all designed using separate tools, by different engineers).

Over the years, many research groups have explored different approaches for the modelling of power electronics circuits, often focusing on the power module, where the fastest transients and highest power densities are encountered. In [2], the authors have relied on finite element simulation, using the 3D Computer Aided Design (CAD) geometry of their module. In [3], the focus is on the generation of Reduced-Order Models (ROMs), so that subsequent simulations can be run quickly. A similar approach is proposed in [4] for the generation of compact thermal models. An optimization tool for the routing of a power module is proposed in [5], taking into account electrical, thermal and thermo-mechanical aspects. All these approaches demonstrate impressive results, but they are limited to a very specific technology (typically bare semiconductor chips mounted on ceramic substrates) and require a significant preparation effort for their input data (simplification of the geometry, manual definition of the boundary conditions, etc.)

Recent developments in Printed Circuit Board (PCB) technology have made it possible to design high performance power converter using PCBs: embedding power semiconductor chips within a PCB [6] allows to reduce the length of the interconnects (hence reducing stray inductance), to bring the chips closer to the thermal

management devices (heatsinks), and to use the same integration technology for the power devices and their peripheral components (power passives, gate drive circuits...). As a consequence, several authors have explored the generation of models for PCB-based electronics. The approach in [7] manages the complexity of a PCB layout by relying on the designer to select the few copper track(s) which must be considered for further analysis (thermal behaviour or calculation of stray inductances). The opposite approach is developed in [8]: small models are pre-computed for elementary circuits, and combined at implementation time to build a complete, yet simplified model of the entire circuit.

In this paper, we develop yet another approach [9]: here, the idea is to consider the electronics Computer Aided Design (eCAD) files as a complete description of a converter. As they contain all the relevant information, these files can therefore be used to automatically generate ROMs, with minimum input from the designer. This requires to export the required data from the eCAD software (Altium Designer, KiCad, etc.), to build a 3D model in FEM simulation tools (Ansys, Comsol), to run a number of simulations, and to use the results to identify the parameters of some ROMs. This approach as been successfully demonstrated for electrical [10] and thermal [11] modelling.

II. Data Management

A. Moving to Standard File Formats and Open Source Tools

The proof of concept presented in [10] and [11] uses proprietary software: PCBs are designed using Altium Designer, their geometry is exported in a proprietary file format (EDB, Ansys), and then loaded into Ansys Q3D Extractor (for the calculation of circuit parasitics) and Ansys Mechanical (for thermal modelling). While this software workflow was found to work well, it is also relatively fragile, as new software versions often introduce new features or changes requiring rewriting of some of the interface code. Furthermore, the use of proprietary file formats makes it difficult to switch from one tool to another (switch to another eCAD software tool for example). Finally, open-source software allows wide dissemination, and benefits the research community.

Several file formats have been used over the years for the description of PCB designs. The venerable "Gerber" format, introduced more than 40 years ago, has undergone multiple revisions, and is still in wide use today. However, in most of its uses, it merely consists in a collection of 2-D geometries (one per "layer" of the PCB design: copper layers, solder mask, mechanical, etc.), loosing many of the features required to build a 3-D model, such as the thickness of each layer, or the stacking order. ODB, later ODB++ was designed in the 90s to allow for exchange between software tools. It includes many features that allows to build a full 3-D model of a design (description of the layer stack-up, list of components, etc.), but its adoption has remained limited, maybe because of its proprietary nature. More recently, IPC-2581 has been introduced as an open format, and is now in its 3rd revision (IPC-2581C). Its specifications are available [12], and have been implemented by a variety of software vendors. KiCad (an open-source eCAD software) introduced IPC-2581 export in its latest version (8). Furthermore, IPC-2581 files use XML formatting [13], which can easily be processed by the many parsing libraries available for a variety of programming languages. In this article, we describe the use of IPC-2581 for the automatic generation of models from two eCAD software tools (Altium Designer and KiCad)

B. File Preparation

In [10], most of the data export is taken care of using a C++ script running as an Altium Designer plugin. Because the objective here is to propose a versatile solution which can be used with different eCAD software, on various computer platforms, the code is written as a standalone python script, which takes IPC-2581 files as an input, and outputs the data required to build a model in Ansys Q3D Extractor and Ansys mechanical.

1) Variants in IPC-2581 files: IPC-2581 addresses a variety of usages with various features, from the description of artwork for board manufacturers to the list of components for assembly (Bill Of Materials, BOM). To control the amount of data circulated between a designer and their subcontractors, the IPC-2581 introduce "sections" which may or may not be present in a file, depending on its intended use: obviously, the BOM is not required for board manufacturing, nor the description of the inner copper layers for component assembly.

In practice, this flexibility means that not all eCAD tools implement all features. For example, files generated using KiCad do not contain a `stackup` section (description of the order and thickness of each copper and dielectric layer in the board), while files generated by Altium include one. This `stackup` section is needed to later build a 3D model of the board, as it provides all the "z" (vertical) information. As a workaround, our code

inserts a `stackup` section in the files lacking it, using two sources of data: the ”PadStack” section in the file, which also contain a list of the layers, and a user prompt (asking the user for the thickness of each layer, as this information is not present in IPC-2581 files exported by KiCad).

2) Additional file: Providing they contain the required sections, IPC-2581 files fully describe a board geometry. However, additional information is required for the modelling:

- the description of a board’s physical interfaces, such as the presence of a heatsink or the location of the heat sources (for thermal calculations) or the presence of a conductive plane in proximity of the board (for the computation of parasitic inductances and capacitances). This is also acquired by prompting the user to select which of the components should be considered for the calculation of thermal resistance, or what heat exchange coefficient should be applied to each of the external surfaces of the PCB [11];
- some directives for the construction of a 3D model, in particular the list of vias which can be grouped into a simpler block (see next section).

because it does not belong to the IPC-2581 file, and because it is needed to build the 3D model in the FEM tool (Ansys), this information is stored in a plain text file. This file is then loaded by an Ansys script when building the 3D model. This text file is generated by our Python script.

III. Simplification of the Geometry

A. Clustering of vias

Power PCBs often contain a large quantity of vias, as cluster of these are used to carry strong currents and to improve through-plane thermal conductivity (using arrays of so-called ”thermal vias”). This is particularly true for PCBs with embedded dies, for which laser-drilled microvias are required. PCBs with thousands of vias are commonly encountered.

This is a problem when preparing a 3D model for FEM simulation, as each of these vias must be meshed in a large number of tiny elements (the typical thickness for the copper plating of vias is 35 µm, resulting in mesh elements of about 10 µm on a side). Such FEM model would end up being too large to be processed.

The workaround developed in [10] is to replace via areas with rectangular blocks having equivalent thermal and electrical conductivities. This results in a dramatic reduction in elements count, and consequently in more manageable models.

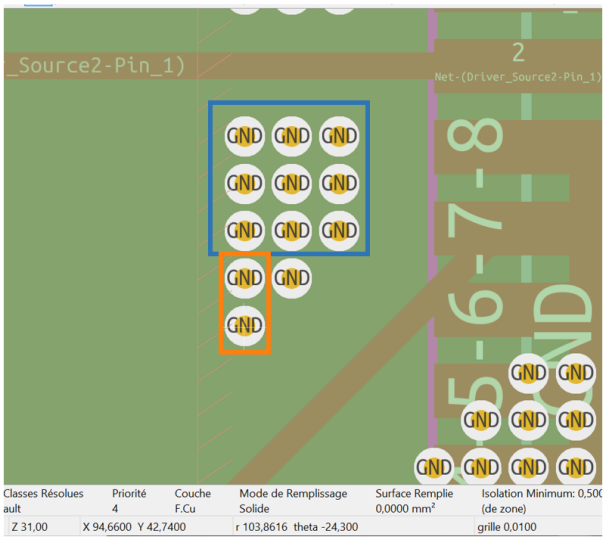


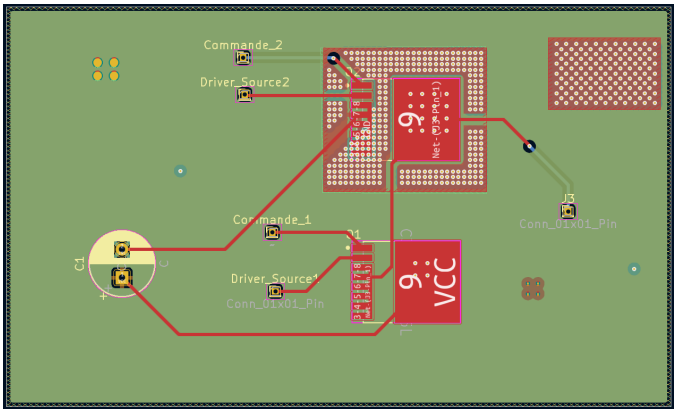
Fig. 1: Principle of via simplification: individual vias are grouped into rectangular blocks wherever possible. Here 9 vias are grouped in a square block (blue), two in a rectangle (orange), and one is left alone.

The principle is presented in Fig. 1: groups of vias are detected, according to their distance from each other, as well as to the layers and electric potentials they are connected to. Vias which are sufficiently close to each other (distance arbitrarily chosen to 2 mm), are connected to the same potentials and have the same top and bottom layers are submitted to an algorithm known as ”largest rectangular area in a histogram” [14]. Once the largest rectangle has been identified, the corresponding vias are removed from the group, and the algorithm is run again. The process is repeated until all vias have been associated to a rectangle, or only isolated vias remain. The process is repeated for each group of vias in the board.

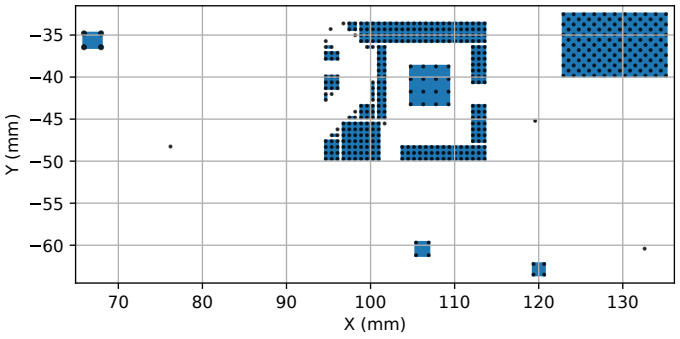
B. Examples

3 PCB designs are considered here to validate the algorithm:

- a non-functional test PCB (Fig. 2) designed using KiCad. It implements a variety of ”tricky” cases: aligned and staggered vias, via areas with complex shapes, areas cut in two by a track at a different potential…
- a more realistic case (Fig. 3): a half-bridge structure with associated gate drivers, designed on a 4-layer PCB by a second person using Altium Designer;



(a)



(b)

Fig. 2: (a) 2-layer test layout having via areas with a complex shape and (b) identification of the via groups (black dots: vias, blue rectangles: the proposed via clustering).

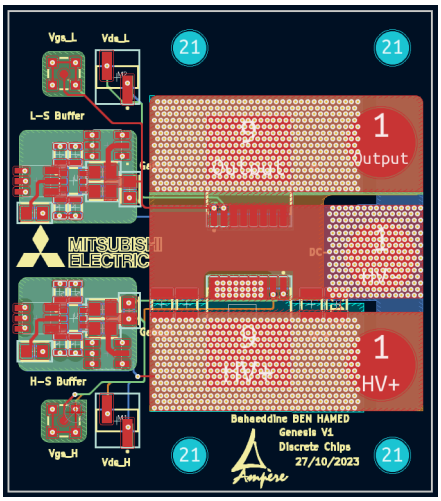
- another board (Fig. 4), designed in KiCad by yet another person, to ensure files generated using another eCAD software, in a different team would still be processed properly.

Tab. I summarises the results of the via simplification algorithm. It can be seen that many of the vias can be grouped, resulting in a much smaller number of items in the geometry. For example, the Half bridge board includes 1286 vias, 1239 of which can be replaced by only 7 rectangles, with only 47 vias remaining ungrouped.

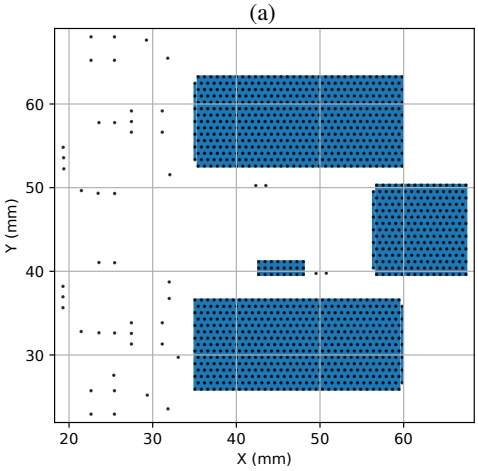
C. *Further simplification*

When building the 3D model in Ansys, the following simplifications are performed [10]:

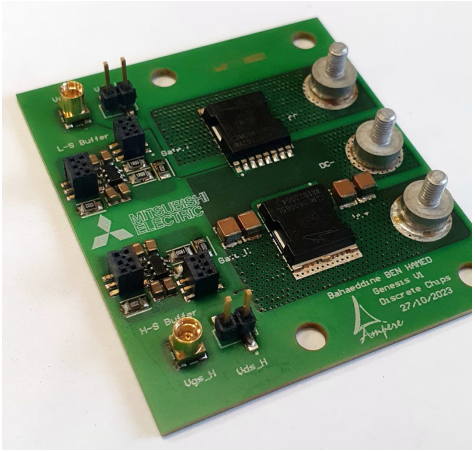
- ”faceting”: curves (especially cylindrical vias) are replaced with prismatic shapes with only 4 facets. This is a feature of the Ansys importing tool (HFSS Layout). As described in [10], this has negligible



(a)



(b)

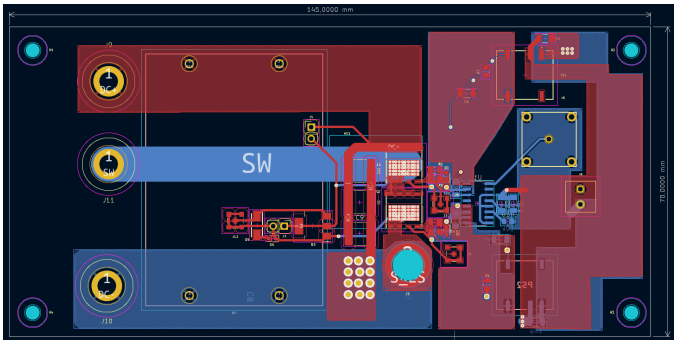


(c)

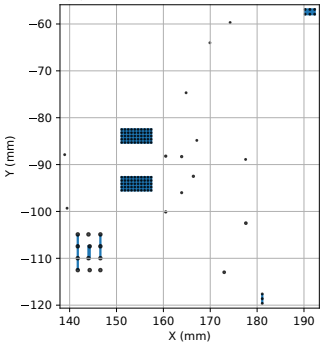
Fig. 3: A more realistic, 4 layer PCB layout with wide areas for thermal vias. This PCB was designed using Altium Designer.

TABLE I: Effect of the via simplification algorithm on the 3 designs considered.

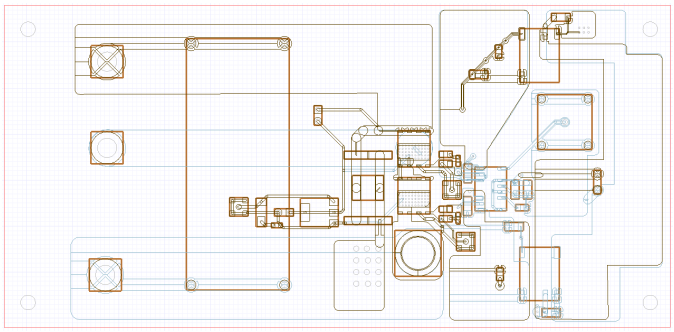
Design	# of vias in design	# of vias in clusters	# of rectangles	# of remaining standalone vias
Test Circuit (Fig 2)	480	469	22	11
Half Bridge	1286	1239	7	47
Double pulse (Fig 4)	135	118	7	17



(a)



(b)



(c)

Fig. 4: A double-pulse board, designed in KiCad, with the identification of groups of vias, and the subsequent model generation in Ansys Q3D Extractor.

consequences on the accuracy of the model, but dramatically reduces the model complexity;
- merging of nearby pads: when the distance between two pads belonging to the same copper track is too small (<1 mm), they are considered to be the same, and no circuit parasitic is computed between them.

IV. Generation of the FEM models

Once the IPC-2851 file is imported in Ansys (using HFSS-Layout, Fig. 4c), the exact same procedure as described in [10] and [11] can be followed: a 3D geometry is built, the simplifications are implemented (removing vias, faceting curves). For the calculations of the circuit parasitics, the 3D geometry is transferred to Q3D Extractor; ”sink” and ”source” terminals (the points of the circuits between which circuit parasitics must be calculated) are defined; simulations are run and an LTSpice circuit model is generated. For the thermal simulations, Ansys mechanical is used; transient thermal simulations are successively run, one per heat source being considered; a reduced-order RC model is fitted to the results and exported as an LTSpice netlist.

No loss of accuracy is observed as a consequence of the via simplification. Parasitic inductance values are difficult to validate experimentally, as they are very small (loop inductance for the circuit in Fig. 3c is below 1 nH). Parasitic capacitances are relatively large (up to 100 pF, because of the flat form factor of PCBs, but they are not affected by the representation of vias. Overall, the comparison presented in [10] shows no significant difference between electrical simulations run with a detailed geometry or its simplified version.

No detrimental effect of the via simplification can be observed on the calculations of thermal impedance either. On a single-chip test PCB (not described here), thermal resistances of 3.76 and 3.83 $\mathrm{K\,W^{-1}}$ are simulated for a full geometry and a simplified geometry, respectively, while the measured value is 3.92 $\mathrm{K\,W^{-1}}$. Both simulated values are within the measurement margin of error for such test.

V. Conclusion

This paper details the technical steps required to automatically generate FEM models of a PCB from eCAD

files. As previously demonstrated, these FEM models can then be used to generate Reduced-Order Models for circuit simulation.

Here, the contribution is to use standardized and open file formats to facilitate exchange between software suites. Systematic simplification techniques are used to keep geometry complexity manageable. The proposed solution is validated using 3 designs generated using two eCAD solutions (Altium Designer and KiCad) and three different engineers. With this relatively simple code, electrical and thermal ROMs can be generated automatically in a few minutes from eCAD data. Performing the same operations manually would require hours if not days.

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