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# A 15-GHz Reconfigurable Calibration-Free Linear FMCW Chirp Generator with Type-III Nested-PLL

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**Abstract**—A 15-GHz reconfigurable calibration-free frequency synthesizer is proposed for linear frequency-modulated continuous-wave (FMCW) chirp generation. By utilizing the type-III PLL architecture to adaptively track the ramp, the chirp linearity is improved remarkably for wide bandwidth operation. In addition, to further reduce the quantization noise from delta-sigma modulation (DSM) and suppress the in-band noise folding effect, a nested-PLL architecture is leveraged. Implemented in a 65-nm CMOS process, the proposed FMCW chirp generator consumes 55 mW power and supports triangular and sawtooth waveforms. Measurement results show that the phase noise of 15.17 GHz carrier frequency is  $-97.8$  dBc/Hz at 1 MHz offset. Without any efforts in calibration, the chirp generator achieves 1 GHz chirp bandwidth and 25  $\mu$ s chirp period with a root-mean-square (RMS) frequency error as low as 341 kHz.

**Keywords**—linear frequency-modulated continuous-wave (FMCW) chirp generation, nested-PLL, type-III architecture

## I. INTRODUCTION

Millimeter-wave (mm-Wave) FMCW radar has achieved a great success in various sensing scenarios such as 3-D imaging, autonomous-driving and biological detection [1]. As the key building block of the FMCW radar system, FMCW chirp generator plays a critical role in enabling reliable radar sensing, but its performance always presents a bottleneck in such applications.

To reduce the phase noise and extend the sweep bandwidth while improving the chirp linearity, several FMCW chirp generators have been proposed in recent years. Conventional fractional-N charge-pump phase-locked loop (CP-PLL) is widely used in the radar system [2]-[4], but it suffers from a limited chirp slope, since this architecture contains a narrow-bandwidth loop to suppress the quantization noise from the delta-sigma modulation (DSM) and in-band noise folding effect [5]. Typically, to increase chirp bandwidth, charge-pump (CP) should have a large dynamic voltage range, but it is hard to achieve high linearity and low phase noise simultaneously over the entire CP voltage range. Alternatively, digital-to-time converter (DTC) based sub-sampling PLLs (SSPLL) and two-point-modulation (TPM) technique are introduced for better linearity and phase noise performance [6]-[7]. However, the gain error of DTC and the time and gain mismatches between two modulated paths need to be calibrated by complex methods through strict procedures. Besides, the frequency acquisition range is limited and an extra FLL is necessary. With features of flexible configuration, high compatibility and scalable size, several all-digital PLL (ADPLL) based FMCWs are presented [8]-[9]. Though a high

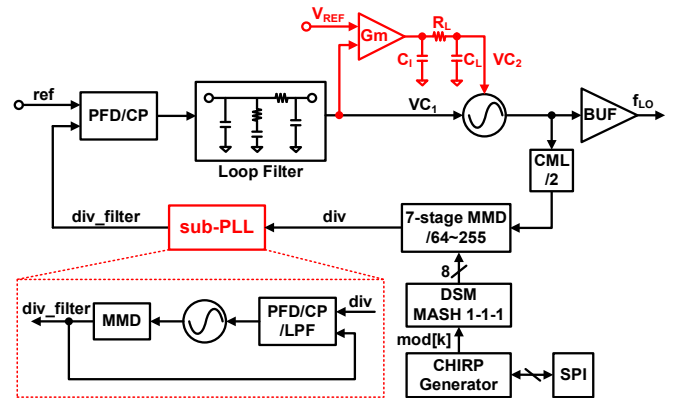


Fig. 1. Architecture of the proposed FMCW chirp generator.

chirp linearity is achieved, the performance of time-to-digital converter (TDC) and phase-interpolator (PI) are quite sensitive to the circuit parasitics, posing difficulties in the chip implementation.

This paper presents a 15-GHz reconfigurable calibration-free frequency synthesizer with wide bandwidth and high linearity. To avoid complex calibration and improve lock acquisition ability, a CP-PLL is utilized as the main structure. In the proposed PLL, a self-adaptive loop is utilized to improve the chirp linearity and a nested-PLL architecture is adopted to suppress the DSM quantization noise and in-band noise folding effect. For different applications, triangular and sawtooth chirps can be configured through the serial peripheral interface (SPI). Moreover, advantages of the proposed type-III nested-PLL are proved through simulation and measurement against the conventional CP-PLL.

## II. PROPOSED 15-GHz CALIBRATION-FREE LINEAR FMCW CHIRP GENERATOR

### A. System Architecture

Fig. 1 shows the block diagram of the proposed 15-GHz calibration-free linear FMCW chirp generator, which could be further multiplied by a quadrupler to drive a 60-GHz radar transceiver. The choice of such a low carrier frequency relaxes the VCO and frequency divider chain design. The 15 GHz VCO output is first processed by a divide-by-2 current-mode logic (CML) frequency divider and then sent to the multi-modulus frequency divider (MMD) to generate the division signal. The chirp generator is controlled by SPI to generate the  $\text{mod}[k]$  signal for the MASH 1-1-1 DSM, which modulates the MMD to obtain a targeted fractional division ratio. To further suppress the DSM quantization noise, a sub-PLL is

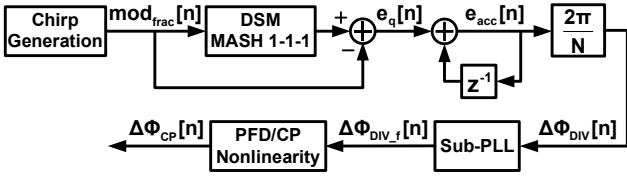


Fig. 2. Block diagram of the Simulink simulation model with PFD/CP nonlinearity in the loop.

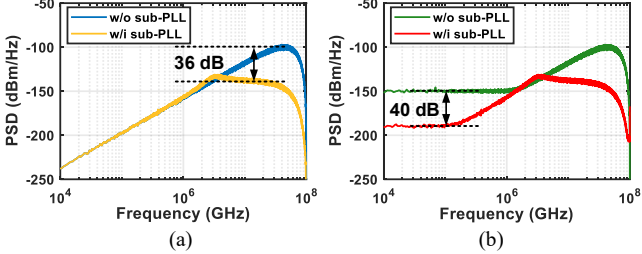


Fig. 3. Simulated PSD of the equivalent phase error at the PFD/CP output (a) when PFD/CP is linear and (b) when PFD/CP is nonlinear.

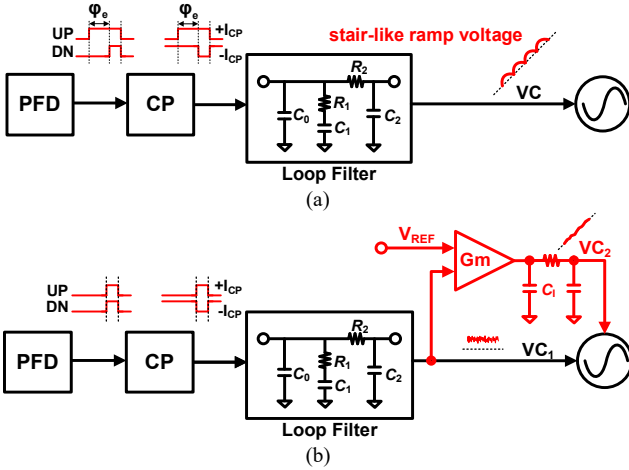


Fig. 4. Ramp generation mechanisms based on different architectures. (a) Conventional type-II architecture. (b) Proposed type-III architecture with an adaptive ramp tracking loop.

integrated to filter the division signal. For the chirp generation, in this design a type-III architecture is adopted by paralleling an additional feedback loop, thereby adaptively tracking the ramp without calibration. With the transconductance amplifier  $G_m$  and integral capacitor  $C_1$ , an  $G_m$ - $C_1$  integrator circuit is realized, and the linearity of the control voltage  $VC_2$  is improved remarkably. Furthermore, an  $R_L$ - $C_L$  low-pass filter is utilized in this  $G_m$ - $C_1$  integrator for anti-aliasing purposes.

### B. Quantization Noise and In-Band Noise Folding Effect Suppression with Sub-PLL

In order to evaluate the suppression of quantization noise and in-band noise folding effect, a Simulink simulation model is established by considering the nonlinearity effects in Fig. 2, where the quantization error  $e_q[n]$  is introduced to quantify the frequency error in the loop. With the accumulation of  $e_q[n]$ , the accumulated error  $e_{acc}[n]$  directly contributes to the PLL phase noise. As shown in Fig. 3(a), without considering the nonlinearity of PFD/CP, the power spectral density (PSD) of the equivalent phase error at the PFD/CP output is decreased by about 36 dB at  $f_{ref}/2$  offset. Furthermore, by introducing 1% mismatch between CP  $I_{UP}$  and  $I_{DN}$  current, the in-band phase noise could be further improved by 40 dB benefiting from the use of sub-PLL, as indicated in Fig. 3(b).

### C. Linearity Improvement with Adaptive Ramp Tracking of Type-III Architecture

In this design, the type-III architecture outperforms the conventional type-II architecture in aspects of adaptive ramp-tracking capability and chirp linearity. Fig. 4 demonstrates ramp generation mechanisms using Type-II and Type-III architectures for performance comparison, without considering the DSM quantization noise. As shown in Fig. 4(a), the conventional type-II architecture inevitably suffers from a fixed phase error  $\varphi_e$  when it generates the up/down sweep voltage for VCO in the chirp mode. According to [10], the phase error  $\varphi_e$  increases with the chirp slope. Furthermore, after the periodic pulsed current is injected into the low-pass loop filter (LPF), a stair-like sweep voltage will be generated for VCO tuning, causing periodic frequency error.

In contrast, the proposed type-III architecture is shown in Fig. 4(b). By shunting the  $G_m$ - $C_1$  integrator across the separated VCO control voltages, i.e.,  $VC_1$  and  $VC_2$ , an additional negative feedback loop is realized. To illustrate the working mechanism, the up ramp generation is explained below. If the output current  $I_{Gm}$  of  $G_m$  is higher than the expected value, a faster chirp slope is induced and a negative phase error  $\varphi_e$  will be detected by the PFD, thus generating a correction signal to compensate  $VC_1$  and reducing  $I_{Gm}$  through the negative feedback loop. Eventually, the phase error  $\varphi_e$  will converge to zero, and  $VC_1$  maintains a constant value, while  $VC_2$  is integrated smoothly into a steady chirp state.

## III. MEASUREMENT RESULTS

As shown in Fig. 5, the proposed FMCW chirp generator is fabricated in a 65-nm CMOS process and the chip area is about  $2.47 \text{ mm}^2$ . With 0.8 V supply voltage for VCO, 1.8 V for  $G_m$  and CP and 1.2 V for the rest circuits, the total power consumption is 55 mW.

Fig. 6 shows the measured phase noise performance in the single tone test. As indicated, the phase noise of 15.17 GHz carrier frequency is  $-97.8 \text{ dBc/Hz}$  at 1 MHz offset. The chirp

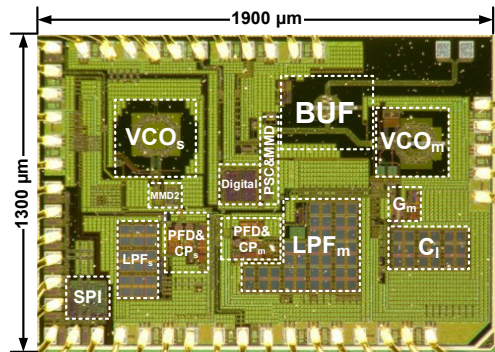


Fig. 5. Chip microphotograph of the proposed FMCW chirp generator.

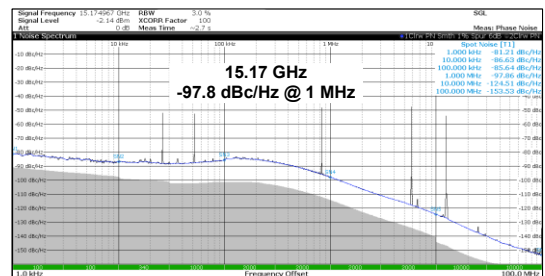


Fig. 6. Measured PLL phase noise.

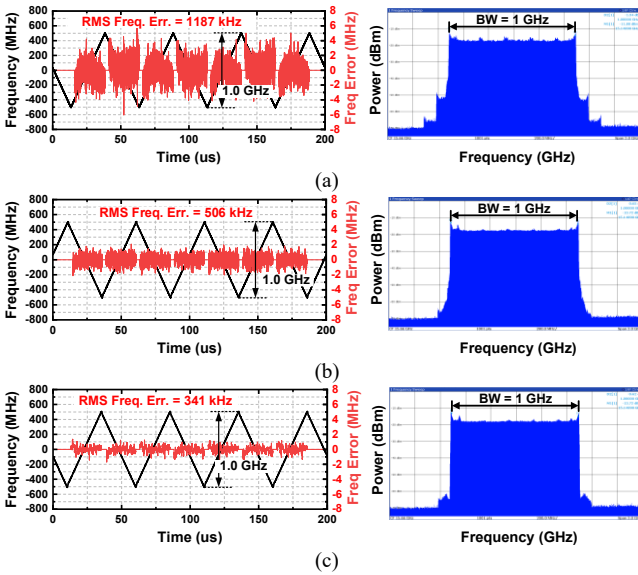


Fig. 7. Measured frequency error and spectrum of FMCW chirps with 1 GHz bandwidth and 25  $\mu$ s chirp period in different PLL architectures: (a) conventional type-II architecture; (b) type-III architecture without sub-PLL; (c) type-III architecture with sub-PLL.

signal is measured by the R&S FSW67 signal and spectrum analyzer. By configuring the PLL with different architectures to generate the same triangular chirp with 1 GHz bandwidth and 25  $\mu$ s chirp period, the measured chirp waveform, frequency error, and spectrum are compared in Fig. 7. As shown in Fig. 7(a), for the conventional type-II PLL without sub-PLL, its RMS frequency error is 1187 kHz. With the type-III architecture, the RMS frequency error could be reduced to 506 kHz in Fig. 7(b). Furthermore, as indicated in Fig. 7(c), for the proposed type-III architecture with sub-PLL, its RMS frequency error is reduced to 341 kHz. Moreover, benefiting from the type-III architecture, the reference spur over the chirp frequency range is attenuated greatly, while the fractional spur at the chirp edge is also suppressed.

TABLE I. PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART RESULTS

	This work		[9]	[2]	[11]
<b>Architecture</b>	Type III /Nested Loop		ADPLL /TPM	Analog	Type III /Mixed-Mode
<b>Process</b>	65 nm CMOS		40 nm CMOS	65 nm CMOS	65 nm CMOS
<b>Calibration</b>	NO		NO	NO	NO
<b>Freq. range [GHz]</b>	14.0-16.6		11.7-13.5	76.0-76.7	77-78.83
<b>Reference [MHz]</b>	100		100	267.6	125
<b>Phase Noise [dBc/Hz]</b>	-97.8 /-85.8*		-113.6 /-99.6*	-85.1 /-87.3*	-81.7 /-83.9*
<b>BW<sub>chirp</sub> [GHz]</b>	1.0 /4.0*		0.3 /1.5*	0.69 /0.53*	1.83 /1.43*
<b>T<sub>chirp</sub> [μs]</b>	100	25	3.85	1413	1000
<b>RMS F<sub>error</sub> [kHz]</b>	128	341	167	<73	336
<b>Chirp slope [MHz/μs]</b>	40*	160*	390*	0.38*	1.42*
<b>RMS F<sub>error</sub>/BW [%]</b>	0.012	0.034	0.056	<0.01	0.018
<b>Power [mW]</b>	55		33.8	51.3	43.1

\*Normalized to 60 GHz frequency band.

Table I summarizes the performance of the proposed FMCW chirp generator and the state-of-the-art works without calibration. As indicated, the proposed FMCW chirp generator could provide a maximum sweep bandwidth of 1 GHz, which can be further extended to 4 GHz by a quadrupler for the targeting 60 GHz band operation with a very low frequency error.

#### IV. CONCLUSION

In this paper, a 15-GHz reconfigurable calibration-free linear FMCW chirp generator with type-III nested-PLL is proposed. A type-III architecture is utilized for adaptive ramp tracking, which improves the chirp linearity greatly. A sub-PLL is employed to suppress the DSM quantization noise and the in-band noise folding effect. Fabricated in a 65-nm CMOS process, measurement results show that the proposed FMCW chirp generator supports triangular and sawtooth waveforms, and achieves 1 GHz bandwidth over 25  $\mu$ s period with a root-mean-square (RMS) frequency error as low as 341 kHz.

#### ACKNOWLEDGMENT

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