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# A 37-43.5-GHz Fully-Integrated 16-Element Phased-Array Transceiver with 64-QAM 7.2-Gb/s Data Rates Supporting Dual-Polarized MIMO

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**Abstract**—This paper presents a fully-integrated 16-element phased-array transceiver (TRX) supporting dual-polarized multi-input multi-output (DP-MIMO). Transmitting/receiving (T/R) switches are embedded for time division duplexing (TDD) operation. High linearity bi-directional variable gain amplifiers (Bi-VGA) and passive phase shifters (PS) are designed for compact area and low power consumption, respectively. Fabricated in a 65-nm CMOS process, this TRX occupies an area of 25.76 mm<sup>2</sup>. With integrated frequency synthesizer, the TRX can work from 37 to 43.5 GHz, which can fully cover 5G NR FR2 n259 and n260 bands. In the receiver (RX) mode, a noise figure (NF) of 5.4–6.3 dB and a peak conversion gain (CG) of 27.3 dB are achieved. The transmitter (TX) mode achieves a peak CG of 48.7 dB, a 13.1-dBm OP<sub>1dB</sub>, and a 15.8-dBm P<sub>sat</sub>. By using 64-QAM modulation, measurement results show that the TRX achieves a data rate up to 7.2 Gb/s per independent data stream with 7.65 dBm output power per channel.

**Index Terms**—5G, CMOS, dual-polarization multi-input multi-output (DP-MIMO), frequency synthesizer, millimeter wave (mm-Wave), phased-array, quadrature amplitude modulation (QAM), transceiver (TRX).

## I. INTRODUCTION

FOR the increasing demand in high data throughput for emerging applications, e.g., augmented reality (AR), virtual reality (VR), mixed reality (MR), etc., several mm-Wave bands including 37–43.5-GHz (n259 and n260)

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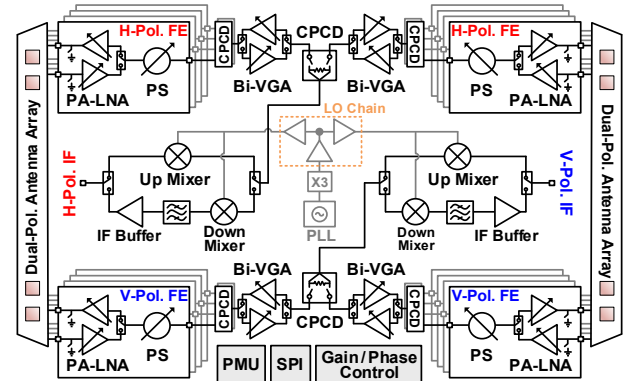


Fig. 1. The proposed dual-polarization phased-array transceiver architecture.

have been allocated in the 5G new radio (NR) frequency range 2 (FR2). To compensate the large propagation loss and to accommodate spatial mobility for the mm-Wave communication, the phased-array technique is urgently required [1]–[3]. In addition to improving the noise figure (NF), linearity, and power efficiency of transmitting/receiving (T/R) elements, the system data throughput could be significantly extended with the dual-polarization multi-input multi-output (DP-MIMO) technique. Recent works prove the feasibility in integrating high data-rate dual-polarized phased-array transceiver chips without scaling up the physical size of the antenna array [4]–[9]. Nevertheless, due to the increasing demands for the miniaturized smart user equipment (UE), it poses more challenges in designing a compact and fully-integrated phased-array transceiver that incorporates more elements while balancing the overall performance and packaging difficulties [10].

To this end, a fully-integrated 16-element phased-array transceiver (TRX) supporting DP-MIMO with compact architecture is proposed in this work, which integrates RF front-end (FE), frequency converter, and frequency synthesizer. Specifically, bi-directional variable gain amplifier (Bi-VGA) is designed to drive multiple T/R elements, reducing the required number of active stages in the TRX. The passive phase shifter (PS) is adopted to reduce the power consumption as well as the T/R element area due to its bi-directional feature. Fabricated in a 65-nm CMOS process, the

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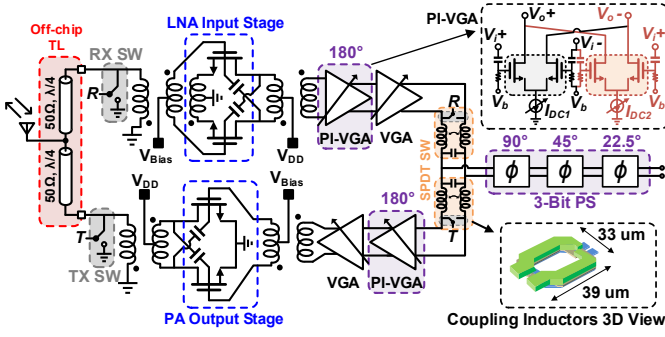


Fig. 2. Structure of the T/R element.

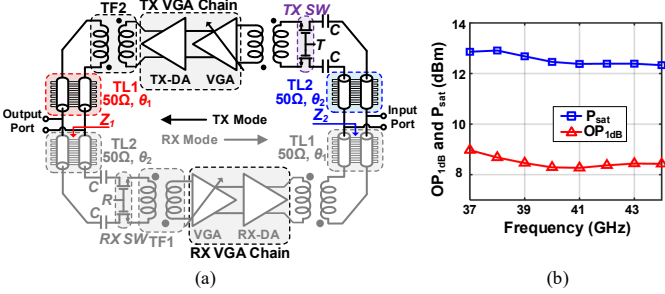


Fig. 3. (a) Structure of the high linearity Bi-VGA. (b) Simulated TX Mode Bi-VGA  $OP_{1dB}$  and  $P_{sat}$  at 37-43.5 GHz.

proposed fully-integrated 16-element TRX achieves a data rate of 7.2 Gb/s per independent data stream in 64-QAM with a 7.65 dBm output power per channel, while occupying a chip area of 25.76 mm<sup>2</sup>.

## II. TRANSCIVER ARCHITECTURE AND BUILDING BLOCKS

### A. Transceiver Architecture

The architecture of the proposed phased-array TRX is depicted in Fig. 1, which comprises 16 T/R elements (8H + 8V) to support the DP-MIMO. In each T/R element, benefitting from the 1-bit 180° phase-inverting (PI) feature implemented in both the low noise amplifier (LNA) and power amplifier (PA), a 4-bit 360° phase control could be realized by merely integrating a 3-bit 180° passive PS. In this way, the size and insertion loss (IL) of the PS are reduced significantly.

The configurable power combiners and dividers (CPCDs) are adopted to support sub-array operations and to expand the TRX dynamic range while maintaining the system power efficiency. High linearity Bi-VGA is adopted to drive four T/R elements and compensate for the significant losses caused by passive components, such as PS, CPCDs, and transmission lines (TLs). Benefiting from the compact Bi-VGA and T/R element, the entire chip size could be significantly reduced. In addition, the local-oscillator (LO) signal is provided by the integrated phase-locked loop (PLL) and frequency tripler. Peripheral circuits, i.e., serial peripheral interface (SPI) and power management unit (PMU), are integrated to support the phased-array applications.

### B. Compact T/R Element

The structure of the compact T/R element is shown in Fig. 2. On the antenna side, the T/R switches are co-designed with off-

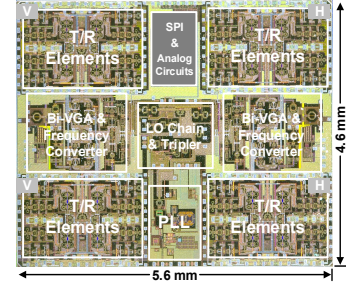


Fig. 4. Chip micrograph of the fully-integrated dual-polarization phased-array transceiver with PLL.

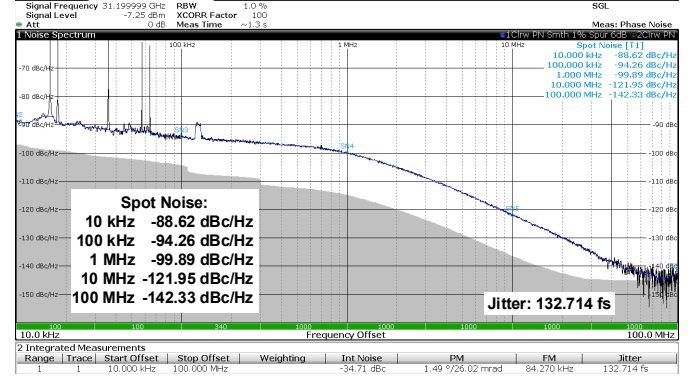


Fig. 5. Measured LO phase noise at 31.2 GHz.

chip 50-Ω  $\lambda/4$  TLs, which are integrated into the packaging to reduce chip area. Meanwhile, to minimize the side-effect of the T/R switches on the element performance, the receiver (RX) switch is designed for low IL performance by using small-sized transistors with lower parasitics, while the stacked transistors are used in the transmitter (TX) switch for high linearity performance. On the other side of the T/R element, a single-pole double-throw (SPDT) switch is integrated with an ultra-compact  $\pi$ -type LC network, which only occupies a core area of 39 $\mu\text{m}$ ×33 $\mu\text{m}$ , as shown in Fig. 2.

To reduce PS units for low IL and chip area, the 1-bit 180° phase-inverting variable gain amplifier (PI-VGA) is used. Such PI-VGA contains double balanced common-source (CS) amplifier with tail current sources  $I_{DC1}$  and  $I_{DC2}$ , which are digitally controlled for gain tuning to compensate for the PS IL variation between different phase states. The PI-VGA output phase can be reversed by 180° by swapping the current of  $I_{DC1}$  and  $I_{DC2}$ , while maintaining the same gain level. By combining the 1-bit 180° PI-VGA and a 3-bit 180° PS, 4-bit 360° phase control is achieved. Note that, the 3-bit 180° PS is realized with phase steps of 22.5°, 45°, and 90°, respectively, and it has a typical cascaded 7 dB IL.

### C. High Linearity Bi-VGA

Fig. 3(a) depicts the Bi-VGA structure, which contains two identical VGA chains reversely connected in parallel. In each VGA chain, a driver amplifier (DA) is integrated in the VGA output to improve its linearity performance, and four T/R elements could be driven simultaneously for the compact TRX architecture. At each VGA chain input, an asymmetric SPDT switch is implemented with low IL features. Meanwhile, 50-Ω

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TABLE I. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART CMOS PHASED-ARRAY TRANSCIEVERS.

		This Work	TMTT'23 [3]	RFIC'19 [8]	ISSCC'20 [9]	JSSC'20 [11]
Technology		65-nm CMOS	65-nm CMOS	28-nm CMOS	28-nm CMOS	65-nm CMOS
Integration		Dual Pol. 16ch. TRX w/ PLL	4ch. FE w/o PLL	Dual Pol. 8ch. FE w/o PLL	16ch. TRX w/o PLL	4ch. TRX w/o PLL
T/R Switch		Yes (w/ off-chip TMs)	Yes (On-chip)	Yes (On-chip)	No	Yes (On-chip)
Carrier Frequency (GHz)		37-43.5	33.5-37.5	37-40	37-40	39
Phase Resolution (bits)		4	6	5	4	13
RX	Peak Gain (dB)	27.3	26	41.9	59	3
	NF/ch (dB)	5.4-6.3	4.2-10.7	6-7.6	4.2-4.6	7.7
	IP <sub>1dB</sub> /ch (dBm)	-26.5	N/A	-44	-44 <sup>#</sup>	-22
	P <sub>DC</sub> /ch. (mW)	69.7 <sup>§</sup>	164	78.5	39	500 (4RX)
TX	Peak Gain (dB)	48.7	44	48	60	7
	OP <sub>1dB</sub> /ch. (dBm)	13.1	17.2	12.3	15.3	9
	P <sub>sat</sub> /ch. (dBm)	15.7	19.8	N/A	16.5	15.5
	P <sub>DC</sub> /ch. (mW)	210@P <sub>1dB</sub> <sup>§</sup>	496	339@P <sub>1dB</sub>	105/115 <sup>§</sup>	1500 (4TX)
Modulation Results		64-QAM, 3.6/7.2 Gb/s 10.6/7.65 dBm P <sub>out</sub> /ch -25.2/-25.54 dB EVM -29.43/-30.38 dBc ACLR	16-QAM, 0.8 Gb/s 11.2 dBm P <sub>out</sub> /ch -29.7 dB EVM	64-QAM OFDM 0.6 Gb/s -32.57 dB EVM	64-QAM OFDM 4.8 Gb/s 6/8.8 dBm P <sub>out</sub> /ch -34/-27 dB EVM	8TX 8RX OTA 64-QAM, 2.4 Gb/s -30.2 dB EVM
		256-QAM, 1.6 Gb/s 6.9 dBm P <sub>out</sub> /ch -30.12 dB EVM -35.8 dBc ACLR	64-QAM, 1.2 Gb/s 11.2 dBm P <sub>out</sub> /ch -30.4 dB EVM	64-QAM OFDM 4.8 Gb/s -26.5 dB EVM <sup>#</sup>		8TX 8RX OTA 256-QAM, 3.2 Gb/s -30 dB EVM
Chip Area (mm <sup>2</sup> )		25.76	25.92	17.25	30	12

<sup>§</sup>Including T/R element, Bi-VGA, up (or down) Mixer, and LO buffer. <sup>#</sup>Estimated from figures. <sup>§</sup>With 6/8.8 dBm P<sub>out</sub>/ch.

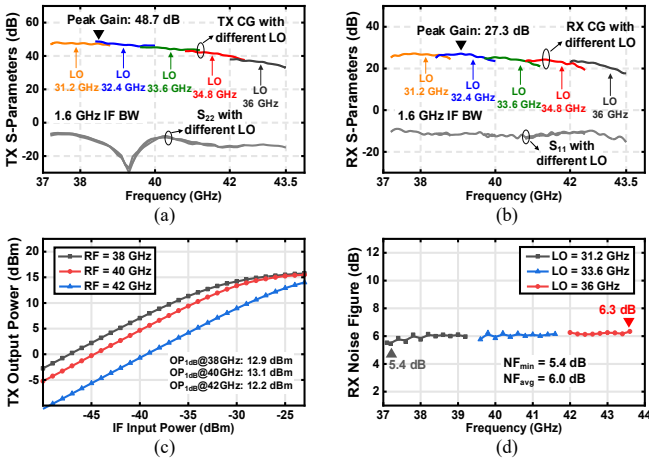


Fig. 6. Measured (a) TX and (b) RX S-Parameters. (c) Measured OP<sub>1dB</sub> of the full TX path. (d) Measured NF of the full RX path.

differential TL1 and TL2 are designed with different electrical length for the impedance matching as well as port isolation purposes in both TX and RX modes. Taking the TX mode as an example, the TX SW is turned on while RX SW are off. Meanwhile, the RX VGA chain is powered off, and with the impedance matching network, its input and output impedances, i.e.,  $Z_1$  and  $Z_2$ , respectively, are transformed to higher values, introducing only 0.74 and 0.93 dB simulated ILs at the Bi-VGA input and output, respectively. To illustrate the linearity performance of the Bi-VGA, the simulated OP<sub>1dB</sub> and P<sub>sat</sub> of Bi-VGA in the TX mode are shown in Fig. 3(b).

### III. MEASUREMENT RESULTS

Fabricated in a 65-nm CMOS process, the proposed phased-array TRX occupies a total area of  $5.6 \times 4.6$  mm<sup>2</sup>, as shown in Fig. 5. The T/R element and Bi-VGA occupy 0.55 and 0.22

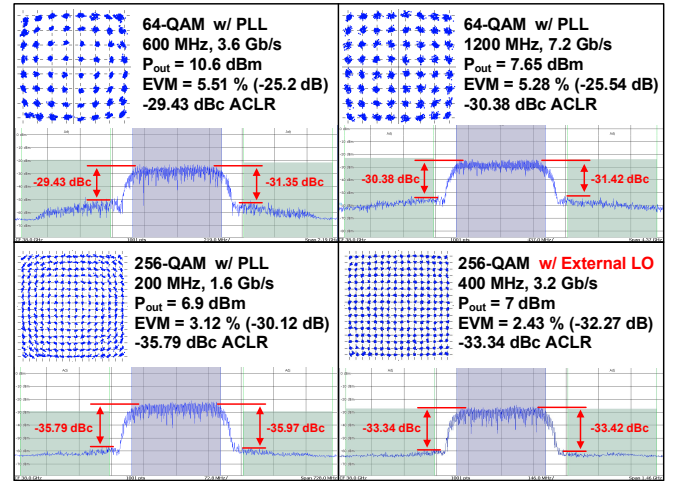


Fig. 7. Measures 64-/256-QAM EVM and ACLR at 38 GHz.

mm<sup>2</sup>, respectively. All measurements were conducted with the on-chip PLL.

As shown in Fig. 5, with a 10.4 GHz LO from the PLL, the measured phase noise (PN) of the 31.2 GHz LO after the frequency tripler achieves -99.89 and -121.95 dBc/Hz PN at 1 MHz and 10 MHz offsets, respectively. With an intermediate frequency (IF) ranging from 6 to 7.6 GHz, the measured TX and RX conversion gains in five sub-bands of the 5G NR FR2 37-43.5 GHz bands are shown in Fig. 6(a) and (b), respectively. Peak conversion gains of 48.7 and 27.3 dB are achieved in the TX and RX modes, respectively. The TX output power from 38 to 42 GHz is shown in Fig. 6(c), where an OP<sub>1dB</sub> from 12.2 to 13.1 dBm is achieved, respectively. The measured RX NF over the desired frequency band is shown in Fig. 6(d), achieving a NF from 5.4 to 6.3 dB and demonstrating a good NF performance over the interested frequency range.

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To further evaluate the TX performance, the modulation measurements are performed. Fig. 7 presents the measured constellations and ACLR results of 64-/256-QAM signal at 38 GHz. As indicated, with 600-/1200-MHz 64-QAM modulation, a  $P_{\text{out}}$  of 10.6/7.65 dBm is achieved with -25.2/-25.54 dB error vector magnitude (EVM), respectively, which is mainly limited by TX linearity and noise performance. It achieves a  $P_{\text{out}}$  of 6.9 dBm for 200-MHz 256-QAM with -30.12 dB EVM, which is mainly limited by the LO PN. Besides, with an external LO signal, it achieves a  $P_{\text{out}}$  of 7 dBm for 400-MHz 256-QAM with -32.27 dB EVM.

Table I compares the performance of the proposed phased-array TRX with the state-of-the-art phased array transceiver results. As indicated, this work integrates PLL and can fully cover the 5G NR FR2 37-43.5 GHz n259 and n260 bands, while achieving lower power consumption and a more compact area. Benefiting from the excellent bandwidth, NF and linearity performance, this work achieves the fastest data rate up to 7.2 Gb/s.

#### IV. CONCLUSION

This paper presents a fully-integrated 16-elements phased-array TRX supporting DP-MIMO with a compact system architecture. Fabricated in a 65-nm CMOS process, the proposed phased-array TRX occupies a total chip area of 25.76 mm<sup>2</sup>. The measured TRX can fully cover the 5G NR FR2 37-43.5 GHz n259 and n260 bands with a 1.6 GHz IF bandwidth in each sub-channel. Consuming an average 210 mW power consumption per channel, the TRX achieves the  $OP_{\text{1dB}}$  and  $P_{\text{sat}}$  of 13.1 and 15.8 dBm, respectively, and supports 1200-MHz 64-QAM and 200-MHz 256-QAM with high output power. Furthermore, the proposed TRX achieves a data rate up to 7.2 Gb/s per independent data stream, which is very suitable for high-throughput and small-scale 5G UE applications.

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