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# A 60-GHz Highly-Reused Joint Radar-Communication Transceiver with Reconfigurable Dual-Mode Gilbert Cells in 65-nm CMOS

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Abstract—A 60-GHz joint radar-communication (JRC) transceiver is introduced in this paper. Benefiting from a reconfigurable dual-mode Gilbert cell which could not only operate as an up-conversion mixer for the baseband signal but could also be configured as an amplifier for the LO signal, a highly-reused JRC transceiver architecture is realized. In the radar mode, instead of utilizing the narrow-band IF chirp modulation scheme which is widely adopted in previous JRC systems, in this work a wideband chirp generated directly from the LO chain could be applied for both transmitting and direct RF de-chirping, thereby significantly improving the range resolution and relieving the hardware burden in radar signal processing. Fabricated in a 65-nm CMOS process, this work achieves a 16-dBm saturated TX output power, an 11-dBm OP<sub>1dB</sub>, and a 5.8-dB minimum RX noise figure (NF). Experiments demonstrate that the proposed JRC transceiver supports >7 Gb/s data rate in the 16-QAM over-the-air (OTA) communication, as well as >4 GHz transmitted chirp bandwidth with <3.75 cm range resolution in the radar mode.

*Index Terms*—Dual-mode, Gilbert cell, highly-reused, joint radar-communication (JRC), transceiver.

#### I. INTRODUCTION

As the most important applications of modern radio frequency technologies, the radar and communication systems are complementary in functionalities [1], [2], [3]. For example, the radar system could assist the communication system to realize rapid beam alignment. On the other hand, the communication system is essential for collaborative radar networks to achieve rapid fusion of the detection data. As a result, studies on joint radar communication (JRC) systems

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have become a hot research topic, especially in the era towards 6G.

Recently, several integrated JRC systems have been reported. In [4], a 28-nm D-band JRC transceiver is presented by utilizing mode multiplexers to switch different signal paths for the radar and communication modes, respectively. As few circuit modules are reused in both operating modes, the chip area is relatively large. In [5] and [6], a Ka-band 4TX/4RX phased-array JRC transceiver and an E-band JRC transmitter are presented, respectively. In these works, the JRC functionality is realized by injecting either the quadrature chirp signals or the communication data at the TX IF input. Although more circuit blocks are reused in [5] and [6], their achievable chirp bandwidths are restricted to 0.5 and 1 GHz, respectively, which are limited by the external IF devices bandwidth and induce relatively low range resolutions in the radar mode. Besides, the IF chirp modulation schemes would increase the hardware burden for the radar signal processing due to the utilized off-chip digital de-chirping.

In this paper, to tackle the aforementioned issues, a 60-GHz JRC transceiver with a reconfigurable dual-mode Gilbert cell is proposed. For communication purposes, the dual-mode Gilbert cell functions as a double-balanced up-conversion mixer. While in the radar mode, the Gilbert cell could be further configured as a neutralized common-source (CS) amplifier for the LO signal, and thus the chirp signal generated from the LO chain could be directly transmitted through the Gilbert cell for radar sensing purposes. By utilizing an on-chip frequency quadrupler in the LO chain, the chirp bandwidth could be further extended for a higher range resolution. Besides, different from the IF chirp modulation scheme that requires digital de-chirping for the radar signal processing, the direct RF de-chirping utilized in this work significantly relieves the hardware burden in the radar mode. Accordingly, benefiting from the proposed reconfigurable dual-mode Gilbert cells, an efficient and highly-reused JRC transceiver is realized. Fabricated in a 65-nm CMOS process, the proposed JRC transceiver achieves a saturated TX output power of 16 dBm with an OP<sub>1dB</sub> of 11 dBm. The measured LO feedthrough (LOFT) suppression is better than 46 dBc under OP<sub>1dB</sub>, and a 5.8-dB RX noise figure (NF) is achieved. Experiments demonstrate that the proposed JRC transceiver supports >7 Gb/s data rate in the 16-QAM over-the-air (OTA) communication, and in the radar mode, a <3.75 cm range resolution could be realized with >4 GHz chirp bandwidth.



Fig. 1. Block diagram of the proposed 60-GHz joint radar-communication system.



Fig. 2. Dual-mode Gilbert cell. (a) Up-mixer mode for the communication applications. (b) Neutralized CS amplifier mode for the radar applications.

#### II. TRANSCEIVER ARCHITECTURE

The detailed block diagram of the proposed JRC system with a quadrature homodyne architecture is shown in Fig. 1. In the LO chain, a frequency quadrupler is integrated to convert the 15-GHz single-tone and FMCW chirp signals to drive the JRC transceiver in the communication and radar modes, respectively. After that, a configurable T/R switch is introduced, which could function as a single-pole doublethrow (SPDT) switch for the time division duplex (TDD) communication, and could also be configured as a power splitter in the radar mode. Wideband I/Q hybrid couplers are used to generate the 60-GHz quadrature LO signals in both operating modes. In the TX, the proposed dual-mode Gilbert cells could work as the double-balanced up-conversion mixers to modulate the baseband data for the communication applications, and could also be configured as the neutralized CS amplifiers to strengthen the quadrature LO chirp signals, which are then synthesized at the PA input for the radar sensing applications. In the RX, tunable low-pass filters (LPF) are placed ahead of the IF variable gain amplifiers (VGA). In order to support high data-rate communication applications, the LPF could be configured with GHz-level bandwidth, whereas to suppress the out-of-range interferences in the radar sensing mode, a 10-MHz cut-off frequency is adopted.

#### III. RECONFIGURABLE DUAL-MODE GILBERT CELL

The detailed structure of the proposed reconfigurable dualmode Gilbert cell is illustrated in Fig. 2(a) and (b). In the communication mode, the Gilbert cell serves as a standard double-balanced up-conversion mixer. In order to eliminate the LO feedthrough (LOFT) caused by undesired device mismatches, 5-bit current DACs at the  $g_m$  stage are adopted to compensate for the DC offsets. In the radar mode as shown in Fig. 2(b), one side of the  $g_m$  stage (M6) in the Gilbert cell is turned off by biasing the gate to the ground, and the other



Fig. 3. (a) Simplified schematic of the proposed reconfigurable Gilbert cell in the neutralized CS amplifier mode. (b) Simulated  $K_f$  and  $G_{max}$ .



Fig. 4. (a) Schematic of the quadrature dual-mode Gilbert cells and I/Q hybrid coupler. (b) Simulated power gains in different operating modes.



Fig. 5. Chip micrograph of the proposed 60-GHz JRC transceiver in 65-nm CMOS.

transistor M5 functions as a tail current source. As a result, the Gilbert cell turns into a CS amplifier, and the parasitic capacitance Cgd of M3 and M4 works as neutralization capacitors, as illustrated by the simplified schematic in Fig. 3(a). The simulated  $G_{max}$  and stability factor  $K_f$  of the neutralized CS amplifier are shown in Fig. 3(b), demonstrating a considerable power gain with unconditional stability over a wide frequency range. In contrast, without M3 and M4 for neutralization, the  $K_f$  would be lower than 1 over the entire presented bandwidth. The schematic of the quadrature dualmode Gilbert cells with a compact I/Q hybrid coupler is shown in Fig. 4(a), and the corresponding power gains in different operating modes are shown in Fig. 4(b). Note that the exhibited power gain in the CS amplifier mode includes the insertion loss of the hybrid coupler, the transmission lines (TL), and the transformer-based broadband matching networks. Besides, the quadrature combination of the LO signals would also introduce about 3-dB power loss compared with the inphase combination. Nevertheless, benefiting from the sufficient gain budget of the LO and TX blocks, the PA could still achieve the targeted output power.

#### IV. EXPERIMENTAL RESULTS

The chip micrograph of the proposed 60-GHz JRC transceiver is shown in Fig. 5. Fabricated in a 65-nm CMOS



Fig. 6. (a) Measured saturated TX output power in the radar mode. (b) Measured TX gain in the communication mode.



Fig. 7. (a) Measured variable RX gain with a fixed 10-MHz IF output. (b) Measured maximum RX gain and minimum NF in the communication mode.



Fig. 8. TX spectrum measurements in the communication mode with a fixed 60.48-GHz LO. (a) LOFT and IRR performance with 1-GHz quadrature IF signal; (b) 1.76-Gsym/s 16-QAM modulated signal.

process, the chip occupies an area of  $2.65 \times 1.19 \text{ mm}^2$ . As shown in Fig. 6, in the radar mode, the measured saturated TX output power is about 16 dBm with a 3-dB bandwidth of 16.8 GHz. In the communication mode, the measured TX gain exceeds 29 dB from 55 to 66 GHz, fully covering the four channels (CH<sub>1-4</sub>) defined in the IEEE 802.15.3c standard [7]. An OP<sub>1dB</sub> exceeding 11 dBm is also achieved across these channels. As shown in Fig. 7(a), the measured variable RX gain ranges from 20 to 75 dB with a 3-dB bandwidth from 54 to 65 GHz. In the communication mode, a minimum NF of 5.8 dB is achieved in CH<sub>2</sub> under the maximum RX gain, as shown in Fig. 7(b).

As shown in Fig. 8(a), with a 60.48-GHz LO and 1-GHz quadrature IF input, the measured image rejection ratio (IRR) is 31.5 dB, and the LOFT is as low as -46.3 dBc benefitting from the LOFT calibration. Furthermore, with 1.76-Gsym/s 16-QAM baseband signal provided by the Tektronix AWG70002A arbitrary waveform generator, the TX spectrum was measured by the R&S FSW67 signal and spectrum analyzer, as shown in Fig. 8(b). With a 6.5-dBm average power, the measured TX constellation exhibits an EVM of -26.4 dB. With two probe stations, the OTA communication measurements between two JRC transceivers are implemented. The experiment setup for the OTA communication is shown in Fig. 9. Note that each transceiver was connected with the 20-dBi horn antennas through probes and coaxial cables with a total length of about 7 m. Due to the huge 42-dB loss of the



Fig. 9. Experiment setup for the OTA communication between two probe stations. (a) Detailed equipment setups. (b) Scenario photograph.



Fig. 10. (a) Measured constellations of the TX-to-RX OTA communication under 1.76-Gsym/s QPSK and 16-QAM modulations. (b) Measured spectrum of the TX chirp with a 4-GHz bandwidth in the radar mode.



Fig. 11. (a) Experiment setup for the radar detection with two human targets moving back and forth in opposite directions in front of the radar system. (b) Detected range map.

coaxial cables, the communication range between the TX and RX antennas was set to 20 cm. With 1.76-Gsym/s QPSK and 16-QAM modulations, the measured constellations of the OTA communications are shown in Fig. 10(a), and the measured EVMs are -21.6 and -20.5 dB, respectively.

For the radar mode test, a 15-GHz chirp signal with 1-GHz bandwidth generated by the R&S SMW200A vector signal generator was injected into the frequency quadrupler, and the measured TX output spectrum is shown in Fig. 10(b). Owing to the 4-GHz TX chirp bandwidth, a theoretical 3.75-cm range resolution could be achieved. As shown in Fig. 11(a), a single JRC transceiver was connected with two horn antennas for the chirp transmitting and receiving, and two human targets were asked to move back and forth in opposite directions in front of the radar system. With a 125-Hz chirp repetition rate, the IF signals of each TRX chirp frame are processed by the fast Fourier transform, and the resultant spectrums could be further

 TABLE I

 PERFORMANCE COMPARISON OF STATE-OF-THE-ART JRC SYSTEMS

| Ref.                         | JSSC<br>2022 [4]             | RFIC<br>2022 [5]             | RFIC<br>2022 [6]    | This Work                    |
|------------------------------|------------------------------|------------------------------|---------------------|------------------------------|
| Process                      | 28nm CMOS                    | 65nm CMOS                    | 40nm CMOS           | 65nm CMOS                    |
| Freq. (GHz)                  | 150                          | 33                           | 79                  | 60                           |
| TX Gain (dB)                 | 30~44                        | 22.2                         | 12                  | 29                           |
| TX P <sub>sat</sub> (dBm)    | 13                           | 19.9                         | 12.4                | 16                           |
| TX OP <sub>1dB</sub> (dBm)   | 8.3                          | 17.4                         | 9.8                 | 11                           |
| RX Gain (dB)                 | Radar: 17~108<br>Comm.: 5~70 | 34.7                         | -                   | 20~75                        |
| $RXNF_{min}(dB)$             | Radar: 15<br>Comm.: 11       | 4.8                          | -                   | 5.8                          |
| OTA EVM (dB)<br>&            | -16.5<br>QPSK 12G<br>-19.7   | -26.5<br>16QAM 1.6G<br>-27.2 | -17.79<br>16QAM 24G | -21.6<br>QPSK 3.52G<br>-20.5 |
| Data Kate (bps)              | 16QAM 10G                    | 64QAM 2.4G                   | (Only TX)           | 16QAM 7.04G                  |
| Channel Num.                 | 1                            | 4                            | 1 (only TX)         | 1                            |
| Chip Area (mm <sup>2</sup> ) | 9.17                         | 14.16                        | 1.42 (only TX)      | 3.15                         |
| Power (mW)                   | Radar: 969<br>Comm.:1177     | 594/Ch                       | 189 (only TX)       | Radar: 490<br>Comm.: 510     |
| TX Chirp<br>Bandwidth (GHz)  | 12                           | 0.5                          | 1                   | 4                            |
| Range<br>Resolution (cm)     | 1.25                         | 30                           | 15                  | 3.75                         |

converted to the 1-D range profiles by transforming the frequency  $f_{IF}$  to the real distance D according to

$$D = f_{IF} \cdot c / (2 \cdot S), \qquad (1)$$

where c is the light speed, and S is the chirp slope. By stacking all the 1-D range profiles along the slow-time direction, the 2-D range map could be constructed as shown in Fig. 11(b), demonstrating explicit tracking trajectories of both targets.

The performance comparisons with the state-of-the-art JRC systems are summarized in Table I. Benefiting from the highly-reused transceiver architecture with the proposed reconfigurable dual-mode Gilbert cells, a compact chip size and low power consumption are exhibited. In addition, competitive performances in both the communication and radar modes are also achieved.

#### V. CONCLUSION

This paper presents a 60-GHz highly hardware-reused JRC transceiver with reconfigurable dual-mode Gilbert cells. Fabricated in a 65-nm CMOS process, this work occupies a compact chip area of 3.15 mm<sup>2</sup> and consumes a DC power of 490 and 510 mW in the radar and communication modes, respectively. A >4 GHz transmitted chirp bandwidth with <3.75 cm range resolution and >7 Gb/s 16-QAM OTA communication are also demonstrated.

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