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A Ka-Band Frequency Doubler With a Broadband Matching Scheme for Efficiency Optimization

Lin Lu, *Graduate Student Member, IEEE*, Xujun Ma, *Member, IEEE*, Jing Feng, Qin Chen, Depeng Cheng, Xiangning Fan, *Member, IEEE*, Xu Wu, *Member, IEEE*, and Lianming Li, *Member, IEEE*

Abstract—Caused by inappropriate allocation of the interstage power mismatches during broadband matching, the boosted dynamic DC current of the frequency doubler (FD) would deteriorate the broadband efficiency. To tackle this issue, an efficiency-optimized broadband matching strategy is proposed by allocating all of the desired low-frequency mismatches ahead of the push-push (PP) pair, which not only keeps a broadband output but also reduces the dynamic DC current and improves the efficiency over the entire operating bandwidth simultaneously. To further enhance the 2nd harmonic (HR2) output power, a 4th-order notch filter is also designed at the PP pair input. Fabricated in a 65-nm CMOS process, the proposed Ka-band FD exhibits >15% efficiency from 24.6 to 36 GHz, and a 23.5% peak efficiency is achieved. A 42.6% fractional bandwidth is also realized with a fundamental rejection ratio over 45 dBc.

Index Terms—Broadband matching, efficiency optimization, frequency doubler (FD), notch filter, push-push (PP) pair.

I. INTRODUCTION

THE growth in high-speed communications and high-resolution radars draws tremendous demands on high-frequency signal sources. As the operating frequency increases, a fundamental voltage-controlled oscillator (VCO) could hardly meet the system requirements on low phase noise (PN) and wide frequency tuning range. To solve these issues, a frequency multiplier driven by a low-frequency VCO would be a much more effective solution [1]-[4].

To design a frequency doubler (FD) with high efficiency, wide bandwidth, and high conversion gain (CG), various techniques have been proposed. In [5], based on a 0.13- μm SiGe technology, an FD with a compact four-way transformer (TF) and common-centroid cascode pairs is proposed for efficient power combining and fundamental rejection ratio (FRR) improvement. Although a 46.2% fractional bandwidth (FBW) from 25 to 40 GHz is achieved with an outstanding peak efficiency of 22.9%, the FBW with >15% efficiency shrinks dramatically to 23.5% (30-38 GHz). In [6], a 28-nm CMOS-based FD with a 2nd harmonic (HR2) feedback technique is proposed. This work achieves 5 dBm output power, 28.5% FBW, and 10.2% peak efficiency. However, the

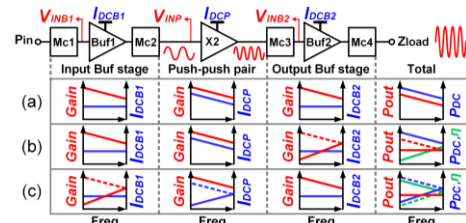


Fig. 1. Topology of the proposed FD and performance comparison of different matching schemes.

minimum efficiency within the concerned bandwidth is merely 3.6% and the required input power is as high as 8 dBm. In [7], a 65-nm CMOS-based FD with a Gm-boosting output buffer is proposed. A 5.7-dBm saturated output power and a 19.5% peak efficiency are achieved within 35.4% FBW, whereas the minimum in-band efficiency is only 10% and the required input power is still as high as 7 dBm. These works typically achieve considerable peak efficiency, whereas the broadband efficiency optimization within the entire operating bandwidth is rarely considered. Moreover, considering practical system integration, it is essential to involve additional buffers to drive the FD and boost the output power. For such a multi-stage FD, an efficiency-optimized technique within the entire operating bandwidth is urgently required.

In this letter, a Ka-band FD based on the push-push (PP) architecture is proposed. Neutralized CS buffers are applied at the input and output stages which depicts a general cascaded case in system integration. An efficiency-optimized broadband matching scheme is proposed by quantifying and allocating specific power mismatches ahead of the PP pair. To further enhance the output HR2 and improve the total efficiency, a 4th-order notch filter is also designed. Based on the proposed techniques, an outstanding efficiency over 15% is achieved from 24.6 to 36 GHz with a peak value of 23.5%. Competitive FBW of 42.6% and FRR over 45 dBc are also demonstrated.

II. BROADBAND MATCHING SCHEME FOR EFFICIENCY OPTIMIZATION

The topology of the proposed FD consists of three stages as shown in Fig. 1. The first stage contains the input buffer as well as the matching networks $Mc1$ and $Mc2$. The second stage contains the PP pair, and the last stage contains the output buffer as well as the matching networks $Mc3$ and $Mc4$. V_{INB1} , V_{INP} , and V_{INB2} are the input voltage swings of the input buffer, the PP pair, and the output buffer, respectively. To indicate the impact of different matching schemes on bandwidth and efficiency, three typical matching schemes are compared in Fig. 1. With a constant input power P_{in} , the power gains and the dynamic DC currents of each stage, as well as the total output power, DC consumption, and

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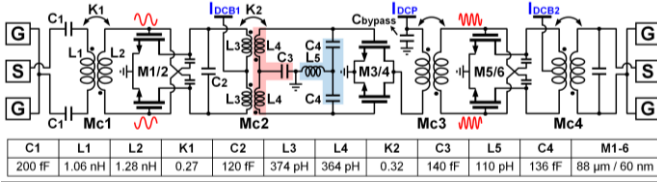


Fig. 2. Schematic of the proposed FD and key parameters.

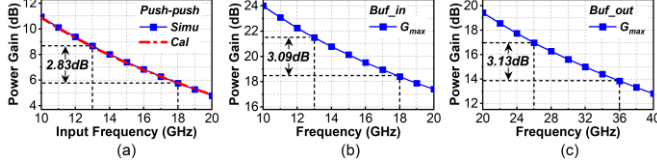


Fig. 3. Power gain degradation of the PP pair as well as buffers.

efficiency, are also presented. To simplify the analysis, the matching networks are assumed to be lossless.

In the first matching scheme for the maximum power transmission as shown in Fig.1 (a), the total output power would roll off with increasing frequency due to the decreased transistor power gain, thus causing a narrow bandwidth. Given that the buffers are biased in class-A mode and the PP pair is biased around V_{th} to boost the HR2, the DC currents I_{DCB1} and I_{DCB2} remain almost constant with varied V_{INB1} and V_{INB2} , whereas I_{DCP} is proportional to V_{INP} [8]. As indicated in Fig. 1(a), the input power of the PP pair decreases with increasing frequency, and thus I_{DCP} as well as the total DC consumption P_{DC} would also exhibit a decreasing trend.

To realize a broadband output power, dedicated mismatches should be introduced to suppress the abundant power gain in the lower frequency band. As shown in Fig. 1(b), by allocating the required mismatches to the output buffer stage, a broadband output power could be achieved while the DC consumption maintains the same value as that in Fig. 1(a). According to the efficiency equation [$\eta = P_{out} / (P_{in} + P_{DC})$], the efficiency would increase with the increasing frequency due to the higher DC consumption in the lower frequency band. In contrast, in the third matching scheme as shown in Fig. 1(c), the same broadband output power could be achieved with the required mismatches allocated to the input buffer stage, whereas the dynamic DC current I_{DCP} and the total DC consumption P_{DC} could be decreased considerably due to the input power attenuation of the PP pair, and thus a higher efficiency could be achieved compared with that in Fig.1 (b). Therefore, to simultaneously achieve a broadband output power with higher efficiency in the following circuits design, the required mismatches are allocated to the input buffer stage.

III. CIRCUITS DESIGN

The schematic of the proposed FD and the key design parameters are shown in Fig. 2. The design details of the broadband matching for efficiency optimization as well as the 4th-order notch filter for HR2 enhancement are demonstrated in this section.

A. Design of the efficiency-optimized broadband matching

To quantify the exact power mismatch required for the broadband matching within the concerned bandwidth, the power gain degradation of the PP pair and the CS buffers are investigated. For the PP pair, the input impedance could be

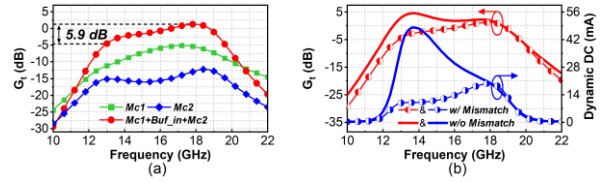


Fig. 4. (a) Simulated G_t of the input buffer stage and its matching networks. (b) G_t comparison and the corresponding dynamic DC currents.

simplified as a gate resistance R_g in series with a gate capacitance C_g . With a fixed voltage swing V_{INP} at the input of the PP pair, the input power variation within the concerned bandwidth from ω_L to ω_H could be expressed as

$$\Delta P_{in_1st} (dB) = 10 \log \left\{ \frac{R_g^2 + 1 / (\omega_L \cdot C_g)^2}{R_g^2 + 1 / (\omega_H \cdot C_g)^2} \right\}. \quad (1)$$

Meanwhile, with the drain current model constructed by a linear function of the effective gate voltage on C_g [8], the amplitude of the HR2 current could be expressed as

$$I_{out_2nd} = \frac{2k \cdot V_{INP} \cdot \sin^3(\alpha/2)}{3\pi \sqrt{1 + (\omega \cdot R_g \cdot C_g)^2}} \quad (2)$$

where ω is the input frequency and α is the conduction angle. To maximize the HR2 component, α is fixed at π and the degradation of the maximum HR2 output power from $2\omega_L$ to $2\omega_H$ could be calculated as

$$\Delta P_{out_2nd} (dB) = 10 \log \left\{ \frac{1 + (\omega_L \cdot R_g \cdot C_g)^2}{1 + (\omega_H \cdot R_g \cdot C_g)^2} \right\}. \quad (3)$$

In this design, with an 11.9- Ω R_g and a 40-fF C_g of the Ka-band PP pair, the CG degradation within the concerned bandwidth could be simplified as

$$\Delta CG (dB) = \Delta P_{out_2nd} - \Delta P_{in_1st} \approx 20 \log(\omega_L / \omega_H). \quad (4)$$

As shown in Fig. 3(a), the calculated CG degradation of the PP pair from (4) matches well with the simulated result under a fixed 750-mV input voltage swing and an optimum HR2 load impedance. In addition, the simulated G_{max} of the input and output buffers are also demonstrated in Fig. 3(b) and (c) to estimate the power gain degradation. To realize broadband matching as well as an optimized efficiency, mismatches are introduced into the TF-based matching networks $Mc1$ and $Mc2$ to compensate for the overall power gain degradation according to Fig. 3. With the design parameters listed in Fig. 2, the transducer power gains (G_t) of $Mc1$ and $Mc2$ are shown in Fig. 4(a). Meanwhile, the G_t of the entire input buffer stage demonstrates a 5.9-dB variation from 26 to 36 GHz, which could exactly compensate for the power gain degradation of the subsequent PP pair and the output buffer. In Fig. 4(b), the G_t of the entire input buffer stage with and without the low-frequency mismatches are compared. With a fixed -6-dBm injected power at the input buffer stage, the dynamic DC currents of the PP pair obtained with optimum load impedances are also presented. Clearly, the DC current is reduced prominently with the proposed mismatches, which is favorable for efficiency improvement, especially in the lower frequency band. In the output buffer stage, $Mc3$ and $Mc4$ are then designed for the maximum power transmission, and thus a broadband FD with optimized efficiency could be achieved.

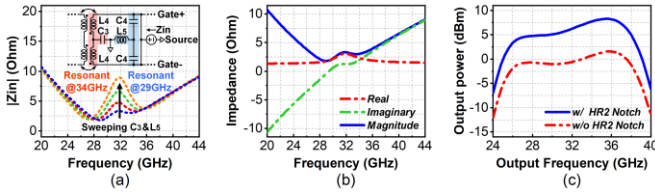


Fig. 5. (a) CM HR2 notch filter optimization. (b) Realized CM impedance. (c) Output power of the PP pair.

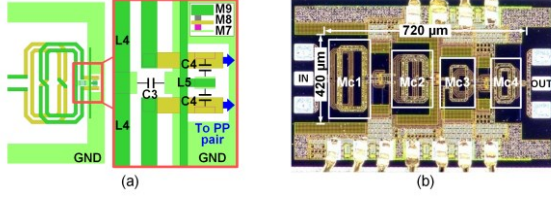


Fig. 6. (a) Layout of the proposed HR2-enhanced notch filter. (b) Micrograph of the proposed FD.

B. Design of the HR2-enhanced notch filter

Due to the parasitic capacitance C_{gd} , the output HR2 of the PP pair would couple to the input with an undesired voltage swing, which would generate an out-of-phase HR2 drain current and thus dramatically degrade the CG [9]. To reduce the common-mode (CM) HR2 voltage swing at the input of the PP pair, a broadband notch filter realized by a 4th-order LC network is integrated into $Mc2$. As shown in Fig. 5(a), to achieve a low CM impedance between the PP pair gate and source over a broad bandwidth, the LC resonances are designed in a staggering way. By enlarging the interval between these two resonance frequencies, the notch filter bandwidth could be widened at the cost of a severer in-band ripple. With the optimization of the LC values, the resonance frequencies of the 4th-order notch filter are finally set around 29 and 34 GHz, respectively, and the realized CM impedance is lower than 4 ohms within the concerned bandwidth as shown in Fig. 5(b). With a -6 dBm injected power at the input buffer stage, the output power of the PP pair obtained with the optimum load impedances is plotted in Fig. 5(c). With the proposed 4th-order notch filter, the output power is enhanced by about 7 dB, which is also favorable for efficiency improvement. The detailed layout of the proposed notch filter is shown in Fig. 6(a).

IV. EXPERIMENTAL RESULTS

The proposed FD is fabricated in a 65-nm CMOS process and the chip micrograph is presented in Fig. 6(b). The chip occupies a core area of $0.72 \times 0.42 \text{ mm}^2$ and works with a 1.2-V supply voltage. The measured output power and efficiency with 15-GHz input are shown in Fig. 7(a), demonstrating an 11.2-dBm saturated output power and a 20.9% peak efficiency. With a -6-dBm input power, the HR2 output power, FRR, and the 3rd harmonic rejection ratios (HRR3) are shown in Fig. 7(b). A measured 42.6% 3-dB FBW from 24.4 to 37.6 GHz is achieved with a >45 dBc FRR and a >40 dBc HRR3. The measured efficiency versus frequency with a -6-dBm input power is shown in Fig. 8(a), and a >15% efficiency is obtained from 24.6 to 36 GHz with a peak value of 23.5%. In addition, the simulated efficiencies with all the dedicated mismatches allocated respectively in the input and output buffer stage are

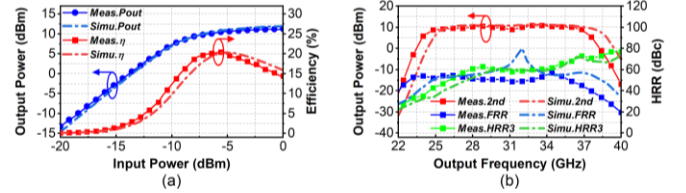


Fig. 7. (a) Measured and simulated output power and efficiency with 15-GHz input. (b) Measured and simulated HR2 output power as well as HRR.

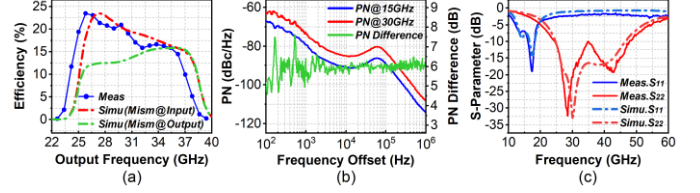


Fig. 8. (a) Measured and simulated efficiencies with a -6 dBm input power. (b) Measured PN of the input (15 GHz) and output (30 GHz) signals with a -6 dBm input power, as well as the PN difference. (c) Reflection coefficients.

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART K/KA-BAND FDS

| Ref | [1] TMIT2018 | [2] MWCL2018 | [3] RFIC2018 | [4] MWCL2021 | This work |
|------------------------|---|---|---|---|--|
| Process | 0.13 μm SiGe | 0.13 μm SiGe | 65 nm CMOS | 110 nm CMOS | 65 nm CMOS |
| Freq (GHz) | 25-40 | 22-36 | 22-25 | 20-25 | 24.4-37.6 |
| Peak η (%) | 22.9 (>15, 30-38GHz) | 27 | 19.5 | 9.9 | 23.5 (>15, 24.6-36GHz) |
| FBW (%) | 46.2(23.5, η >15%) | 48.2 | 35.4 | 22 | 42.6 (37.6, η >15%) |
| P_{sat} (dBm) | 13.5 | 11.9 | 5.7 | -6 | 11.2 |
| P_{in} (dBm) | -1 | -5 | 7 | 0 | -6 |
| CG_{max} (dB) | 17 | 21 | 0.8 | -8.4 | 17.5 |
| P_{DC} (mW) | 84 | 43.1 | 14 | 2.4 | 43 |
| FRR (dBc) | >35 | >32 | >30 | >44 | >45 |
| Features | 4-way TF balun+ common-centroid active cell+C-L-C CM HR2 short | Bootstrapped Gilbert cell + phase control | Fully balanced PP cell+I/Q input | Supply voltage optimization+ 3-coupled inductors | η -optimized matching + 4 th order CM HR2 short |
| FOM ^a | 22.4 | 22.3 | 15.2 | 6.9 | 25 |
| Size (mm^2) | 0.5 | 0.48 | 0.33 | 0.35 | 0.3 ^b |

^a $FOM = \{10 \log[100 \cdot P_{\text{out}} / (P_{\text{in}} + P_{\text{DC}})] + FRR\} \cdot FBW$ [13]. ^b excluding the pads.

also compared, and a prominent efficiency improvement is achieved with the proposed broadband matching strategy. The measured input and output PN are shown in Fig. 8(b). The PN difference from 1.5-kHz to 1-MHz offset is close to the theoretical value of 6 dB, and the additional PN deterioration below 1-kHz offset is mainly caused by the flicker noise from the active circuits. The measured input and output reflection coefficients are shown in Fig. 8(c), and a <-7 dB S_{11} from 13 to 18.5 GHz as well as a <-10 dB S_{22} from 24 to 48 GHz are achieved. The comparison between this work and other state-of-the-art K/Ka-band FDS is shown in Table I, and this work achieves the best figure of merit (FOM) and a competitive efficiency over nearly the entire operating bandwidth.

V. CONCLUSION

A Ka-band FD is presented in this letter. A novel broadband matching scheme for efficiency optimization within the entire operating bandwidth is proposed, and a broadband 4th-order notch filter is also designed for HR2 enhancement. Fabricated in a 65-nm CMOS process, the proposed FD demonstrates a saturated output power of 11.2 dBm. With a -6-dBm input power, an efficiency over 15% is achieved from 24.6 to 36 GHz with a peak value of 23.5%. A 3-dB FBW of 42.6% is also demonstrated with an FRR over 45 dBc.

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