10.7 An 11GHz 2nd-order DPD FMCW chirp generator with 0.051% rms frequency error under a 2.3GHz chirp bandwidth, 2.3GHz/μs slope, and 50ns idle time in 65nm CMOS

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A frequency-modulated continuous-wave (FMCW) chirp generator serves as the pivotal building block for short-range 3D imaging radar systems, which have been widely utilized in medical and security applications. To enable quick and precise scanning with sub-millisecond snapshot duration and sub-centimeter depth resolution in a 79GHz large-scale MIMO radar imaging system, which composes of hundreds of TX/RX elements, the FMCW chirp generator must generate chirps with about 1μs chirp duration and operate >15GHz bandwidth (BW), necessitating an ultra-fast chirp slope exceeding 15GHz/μs. Meanwhile, high chirp linearity and low phase noise (PN) are also essential to improve the signal-to-noise ratio (SNR) for high-quality imaging, and the between-chirp idle time (T_{idle}) must be shortened to 50ns given that at least 95% of the chirp duty-cycle is required. To resolve the contradictions between narrow PLL BW for low PN and quick loop response for fast chirp, two-point-modulation (TPM) technique is widely implemented in fractional-N PLLs [1-5]. Regarding the linearity of an ultra-fast wideband chirp, it is challenging to effectively compensate for the residual frequency error (F_{error}) of a 1st-order digital pre-distortion (DPD) [2-4] and the ramp non-linearity of a ramp tracker [1,5] with an insufficient PLL bandwidth, calling for advanced curve fitting techniques. In this work, to diminish rms F_{error} in the context of ultra-fast wideband chirp generation, a ramp-tracker assisted 2nd-order curve-fitting (2nd-CF) DPD is proposed in a fractional-N sub-sampling (SS) PLL, achieving an 11GHz fast saw-tooth chirp with a 2.3GHz chirp bandwidth, 2.3GHz/μs chirp slope, and 0.051% rms F_{error}. Leveraging an integral path in the digital loop filter (DLF), dynamic track-and-hold functionalities are realized in the voltage tracking loop (VTL) for robust LUT calibration. Advanced phase control is investigated in a DTC modulator to eliminate the fluctuation of the loop locking voltage during large frequency hopping (>20% of the center frequency f_{center}), which further secures 50ns T_{idle}.

Conventionally, a 1st-order curve-fitting (1st-CF) DPD technique can be used to obtain a well-fitted VCO tuning curve, in which a 1st-order look-up table (1st-LUT) for ramp fitting [3] and 0th-order LUT for ramp-rate fitting [2] are both practical solutions. However, with an enlarged chirp BW and slope, the residual F_{error} becomes more severe; thus, a higher-order curve-fitting DPD is required. Unfortunately, direct ramp fitting using a 2nd-order LUT suffers from high design and hardware complexity. In this work, by leveraging the integral mechanism of the ramp integrator, the 2nd-CF DPD functionality for ramp fitting is realized by implementing a 1st-LUT ahead of the ramp integrator as shown in Fig. 10.7.1. In the 1st-LUT, c_i is estimated with an LMS algorithm, and g_i is calculated by c_{i+1}-c_i. The chirp-frequency control word (FCW) fcw_chirp[k] is scaled to cover 16 registers. As shown in Fig. 10.7.1 (bottom right), the proposed 2nd-CF DPD achieves smaller residual F_{error} compared with the conventional 1st-CF DPD. However, due to the integral operation of the calibrated ramp rate and interactions among c_i through the calculation of g_i [4], the convergence of the LUT slows down and becomes unstable. To tackle this problem, a pre-running ramp tracker is leveraged to initialize the LUT with the coefficients that are close to final convergent states, and a multiplexer is utilized to switch between the ramp tracker and the LUT in different time slots. In the first chirp period, the ramp tracker is enabled to configure a slower chirp but with the same target BW. The sampling principle of the estimated slope slope_rt[k] is demonstrated in Fig. 10.7.1 top right. Addressed by the scaled FCW fcw_scale[k], 16 coefficients are sampled from slope_rt[k] and then passed to c_i in the LUT. Subsequently, the LUT is enabled to configure the desired fast chirp with the initialized c_i. The cooperation between the ramp tracker and LUT is elaborated in Fig. 10.7.1 (bottom left) for over 100% VCO gain variations. Clearly, as most of the ramp non-linearity is estimated by the ramp tracker, the converged c_i gets very close to the initialized value, greatly reducing the convergence time.

In an SS-PLL, the sign of the phase error for background calibration could not be extracted directly. Conventionally, it could be extracted from the output current of a transconductor G_m [2,3], but the comparator offset would cause calibration inaccuracies. Alternatively, as the sampling voltage V_{samp} of the SSPD stays stable while the SS-PLL is locked, a VTL could be utilized for sign extraction [6]. The architecture of the proposed VTL in cooperation with SSPD, G_m, and pulser and their timing diagrams are shown in Fig. 10.7.2. In each SSPD clock cycle, the comparator clock CMP_CLK is delayed by a G_m pulse, which effectively prevents the PLL performance deterioration caused by the kickback effect. Within the voltage tacking range of the VTL, the locking point could be tracked precisely, overcoming the impact of process variations and circuit offsets (i.e., comparator offset V_{cmp_os} and G_m offset G_{m_os}). However, in the ramp duration before the LUT convergence is accomplished, V_{samp} fluctuates largely due to the unlocked phase, which further disturbs V_{tmp} and generates inaccurate EK_EXT for the LUT calibration. As a result, the LUT convergence inevitably slows down. To tackle this issue, by newly involving an integral path to the DLF in the VTL, the non-zero offset of EK_EXT could be removed, and V_{tmp} could be held during the ramp duration for a robust LUT calibration. In the DLF, β is set much larger than α to ensure stability, and the tracking speed can be improved by enlarging α. The detailed functionality of the VTL in three working states is shown in Fig. 10.7.2 (bottom). In the tracking state, with EK_EXT=1, V_{tmp} grows steadily along with DLF_{out}, covering a wide trackable voltage range. In the stabilized state, DLF_{out} tends to stabilize, and V_{tmp} fluctuates around V_{samp} within the maximum step of ΔV-DAC, generating a zero-mean EK_EXT. In the hold state, the DLF is disabled, and its output maintains the last state of the integral path, which makes V_{tmp} immune to a V_{samp} drift. Subsequently, the DLF is enabled, and the VTL is activated again to update V_{tmp}. In this work, to operate the VTL properly with the LUT for robust sign extraction, EN_DLF is enabled in T_{idle} and disabled in T_{chirp}, while EN_LUT takes the inverse logic as shown in Fig. 10.7.2 (middle right).

The architecture of the proposed FMCW chirp generator is shown in Fig. 10.7.3. In the lowpass injection path, a delay-spread calibration [7] is utilized to compensate for the response time of the VDAC. The DTC modulator could compensate the phase error caused by the quantization of a delta-sigma modulator (DSM), but there still exists a residual mismatch of the compensated phase error during the large frequency hopping in the conventional structure [2,3], which causes a V_{PLL} fluctuation in the T_{idle}. As shown in the two bottom-left figures in Fig. 10.7.3, the voltage fluctuation becomes more severe with wider BW_{chirp}, and the loop fails to settle within tens of nanoseconds, which deteriorates F_{error} at the beginning of each chirp. In this work, a zero-phase-error DTC modulator designed for the ultra-fast wideband saw-tooth chirp is proposed to eliminate the V_{PLL} fluctuation over 2.3GHz frequency hopping. Based on the principles of the DTC compensation and phase modulation in the TPM, the exact extra phase, $Diff[k]\times K_{DTC}[k]$, to be compensated in the k-th cycle is accumulated to generate a DTC code for sampling the next zero-crossing precisely, whereas the conventional DTC modulator fails, especially facing with large frequency hopping. To avoid an unbounded DTC code, the accumulated phase error ACC[k] is wrapped by the DTC gain $K_{DTC}[k]$, further generating the carries C_ACC[k] and the residues R_ACC[k] for the multi-modulus divider (MMD) and DTC, respectively. As shown in Fig. 10.7.3 (bottom right), with the proposed DTC modulator, the voltage fluctuation due to 2.3GHz frequency hopping is eliminated significantly, thus ns-level T_{idle} could be achieved. Moreover, an LC-VCO with complementary varactors is designed to enhance the linearity under >2.5GHz/V KVCO, and following the VDAC additional lowpass RC filters are used to suppress the DSM quantization noise.

The proposed FMCW generator is fabricated in a 65nm CMOS process. The die micrograph is shown in Fig. 10.7.7, and the core area is about 1.2mm^2 excluding decoupling capacitors and test circuits. During chirp modulation, the measured power consumption is about 50.8mW. The fractional-N SS-PLL could generate frequency from 9.6 to 12.4GHz with a 100MHz reference clock. At 10GHz, the measured PN and spectrum of the proposed PLL in the fractional-N mode are shown in Fig. 10.7.4 to indicate the worst-case performance. The measured PN is -116.0dBc/Hz at a 1MHz offset, which is equivalent to -98dBc/Hz normalized to 79GHz, and the worst-case spur is -52.49dBc at a 1.5kHz offset. The divide-by-16 spectrum of the FMCW is measured with a 2.4GHz BW_{chirp}. Figure 10.7.5 shows that the measured rms F_{error} of the fastest chirp configured with a 2.3GHz/1μs chirp slope and 50ns T_{idle} is around 1176kHz (0.051% of BW_{chirp}) and the measured frequency range (MFR) is 2.16GHz. For a slower chirp with a 2.4GHz/10μs slope and 500ns T_{idle}, the rms F_{error} is about 240kHz (0.01% of BW_{chirp}). Configured with a 2.4GHz/50μs slope and 1μs T_{idle}, the rms F_{error} of the chirp is about 49.6kHz (0.002% of BW_{chirp}). As shown in Fig. 10.7.5 (bottom right), the rms F_{error} with the 1st-CF DPD and 2nd-CF DPD are compared under different chirp slopes, demonstrating that the 2nd-CF DPD outperforms the 1st-CF DPD especially for the faster chirp slope. Compared with prior works in Fig. 10.7.6, the proposed FMCW generator achieves the fastest chirp slope and the best chirp linearity with a ns-level idle time.

Acknowledgement:

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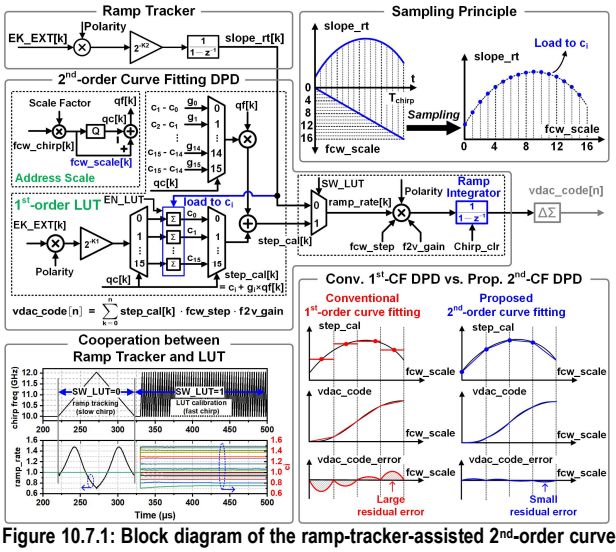


Figure 10.7.1: Block diagram of the ramp-tracker-assisted 2nd-order curve-fitting DPD.

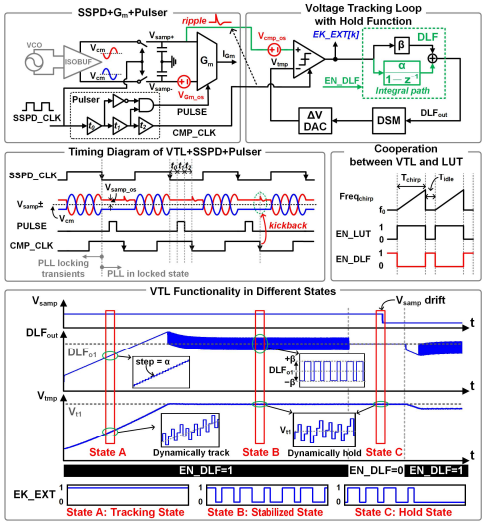


Figure 10.7.2: Block diagram and the working principles of the VTL.

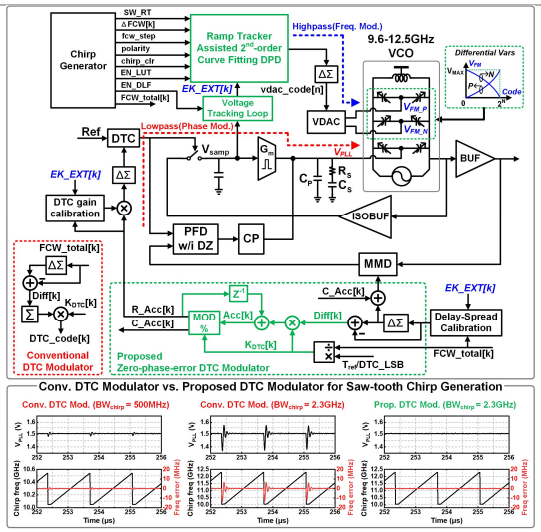


Figure 10.7.3: Block diagram of the proposed FMCW synthesizer and the comparison of the frequency error between conventional and proposed DTC modulators (bottom).

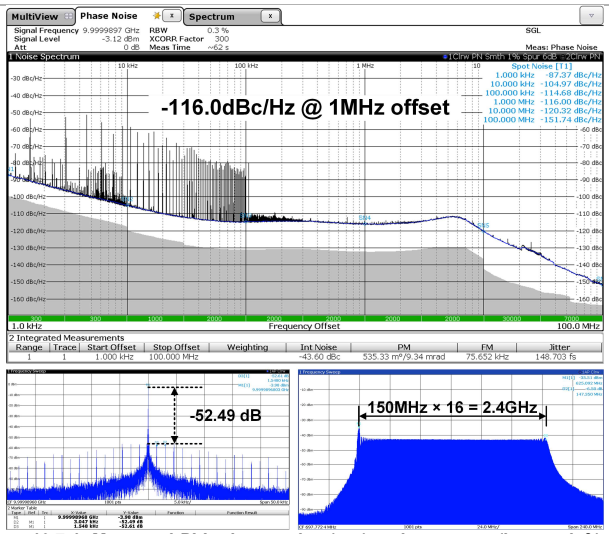


Figure 10.7.4: Measured PLL phase noise (top) and spectrum (bottom left) and measured saw-tooth chirp spectrum with a 2.4GHz chirp bandwidth and a 10μs chirp duration (bottom right).

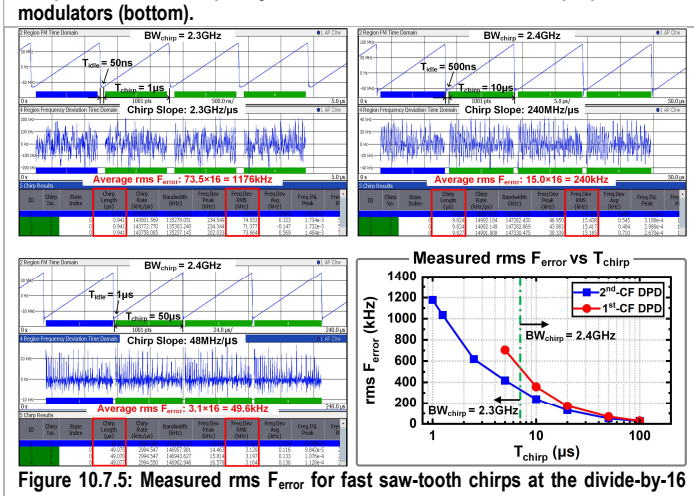
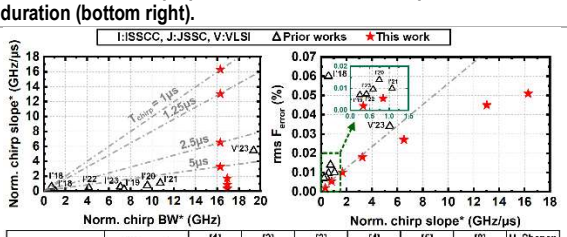


Figure 10.7.5: Measured rms F_{error} for fast saw-tooth chirps at the divide-by-16 output. Comparison of the measured rms F_{error} between the 1st-CF DPD and 2nd-CF DPD under different chirp slopes.



	This work		[1] ISSCC'21	[2] ISSCC'20	[3] ISSCC'19	[4] JSSC'18	[5] VLSI'23	[8] ISSCC'23	H. Shanan ISSCC'22
Architecture	SSPLL+TPM +2^{17}-order curve fitting DPD		ADPLL +TPM	SSPLL +TPM +QDAC	SSPLL +TPM	BBPLL +TPM	ADPLL +Type II TPM	CPPLL +TPM	RTWO-Based ADPLL
Reference(MHz)	100		200	80	80	52	76.8	80	80-200
Frequency(GHz)	9.6~12.4		21.8-25.4	8.3-11.7	14.7-17.2	20.4-24.6	11.4-16.4	15-18.5	8.8-12
BW_{chirp}/T_{chirp} (GHz/μs)	2.3/1.0	2.4/10	3.2/10	1.21/12.8	1.5/30	0.2/1.2	3.43/4.8	1.5/12	0.5/10
MFR(GHz)	2.16	2.35	-	1.14	1.49	-	2.50***	1.43	-
rms F_{error}(kHz)(%)	1176 (0.051)	240 (0.010)	309 (0.010)	168 (0.014)	103 (0.007)	124 (0.06)	1157 (0.034)	138 (0.0096)	37 (0.0074)
*Norm. BW_{chirp} (GHz)(%)	16.29 (20.6)	16.93 (21.4)	10.76 (13.33)	9.559 (11.95)	7.406 (9.375)	0.714 (1.0)	19.36 (24.5)	7.075 (8.95)	4.158 (6.5)
*Norm. chirp slope(MHz/μs)	16296	1693	1076	747	247	595	5417	589	416
*PN@1MHz offset (dBc/Hz)	-98		-83.5	-90.7	-92.6	-90	-85	-91	-102.6
Idle time(μs)	0.05	0.5	-	-	2	0.2	-	1	0.0125**
Power(mW)	50.8		28	11.7	44	19.7	10	16.5	187
Core Area(mm^2)	1.2		0.26	0.9	1	0.48	0.19	0.6	2
Chirp waveform	Saw & Tri		Saw & Tri	Saw	Saw	Saw & Tri	Tri	Saw	Saw
CMOS technology	65nm		40nm	28nm	28nm	65nm	28nm	28nm	28nm

*Normalized to 79 GHz **With 2μs settling time ***Estimated from measured figure

Figure 10.7.6: Performance summary and comparison with prior works.

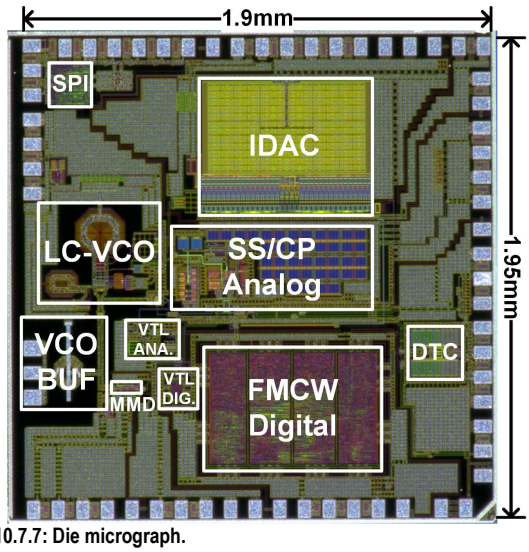


Figure 10.7.7: Die micrograph.

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