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GeTe/Sb_2Te_3 Super-Lattices: Impact of Atomic Structure on the RESET Current of Phase-Change Memory Devices

*Damien Térébénec, Françoise Hippert, Nicolas Bernier, Niccolo Castellani, and Pierre Noé**

Phase change memories (PCMs) are at the heart of modern memory technology, offering multi-level storage, fast read/write operations, and non-volatility, bridging the gap between volatile DRAM and non-volatile Flash. The reversible transition between amorphous and crystalline states of phase-change materials such as GeTe or $Ge_2Sb_2Te_5$ is at the basis of PCM devices. Despite their importance, PCM devices face challenges including high power consumption during the RESET operation. Current research efforts focus on improving device architecture and exploring alternative phase-change materials such as GeTe/Sb_2Te_3 super-lattices (SLs), for which a reduced programming power consumption is observed compared with standard PCMs. Herein, by combining X-ray diffraction and scanning transmission electron microscopy imaging of SL thin films with the study of the same SL in PCM devices, it is shown that it is possible to significantly decrease RESET energy of the device, without modifying the SL composition, by reducing the amount of structural defects through annealing treatment. The best device properties are obtained after transforming the SL into a defect-free, highly out-of-plane oriented rhombohedral phase. These results offer a promising avenue for further improving the performance of SL-based PCM devices through structural optimization.

1. Introduction

From their discovery over 50 years ago to their current leading position among emerging memory technologies, Phase-Change Memories (PCMs) offer a unique set of features (multi-level storage, fast read/write latency, non-volatility, good cycling endurance, and good scalability beyond lithographic limits) to bridge the performance gap between volatile Dynamic Random Access Memory (DRAM) and non-volatile Flash memories. This has led PCMs to play a major role in storage memory today, as well as in emerging neuromorphic and in-memory computing applications.[1] PCMs are currently at the forefront among the various types of emerging memory.[2] In a PCM device, a fast and reversible switching between amorphous and crystalline phases of a phase-change material, such as GeTe or $Ge_2Sb_2Te_5$ chalcogenide alloys, is induced by applying electrical pulses.[3,4] A large resistance contrast is observed between the SET state, where the phase-change material is entirely crystalline, and the RESET state, where an amorphous dome is present above the bottom electrode. This contrast arises from the large difference in resistivity between the amorphous (high resistivity) and crystalline (low resistivity) phases of the phase-change material. In the case of $Ge_2Sb_2Te_5$, the crystalline phase is a metastable cubic phase. The main drawback of PCM devices compared with competing resistive memories is the excessively high power consumption during the RESET operation, i.e., the transition from the low resistance state (LRS) to the high resistance state (HRS). This requires the phase-change material to be locally amorphized by a Joule-induced melting and quenching process, thanks to rapid heat dissipation in the memory cell.[3,4,5] A major research effort has been devoted to improving the device architecture to better confine heat during pulses or to find phase-change materials other than the alloys located on the GeTe-Sb_2Te_3 pseudo-binary tie line in the Ge-Sb-Te phase diagram. A promising direction is to integrate a GeTe/Sb_2Te_3 super-lattice (SL) obtained by a periodic deposition of nm-thick crystalline GeTe and Sb_2Te_3 layers with atomic planes parallel to the substrate's surface. As first shown by Simpson et al.[6] and then confirmed by other groups,[7–10] PCM devices based on a GeTe/Sb_2Te_3 SL exhibit a lower power consumption than similar devices containing a GeTe or $Ge_2Sb_2Te_5$ alloy. The thickness of the GeTe is most often chosen equal to 0.7 nm (or 1 nm), which corresponds to the thickness of two Ge and two Te planes in the rhombohedral GeTe phase.[11] The rhombohedral Sb_2Te_3 phase consists of a periodic stacking of 1.015 nm thick blocks of Te/Sb/Te/Sb/Te atomic planes (so-called quintuple layers (QLs)) separated by pseudo van der Waals (vdW) gaps. The term pseudo is introduced because the distance between Te atomic planes across a gap is smaller than that expected for a true vdW gap.[12,13] The thickness of the deposited Sb_2Te_3 layers

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in an SL is therefore chosen to contain *m* QLs, with *m* an integer varying typically between 1 and 8. The origin of the reversible switching between a low (HRS) and a high (HRS) resistance state in PCM devices based on SLs was first ascribed to a crystal-crystal transition involving a switch of the Ge planes at the interface with a Sb_2Te_3 QL, hence the name interfacial phase-change memory (iPCM) introduced in reference[6]. However, this model, as well as all other models based on the existence of GeTe layers,[14,15,16] is not valid because the actual atomic structure of the deposited films differs from the targeted GeTe/Sb_2Te_3 SL structure.[17–23] Intermixing of the GeTe and Sb_2Te_3 layers occurs, whatever the deposition method used, whether sputtering,[17–19] pulsed laser deposition,[20,21] or molecular beam epitaxy (MBE).[22,23] Scanning transmission electron microscopy (STEM) images show that an SL film consists of a stacking of Sb_2Te_3 quintuple layers (QLs) and blocks containing Te planes and planes with a mixed Ge/Sb occupancy (so-called GST blocks).[17,18,20,21,22] Blocks are separated by pseudo vdW gaps. The GST blocks in SLs are similar to those existing in the ternary rhombohedral Ge-Sb-Te phases belonging to the GeTe-Sb_2Te_3 pseudo-binary tie line.[17,22,24–30] Despite the absence of GeTe layers, the films obtained are still referred to in the literature as GeTe/Sb_2Te_3 SLs, in reference to the fact that they are obtained by alternately depositing crystalline GeTe and Sb_2Te_3 layers with atomic planes parallel to the substrate's surface.

The low energy consumption of SL-containing devices during the RESET operation has been attributed to a resistive switching involving structural reorganizations in the crystalline SL, in contrast to the crystal-amorphous phase transition that occurs via a Joule-induced melting-quenching process in devices incorporating polycrystalline phase-change alloys. However, recent works have shown that the switching of SL-based PCM devices from the LRS to HRS occurs through a melting-quenching process leading to amorphization of the SL.[8,9,10] For a given material, a decrease in the RESET current (I_{RESET}) as the resistance of the LRS state (R_{SET}) increases is well established for standard PCM devices incorporating phase-change alloys, based on studies of the impact of cell size on thermal confinement. Thus, the observation of a decrease in I_{RESET} as R_{SET} increases in SL-based devices was attributed to a melting-quenching process.[8] This was later proven by the observation of an amorphous dome in SLs programmed to the HRS.[9,10] The low power consumption of SL-based devices during the RESET operation must therefore be related to the electronic and thermal properties of the SL. The out-of-plane thermal conductivity of a GeTe(1 nm)/Sb_2Te_3(4 nm) SL was found to be nearly temperature-independent in the range of 300–700 K and lower than that of a polycrystalline cubic or rhombohedral $Ge_2Sb_2Te_5$ alloy.[31] In the latter study, changes in the thermal conductivity according to the SL design were reported.

In previous work, we observed a decrease in RESET current when decreasing disorder within SL's atomic structure. Decreasing disorder could be achieved by increasing the thickness of the Sb_2Te_3 layer from 2 to 8 nm in the deposited SL, for a fixed thickness (0.7 nm) of the GeTe layer.[9] In the present work, we present a novel approach that correlates the programming characteristics of devices incorporating a $[(GeTe)_2(Sb_2Te_3)_2]_p$ SL, where *p* is the number of periods, subjected to various post-fabrication thermal treatments, with information on the structure of similar SL films deposited on SiO_2, and annealed under the same conditions as the devices. We show that a significant decrease in RESET energy of the device can be achieved, without changing the SL composition, by reducing the number of structural defects through annealing treatment. The best performance is obtained after the transformation of the SL into a highly out-of-plane oriented, defect-free rhombohedral phase.

2. Effect of Annealing on the Atomic Structure of a 0.7/2 SL Film

Information on the deposition conditions of the SL film by magnetron sputtering on a 500 nm-thick thermal SiO_2 layer on a Si (100) wafer (200 mm diameter) is given in the Experimental Section. The thickness of the deposited $(GeTe)_2$ block being 0.7 nm and the thickness of the Sb_2Te_3 layer being close to 2 nm (two Sb_2Te_3 QLs), the film is labeled 0.7/2 SL in the following. The SL film is protected against oxidation by a 10 nm thick SiN_x layer. A square piece of the 130 nm thick film was cleaved into 4 samples (size 1 cm × 1 cm). Three samples were heated at 300 °C for 15 min. This thermal treatment is chosen to reproduce the maximum thermal budget to which an SL layer is submitted during the integration process in our PCM test vehicle devices. Two samples were then annealed at 415 °C for 1 h and finally, one sample was submitted to an additional annealing at 450 °C for 15 min. The annealing temperature has been limited to 450 °C, as this is the maximum temperature that can be reached by PCM devices during back-end-of-line (BEOL) integration in microelectronics. The aim of annealing at 415 °C and above was to reduce the structural disorder in the SL. The results presented below show that this objective was achieved and that these heat treatments transform the SL into an out-of-plane oriented $Ge_1Sb_2Te_4$ rhombohedral phase. The diffraction patterns of a pristine sample (as-deposited at 250 °C) and annealed samples were measured by X-ray diffraction (XRD) and then electron-transparent foils were prepared and studied by scanning transmission electron microscopy (STEM).

Out-of-plane XRD patterns are shown in **Figure 1**, High-angle annular dark-field (HAADF)-STEM images in **Figure 2**, and crystal orientation maps (COM) measured by precession electron diffraction (PED) in **Figure 3**. HAADF-STEM and PED techniques play complementary roles in the analysis of SL films, as PED provides insights into the orientation, size, and shape of crystalline domains, while HAADF-STEM reveals atomic local order, block types, and potential structural defects within a crystalline domain.

The XRD patterns of the 0.7/2 SL film annealed at 300 °C and the as-deposited film are similar. They show narrow diffraction peaks coexisting with much broader ones, as previously observed in GeTe/Sb_2Te_3 SLs.[9,17,18,22,32,33] The COMs of the two films are also similar in terms of crystal orientations and domain size and shape. Only crystallites with the <0 0 1> direction (hexagonal indexation) almost perpendicular to the substrate, i.e., with atomic planes almost parallel to the substrate, are detected in the x-maps. The y- and z- maps show that these crystallites differ by their in-plane orientation. Thus, the as-deposited and 300 °C annealed 0.7/2 SL films have a fiber texture, as previously observed for GeTe/Sb_2Te_3 SLs and Sb_2Te_3 films deposited by sputtering on amorphous substrates.[17,18] The lateral size of the crystallites is in the range [30–120 nm]. Only a few crystallites

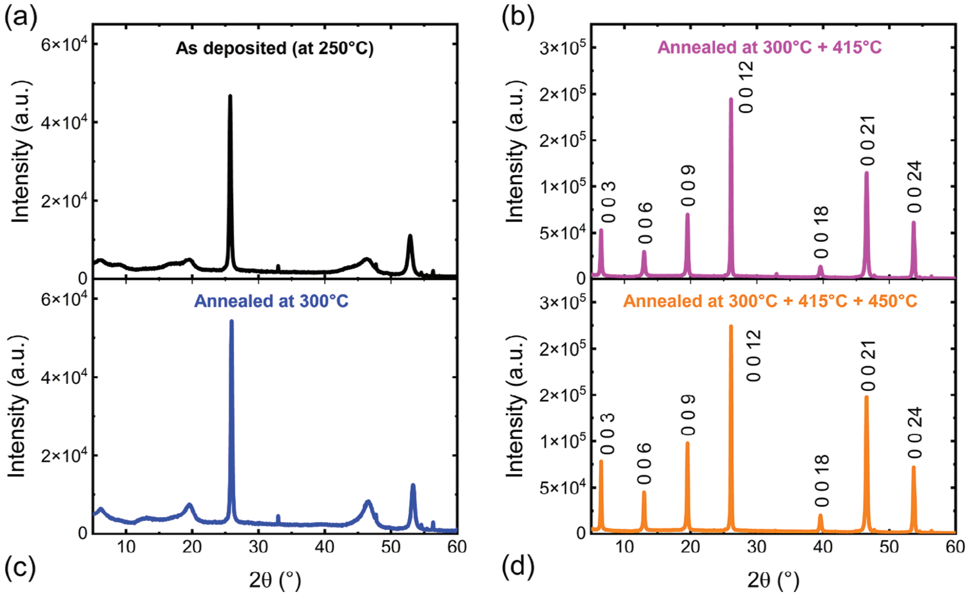

Figure 1. Out-of-plane XRD patterns (Cu K_α radiation) of a 0.7/2 SL film in the pristine state (as-deposited at 250 °C) a) and after cumulative annealing treatments b,c,d). The XRD patterns of the as-deposited film and the film annealed at 300 °C are similar with the coexistence of narrow and broad diffraction peaks. The XRD patterns of films annealed at 415 °C (c) and 450 °C (d) only contain narrow peaks all of which can be indexed as 0 0 *l* peaks (hexagonal indexation) of a rhombohedral $Ge_1Sb_2Te_4$ phase with a *c* parameter equal to 4.095 ± 0.003 nm.

have a vertical size coinciding with the film thickness (130 nm). Additional information on the distribution of the orientation of the atomic planes between different crystallites is obtained by measuring rocking curves for a narrow diffraction peak at $2\theta = 25.8°$ (Figure S1, Supporting Information). The rocking curves of the as-deposited and 300 °C annealed films are similar. Their Full Width at Half maximum (FWHM) is 5.2 ± 0.3°, excluding a small contribution (relative area of the order of 2%) from crystallites with a much narrower orientation distribution (FWHM of 0.45 ± 0.1°).

The presence of broad peaks in the XRD pattern is a consequence of the stacking disorder in the SL. The HAADF-STEM image acquired in a crystallite of the as-deposited 0.7/2 SL shows GST blocks of various numbers of atomic planes, and hence heights, separated by gaps (dark lines in the image) between two Te planes, in agreement with previous

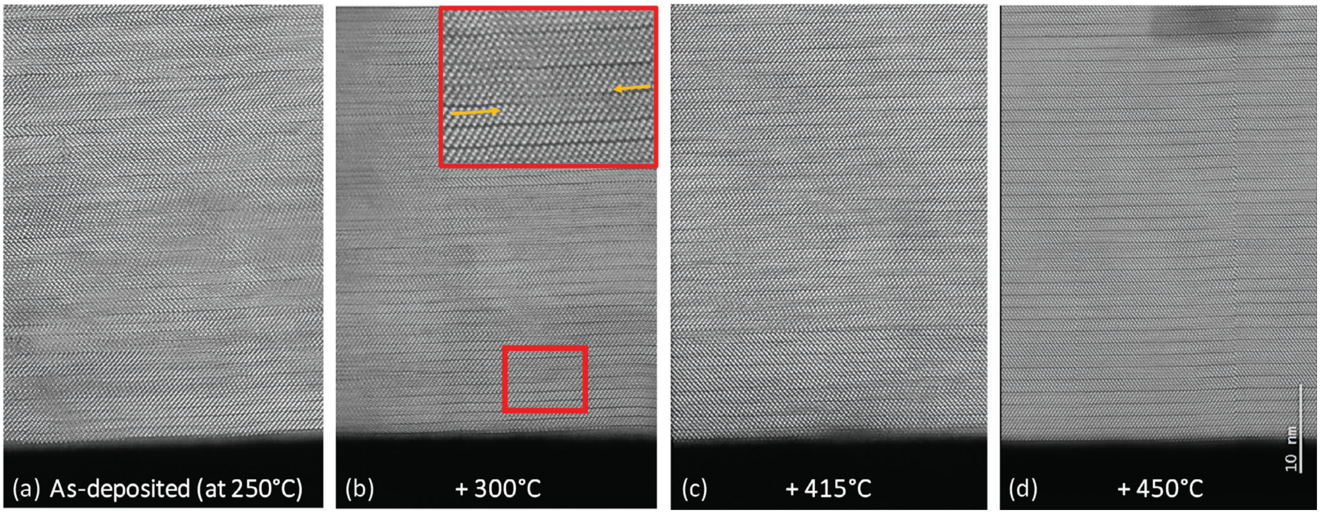

Figure 2. High-resolution HAADF-STEM cross-sectional images of a 0.7/2 SL film in the pristine state (as-deposited at 250 °C) a) and after cumulative annealing treatments b,c,d). Blocks differing by the number of atomic planes are separated by gaps (dark lines). The nature of the stacking changes in the lateral direction in (a), (b), and (c) due to the presence of a large number of bilayer defects, as illustrated in the inset shown in (b) (zoom in the red rectangle) where bilayers defects are indicated by arrows. In (d) no bilayer defects are present and the stacking consists only of blocks of 7 atomic planes, apart from a block of 9 planes in the center of the image. In (a) and (b) the Sb_2Te_3 QLs of the seed layer are clearly visible above the SiO_2 layer. They are absent in (c) and (d) due to intermixing with the above layers induced by annealing. Viewing direction: along the zone axis <1 1 −2 0>.

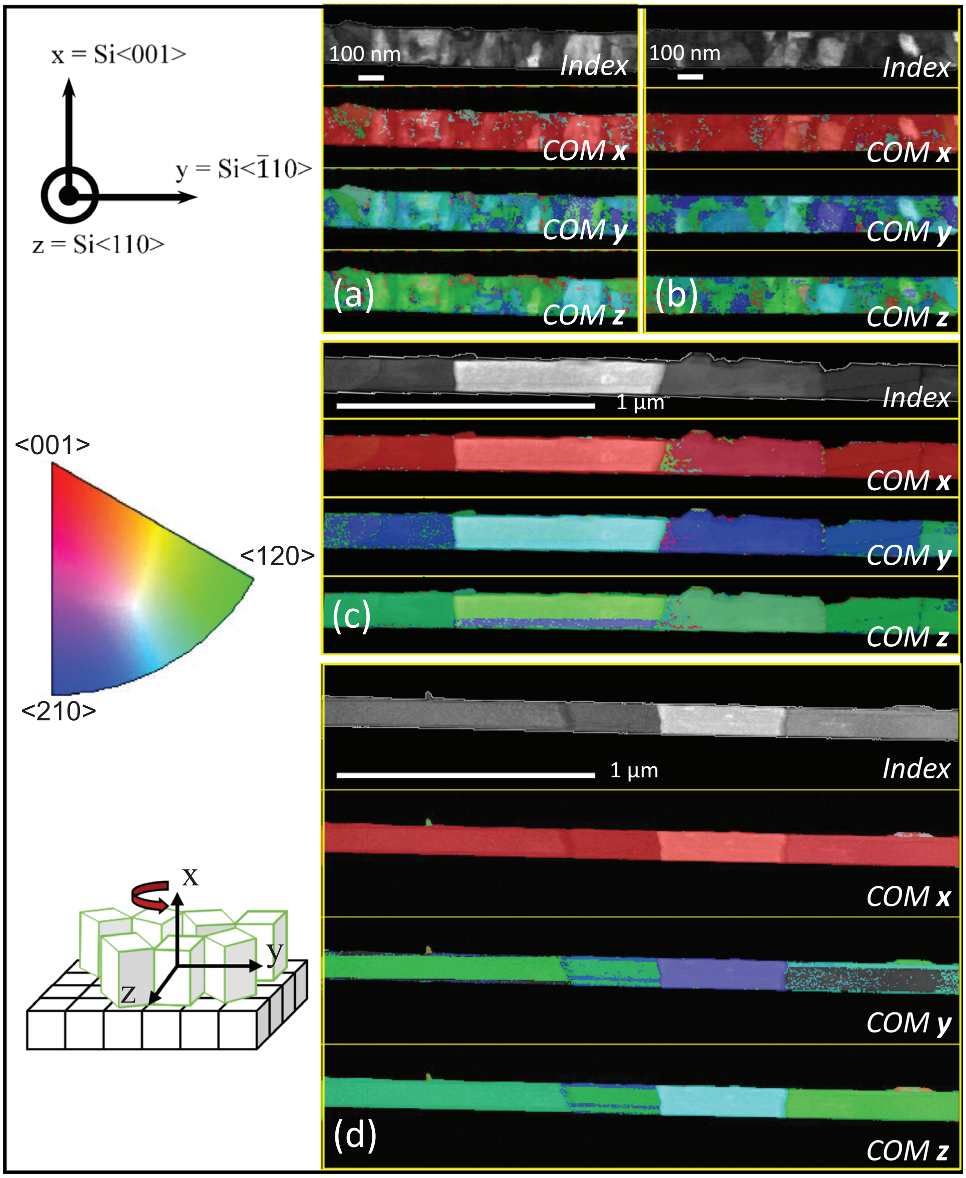

Figure 3. Index maps and crystal orientation maps (COM), superimposed on index maps, along the x, y, and z directions in a 0.7/2 SL film in the pristine state (as-deposited at 250 °C) a) and after cumulative annealing treatments: 300 °C b), 415 °C c) and 450 °C d). The orientation of x, y, and z axes with respect to the Si (100) substrate is shown in the insert. The x direction corresponds to the film normal, while the y and z directions are in the film plane and form an angle of 90°. The orientation of the crystallites is coded using the inverse pole figure color map given in the insert. For instance, red is assigned to a crystallite with the <001> direction aligned with the selected COM direction (x, y, or z). The grey levels of index maps give the correlation index between simulated and measured electron diffraction patterns. Brighter areas indicate stronger matches. The fiber structure of the films is represented in a schematic drawing in insert.

HAADF-STEM studies.[17,18,20–22] The magnification of the images in Figure 2 was chosen in order to analyze the stacking of the blocks in the SL on a large scale, which prevents an analysis of intensity profiles across a given block. In addition to Sb_2Te_3 QLs containing 5 atomic planes, GST blocks containing 7, 9, or 11 atomic planes are observed. Blocks containing a larger number of atomic planes are also detected. When comparing the nature of the successive blocks along arbitrary vertical lines perpendicular to the atomic planes, many changes are detected according to the lateral position of the lines in the 35 nm wide HAADF-STEM image. These changes are due to the presence of a large number of so-called bilayer defects.[34–37] A bilayer defect involves a swapping of Te and Ge/Sb planes and thus a change in the position of the pseudo vdW gap and a change in the nature of the two adjacent blocks, as illustrated in the inset in Figure 2b. After annealing at 300 °C, most of the GST blocks containing more than 11 atomic planes have disappeared, in agreement with the results reported in the reference[34] There are still a large number of bilayer defects. Note that the electron beam intensity during the acquisition of all HAADF-STEM images was restricted to less than 30 pA so that the beam does not induce structural changes, as GeTe/Sb_2Te_3 SLs are prone to reorganizations of bilayer defects, vdW gaps, and block stacking under high electron irradiation.[35] In summary, the atomic structure and the microstructure of 0.7/2 SL films as-deposited and annealed at 300 °C are very similar, with only a small reduction in block disorder observed after annealing at 300 °C.

However, significant changes are observed after annealing at 415 °C. A majority of blocks containing 7 atomic planes are observed in the HAADF-STEM image of the film annealed at 415 °C, coexisting with blocks with 5 or 9 atomic planes (Figure S2, Supporting Information). A significant number of bilayer defects are still present. The XRD pattern of this film only contains narrow diffraction peaks, all of which can be indexed as 0 0 l peaks (hexagonal indexation) of a rhombohedral $Ge_1Sb_2Te_4$ phase,[25,28] in agreement with the overall nominal composition of the deposited film (see the Experimental Section). The parameter c equals 4.095 ± 0.003 nm (Figure S3, Supporting Information). This value is in excellent agreement with that reported for a $Ge_1Sb_2Te_4$ single crystal[38] and epitaxial $Ge_1Sb_2Te_4$ films.[25] The FWHM of the rocking curve measured at $2\theta = 26.09°$ (0 0 12 diffraction peak) is 1.25 ± 0.08° (Figure S1, Supporting Information), a much smaller value than in the film annealed at 300 °C (5.2 ± 0.3°). This significant reduction in the distribution of orientation of the atomic planes between the different crystallites is accompanied by a spectacular increase in their lateral size, as shown by the COMs. The lateral size of the largest crystallites reaches ≈800 nm in the film annealed at 415 °C, while the size of the smallest ones is ≈150 nm. The vertical size of several crystallites coincides with the film thickness, as can be seen by comparing the x-, y-, and z-maps. In other cases, a stacking of two crystallites with in-plane orientation differing by 60° is observed across the thickness of the film. Such twin domains are frequently observed in SLs and rhombohedral $Ge_1Sb_2Te_4$ or $Ge_2Sb_2Te_5$ epitaxial films deposited by MBE on monocrystalline Si (111).[17,25,39] The comparison of the COMs obtained for as-deposited or 300 °C annealed films with those of the 415 °C annealed film shows that crystallite coalescence is induced by annealing at 415 °C. In summary, annealing at 415 °C strongly reduces the block disorder present in the as-deposited 0.7/2 SL and leads to an XRD pattern that can be indexed as a rhombohedral $Ge_1Sb_2Te_4$ phase. These observations are in agreement with the results obtained on GeTe(1 nm)/Sb_2Te_3(3 nm) SLs deposited by MBE or sputtering and annealed at 350 or 400 °C.[17,22] The present study shows that this structural transformation is accompanied by a strong increase in the lateral size of the crystallites and a reduction of the disorientation of atomic planes with respect to the substrate. Annealing at 450 °C further improves structural order. An almost perfect stack of blocks containing 7 atomic planes is observed in a HAADF-STEM image, with a single exception in the center of the image where a block with 9 atomic planes is present. No bilayer defects remain after annealing at 450 °C. The structural changes revealed by comparison of the HAADF-STEM images of films annealed at 415 or 450 °C are not detectable by XRD. The out-of-plane XRD patterns (Figure 1) and the rocking curves (Figure S1, Supporting Information) are similar. As shown by the COMs, the microstructure of the 450 °C annealed film is not significantly different from that of the 415 °C annealed film, with the exception of a further increase in the lateral size of several grains. Thus, annealing at 450 °C eliminates the residual disorder present after annealing at 415 °C and transforms the initial 0.7/2 SL structure into an almost perfectly out-of-plane ordered, defect-free, rhombohedral $Ge_1Sb_2Te_4$ phase with a large lateral crystallite size reaching ≈1 µm.

3. Electrical Characterization of As-Fabricated and Annealed PCM Devices

Memory cells integrating a 0.7/2 SL were studied in as-fabricated devices and in devices that have been subjected to annealing treatments similar to those applied above to the 0.7/2 SL film deposited on SiO_2 (either 415 °C for 1 h or 415 °C for 1 h + 450 °C for 15 min). The equivalent thermal budget applied to the SL layer after deposition in as-fabricated devices, resulting from the subsequent deposition of multiple dielectric and metallic layers at the end of the integration process, corresponds to annealing at 300 °C for ≈15 min. The initial state of a memory cell, whether after fabrication or after annealing, is a low resistance state. No programming or forming operation is applied to a device before switching it to an HRS by applying successive electrical pulses of increasing voltage (see the Experimental Section). This ensures that the structural state of the SL is similar in devices in the initial low resistance state and in full sheet SL films studied by means of XRD and STEM-HAADF in section 2, which is mandatory to correlate device properties and SL atomic structure. R-I curves, with R the resistance of a memory cell and I the current flowing during a programming pulse, were measured on 11 to 16 memory cells, either in the as-fabricated state or after annealing. The individual R–I curves and the median curve for each device type are shown in **Figure 4**a. Clear changes are induced by the annealing of devices after fabrication. These are much larger than the variability observed between devices of the same type. The dispersion of R–I curves from one device to another may be due to changes in the contact size and hence resistance of the heater, as well as in a possible electrical contact resistance between the heater and the phase-change layer. Besides, changes in the out-of-plane resistivity of the SL layer from one device to another could add a contribution in the case of as-fabricated and 300 °C annealed devices. As shown by the analysis of the HAADF-STEM images (Figure S2, Supporting Information), the block stacking and the location of bilayer defects are different along vertical lines located 10 to 15 nm apart. However, the fact that an appreciable variability of R–I curves is still observed for devices annealed at 450 °C, for which the contribution of the SL is expected to be the same in all memory cells, could suggest that technological issues are dominant. The median RESET current (I_{RESET}), defined as the minimum current required to reach the high resistance state, decreases from ≈2.6 mA in as-fabricated devices to ≈2.25 mA after annealing the devices at 415 °C while the median resistance of the initial state R_0 increases by a factor ≈12 and the resistance of the RESET state by a factor ≈5. Additional annealing at 450 °C further reduces I_{RESET} to ≈1.9 mA without changing significantly the initial and RESET resistances. As shown in Figure S4 (Supporting Information), we checked for devices annealed at 415 °C + 450 °C that the R–I curves measured during the first programming sequence can be reproduced in successive cycles. This aimed to confirm that no forming operation was required in our SL devices and that the first cycle is representative

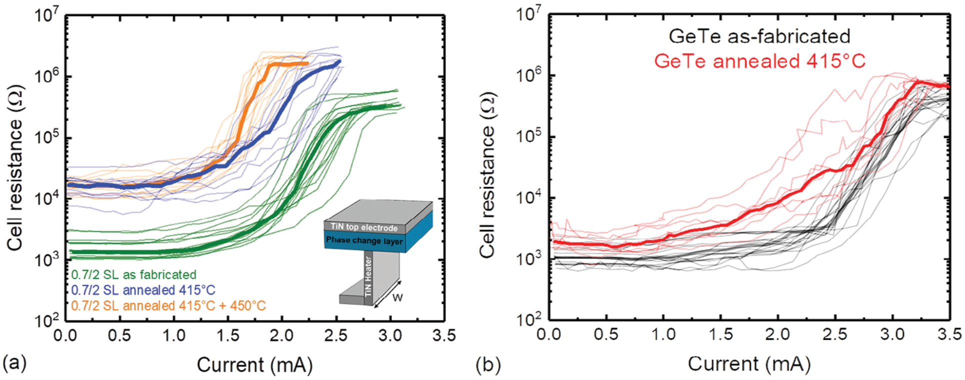

Figure 4. a) *R–I* curves (staircase sequence) measured on 0.7/2 SL devices in the as-fabricated state (green curves), annealed at 415 °C for 1 h (blue curves) and annealed at 415 °C for 1 h + 450 °C for 15 min (orange curves). b) *R–I* curves measured on GeTe devices in the as-fabricated state (black curves) and annealed at 415 °C for 1 h (red curves). For each type of device, the median *R–I* curves are shown as bold lines. A schematic drawing, not to scale, of a "wall-structure" memory cell is shown in (a) (W = 200 nm).

of the SL device properties. *R–I* curves obtained on as-fabricated reference devices incorporating polycrystalline GeTe and on GeTe devices annealed at 415 °C for 1 h are shown in Figure 4b for comparison. The architecture of these devices is the same as that of the 0.7/2 SL devices. As previously reported in reference,[9] the median RESET current of as-fabricated GeTe devices (≈3.25 mA) is larger than that of as-fabricated 0.7/2 SL devices. Annealing the GeTe devices at 415 °C results in only a slight increase in initial resistance and RESET resistances by a factor ≈2, while the RESET current remains almost unchanged.

A comparison of the results obtained on GeTe and SL devices allows us to clarify the origin of the annealing-induced changes in SL devices. A decrease in RESET current is induced by annealing in SL devices, but not in GeTe devices. Thus, it does not result from thermal treatment-induced changes in device architecture but must be attributed to changes in the properties of the SL layer. The same conclusion applies to the strong annealing-induced increase in initial resistance R_0 observed in SL devices. R_0 includes the out-of-plane resistance of the phase-change layer, the resistance of the heater, and any contact resistances. R_0 values in the range [10–30 kΩ] are measured in 0.7/2 SL devices annealed at 415 °C or 450 °C whereas the R_0 values in as-fabricated GeTe and 0.7/2 SL devices are similar, in the range [700–3000 Ω]. Annealing GeTe devices increases the median R_0 value by a factor of ≈2. This factor includes possible changes in the properties of the polycrystalline GeTe film and in the heater or contact resistance after annealing but is much weaker than that measured in SL-based devices after annealing. Thus, the large R_0 values measured in annealed 0.7/2 SL devices can be attributed to a dominant contribution of the out-of-plane resistance of the annealed SL layer. The fact that in annealed SL devices, the main contribution to the resistance in the SET state comes from the phase-change layer leads to an improved thermal efficiency since it allows to confine heat dissipation mostly in the phase-change layer, and not in the heater, at the beginning of the RESET process. As we showed in reference[9] for a 0.7/8 SL device, after switching to the HRS, the amorphous dome extends up to the top electrode throughout the entire thickness of the SL film. Thus, by opposite to conventional mushroom cells incorporating GST polycrystalline alloys, the amorphous volume is not confined close to the bottom electrode contact, evidencing that the hot spot due to Joule heating effect during the programming pulse is delocalized within the SL layer, instead of being localized at the interface between the bottom electrode and the phase change layer. This is due to the high out-of-plane electrical resistance of the SL, compared to that of the bottom heater, when a low density of structural defects is present, as is the case for a 0.7/8 SL device in reference[9] or, in the present study, for a defect-free 0.7/2 SL device after appropriate annealing.

4. Discussion

The results presented above and summarized in **Table 1** allow us to establish correlations between annealing-induced changes in 0.7/2 SL device characteristics and structural changes observed by XRD and HAADF-STEM imaging on 0.7/2 SL films deposited on SiO_2. The fraction of blocks of 7 atomic planes given in Table 1 is deduced from the analysis presented in Figure S2 (Supporting Information) where block stacking is investigated in STEM-HAADF images of SL films along vertical lines perpendicular to the atomic planes. Except for the film annealed at 450 °C, the stacking depends on the location of the line in the image due to the presence of many bilayer defects. Thus, in each image, block stacking is analyzed along three vertical lines ≈10 to 15 nm apart. In the case of the as-deposited 0.7/2 SL, the fluctuations from one line to another are so great that no reliable analysis could be carried out. Although the analysis provided in Figure S2 (Supporting Information) should be considered qualitative, it allows us to estimate the number of blocks of 5, 7, 9, and >9 planes along each line. Note that the number of blocks along a line, and hence the number of pseudo vdW gaps, is almost constant in all annealed films, equal to ≈33. The fraction of blocks of 7 atomic planes (average over the three lines in the image) clearly increases from ≈41% after annealing at 300 °C to ≈63% after annealing at 415 °C. After annealing at 450 °C, the SL is composed of over 97% $Ge_1Sb_2Te_4$ blocks.

The main conclusion of the present work is that the transformation of a 0.7/2 SL with a high block disorder into an out-of-plane oriented $Ge_1Sb_2Te_4$ phase with almost no block disorder leads to improved device properties. The higher the

Table 1. Summary of annealing-induced changes in 0.7/2 SL device characteristics (median initial resistance R_0 and median RESET current) and structural changes observed by XRD and HAADF-STEM imaging on SL films deposited on SiO_2. The fraction of blocks of 7 atomic planes is deduced from the analysis of STEM-HAADF images as detailed in Figure S2 (Supporting Information).

Sample	FWHM rocking curve [°]	c parameter [nm]	Lateral grain size [nm]	Fraction of blocks of 7 atomic planes	R_0 Median [Ω]	I_{RESET} Median [mA]
As-deposited film (at 250 °C)	5.2 ± 0.3	–	[30–120]	–	–	–
Film annealed at 300 °C *Devices as-fabricated*	5.2 ± 0.3	–	[30–120]	41%	*≈1370*	*2.6 ± 0.1*
Film annealed at 300 + 415 °C *Devices annealed at 300 + 415 °C*	1.25 ± 0.08	4.095 ± 0.003	[150–800]	63%	*≈16500*	*2.25 ± 0.1*
Film annealed at 300+415+450 °C *Devices annealed at 300+415+450 °C*	1.14 ± 0.08	4.095 ± 0.003	[250–1200]	97%	*≈16 500*	*1.9 ± 0.05*

structural order, the lower the RESET current. A reduction in the RESET current is also achieved by increasing the thickness of the Sb_2Te_3 layers in SL devices, thereby reducing block disorder.[9] The present results show that the integration of an SL structure is not a necessary step to reduce the RESET current compared with devices incorporating polycrystalline phase-change alloys such as GeTe or cubic $Ge_2Sb_2Te_5$. The integration of an out-of-plane oriented $Ge_1Sb_2Te_4$ phase achieves the goal of reducing the RESET current and should offer several advantages over SL devices for large-scale integration. Reduction in device-to-device variability is expected thanks to the elimination of the block stacking disorder inherent in the SL structure and inevitably different from device-to-device. In addition, the large lateral size of the crystallites in the out-of-plane $Ge_1Sb_2Te_4$ phase limits the likelihood of having a grain boundary located above the heating element.

The reduced RESET programming energy of devices incorporating an out-of-plane oriented $Ge_1Sb_2Te_4$ phase must be attributed to its electronic and thermal transport properties. As shown above, the increase in the initial resistance by a factor of ≈12 after annealing at 415 or 450 °C reflects an increase in the out-of-plane resistance of the phase-change layer. It can be concluded that the out-of-plane resistivity of the rhombohedral $Ge_1Sb_2Te_4$ phase is higher than that of the 0.7/2 SL in as-fabricated devices. Further information on annealing-induced changes in electronic transport is provided by measuring the in-plane resistivity of as-deposited and annealed 0.7/2 SL films as a function of temperature (**Figure 5**). Samples were annealed under the same conditions as those used for structural characterization before sheet resistance measurements were carried out. In the temperature range studied [50–200 °C], resistivity increases with temperature, and the resistivity curves measured after various annealing treatments are parallel. The extrapolated room-temperature value of the in-plane resistivity of the as-deposited 0.7/2 SL (10^{-3} Ω cm) is close to 5.5×10^{-4} Ω cm, measured on a GeTe(1 nm)/Sb_2Te_3(3 nm) SL deposited by MBE in reference,[32] and to 5.8×10^{-4} Ω cm, measured on a GeTe(1 nm)/Sb_2Te_3(4 nm) SL deposited by sputtering in reference.[31] Annealing the as-deposited 0.7/2 SL sample at 300 °C reduces its in-plane resistivity at 50 °C by a factor of 1.4. Annealing at 415 °C produces a reduction in resistivity by a factor of 1.9. Further annealing at 450 °C has no additional effect on resistivity, showing that residual block disorder and bilayer defects present in the 415 °C-annealed film (Figure 2c) have no significant impact on in-plane resistivity. The resistivity curve of another piece of the 0.7/2 SL film annealed at 450 °C for 1 h is exactly the same as those shown in Figure 5 for 415 °C or 450 °C annealed films, indicating good reproducibility of the measurements. The approximately 1.4-fold decrease in in-plane resistivity between 300 and 415 °C annealed films is a small effect compared to the increase in out-of-plane resistivity deduced from the change in initial resistance between as-fabricated and 415 °C annealed devices. Thus, the transformation of 0.7/2 SL into an out-of-plane oriented rhombohedral $Ge_1Sb_2Te_4$ phase leads to an increase in out-of-plane resistivity and a decrease in in-plane resistivity and hence to an increase in the anisotropy of electronic transport. In the literature, anisotropic electronic transport has been studied in single crystals of the rhombohedral $Ge_1Sb_2Te_4$ phase.[40,41] Their room temperature in-plane resistivity (≈2.2×10^{-4} Ω cm) is close to the value measured here (4×10^{-4} Ω cm) for the 0.7/2 SL films annealed at 415 or 450 °C. This result shows that the grain boundaries between $Ge_1Sb_2Te_4$ crystallites differing by their in-plane orientation have no significant impact on the measured in-plane resistivity in annealed 0.7/2 films, as could be expected from their large lateral size (Figure 3c,d). The out-of-plane resistivity of single crystals is found larger by a factor of 2.4 or 2.2 than the in-plane resistivity. A much larger anisotropy is expected from

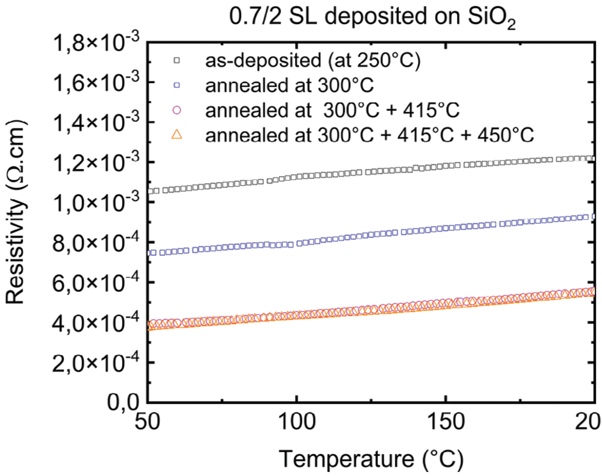

Figure 5. In-plane resistivity as a function of increasing temperature for 0.7/2 SL films in the pristine state (as-deposited at 250 °C) and after various annealing treatments. The resistivity curves of samples annealed at 415 °C and above are identical.

the analysis presented above in the case of a $Ge_1Sb_2Te_4$ layer in devices. A qualitative explanation could be that the out-of-plane transport is highly sensitive to the concentration of bilayer defects. A large amount of such defects could create conduction paths bridging the pseudo vdW gaps. A correlated study of bilayer defects and transport properties in single crystals and thin films would be necessary to quantify this assertion.

5. Conclusion

In conclusion, the RESET current of 0.7/2 SL devices can be significantly reduced by transforming the 0.7/2 SL by annealing into an out-of-plane oriented $Ge_1Sb_2Te_4$ layer. The results presented above show that a reduction in RESET current, compared with devices based on polycrystalline phase-change alloys, does not require any specific feature of the SL structure, widely invoked in the literature, but can be achieved in devices integrating an out-of-plane oriented $Ge_1Sb_2Te_4$ layer. The above conclusion is promising for the industrial integration of these films.[42] In a very recent paper,[43] Cohen et al. showed that PCM devices based on homostructure GST (*c*-axis oriented GST film with a fiber texture), using the same thin $TiTe_2$ seed layer to orient the growth, showed similar characteristics independently of the Ge-Sb-Te composition (GST 225 124 or 147). As mentioned in the introduction, the wide interest that arose from $GeTe/Sb_2Te_3$ SLs in the literature came from the reduction in RESET current concerning devices incorporating a $Ge_2Sb_2Te_5$ alloy. However, this conclusion was deduced from measurements on test devices similar to those used in the present work for which the thermal budget applied to the SL is moderate. The question of whether the reduced RESET current in SL devices would be maintained after back-end-of-the-line integration (BEOL) in industrial microelectronic devices, although already raised in reference,[17] has not been answered yet. The present results show that heating a 0.7/2 SL is not detrimental and, in fact, further reduces the RESET current.

6. Experimental Section

SL Deposition Method: SLs were deposited at 250 °C by magnetron sputtering in an industrial cluster tool by alternating sputtering of a GeTe target and co-sputtering of Te and Sb_2Te_3 targets. During deposition, the Ar pressure in the chamber was 0.11 Pa. As shown in the previous works, co-sputtering allows the deposition of stoichiometric Sb_2Te_3 layers and SLs.[18,44] The thickness of the deposited GeTe layers was equal to 0.7 nm (corresponding to 2 Ge and 2 Te planes). The thickness of the deposited Sb_2Te_3 layers was chosen to contain 2 QLs. The obtained SL is a $[(GeTe)_2(Sb_2Te_3)_2]_p$ stack, with p the number of periods, labeled 0.7/2 since the thickness of the deposited Sb_2Te_3 layer is close to 2 nm. Deposition times were determined on the basis of a preliminary study of a series of GeTe and Sb_2Te_3 thin films of varying thickness deposited under the same conditions. Their thickness was measured by X-ray reflectivity to obtain deposition rates. Prior to the SL deposition, a 5 nm thick Sb_2Te_3 seed layer was deposited at ≈250 °C. Under Te-rich sputtering conditions, such as those provided by co-sputtering Te and Sb_2Te_3 targets, a well out-of-plane oriented Sb_2Te_3 layer grows on any substrate, including SiO_2, thanks to the formation, at the substrate surface, of a Te-rich layer separated from the first Sb_2Te_3 QL by a true van der Waals gap.[13,44] The overall nominal composition of the film is Ge 13.75 at%, Sb 29 at%, Te 57.25 at%, including the Sb_2Te_3 seed layer, which is close to the composition of the $Ge_1Sb_2Te_4$ rhombohedral phase on the GeTe-Sb_2Te_3 pseudo-binary tie line in the Ge-Sb-Te phase diagram.[24]

Device Fabrication: A $[(GeTe)_2(Sb_2Te_3)_2]_{12}$ SL (nominal thickness 38 nm, including the Sb_2Te_3 seed layer) was integrated into test vehicle PCM devices on a 200 mm-diameter Si wafer during a first deposition campaign.[9] In a memory cell, the SL layer is deposited on a metallic TiN heater and on a SiN_x dielectric layer surrounding the heater. The SL layer is covered by a planar TiN top electrode. The memory cell has a "wall structure" in which the TiN heater, acting as a bottom electrode, is L-shaped (schematic drawing not to scale in Figure 4a). The length of the heater W is equal to 200 nm. After deposition at ≈250 °C, the SL layer was subjected to a thermal budget of ≈300 °C for 15 min during the final integration process of the test vehicle PCM devices. It is shown by STEM imaging of PCM devices that this integration process does not damage the SL structure.[9] Test vehicle PCM devices with the same architecture integrating a 40 nm-thick polycrystalline GeTe layer were also fabricated for reference purposes. The GeTe layer was deposited amorphous at room temperature, and then crystallized during the final stages of integration into PCM devices. The Si wafer contains numerous chips. Each chip contains sets of 20 devices with a given heater geometry. After fabrication, chips were cleaved from the 0.7/2 SL and GeTe wafers, and then subjected to various annealing treatments (more information in the Supporting Information).

SL Film: For structural characterization and sheet resistance measurements, a $[(GeTe)_2(Sb_2Te_3)_2]_{46}$ SL was deposited on a 500 nm-thick thermal SiO_2 layer on a Si (100) wafer (200 mm diameter) during a second deposition campaign. After deposition, the film was coated in situ by a 10 nm thick SiN_x layer to protect it from oxidation. The SL thickness was measured by X-ray reflectivity and found to be in line with the expected value (130 nm, taking into account the Sb_2Te_3 seed layer). The composition of the as-deposited film measured by wavelength dispersive X-ray fluorescence (WDXRF) is Ge 13.1 at%, Sb 28.5 at%, Te 58.4 at%, in qualitative agreement with the nominal composition. One observes a small excess of Te, correlated to a small deficiency in Ge and Sb. However, absolute composition values measured by WDXRF are affected by possible systematic errors caused by the calibration procedure that are difficult to estimate.[18] The fact that the formation of a $Ge_1Sb_2Te_4$ phase is observed by XRD and HAADF-STEM imaging in samples annealed at 415 °C and above proves that the composition of the deposited SL film was close to the targeted one. Pieces of the film, cleaved at the mid-radius of the wafer, were subjected to various annealing treatments (more information in the Supporting Information) by heating under a high N_2 flow, and then used for structural characterizations and sheet resistance measurements. The annealing treatments applied to 0.7/2 SL films and devices are identical but SL films and SL in devices were deposited in distinct deposition campaigns. Slight structural differences between the SLs are unavoidable. In particular, bilayer defects are present in an SL film annealed at 415 °C and not in a film annealed at 450 °C, while the two kinds of devices have similar R_0 values.

X-Ray Diffraction Measurements: Out-of-plane diffraction patterns were measured at room temperature using a diffractometer (Cu K_α radiation) in the Bragg-Brentano geometry (θ-2θ with 2θ the angle of the detector with respect to the incident beam). Rocking curves (ω scans at a fixed 2θ value, with ω the incidence angle) were also measured on selected diffraction peaks.

Scanning Transmission Electron Microscopy: Electron transparent foils were prepared by Ga^+ focused ion beam (FIB) milling using a ThermoFisher Scientific (TFS) STRATA 400 machine. A conventional 30 kV voltage at medium current was first applied and then a low energy beam (voltage range 5–8 kV) was used in order to reduce the surface damage on each free side of the foil. To maximize the relevance of comparisons between samples, it was ensured that all foils had almost the same thickness (≈80 nm). High-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) images were acquired on a probe Cs-corrected FEI Titan Themis microscope operating at 200 kV. In order to avoid any damage caused by electron irradiation, the HAADF images were obtained using a low current beam below 30 pA. Precession Electron Diffraction (PED) mapping, also known as Automated Crystal Orientation Mapping (ACOM),[45] was acquired to examine the micro-texture of the films. PED experiments were performed on a Jeol NeoARM200F microscope operating at 200 kV and equipped with the NanoMEGAS ASTAR system. The microscope was set to NBD-L mode, i.e., nanobeam diffraction large, with a spot size of 1 nm, and using a 10 µm condenser aperture. Diffraction patterns (consisting of 512 × 512 pixel images) were acquired on a Stingray CCD camera. The camera length was precisely calibrated using the diffraction patterns from the silicon substrate. Diffraction patterns were acquired using a 30 ms integration time. Mappings were acquired with a 5 nm pixel size.

Sheet Resistance Versus Temperature: The sheet resistance R_s of pieces (size 2 cm × 2 cm) of 0.7/2 SL film was measured using the four-point probe technique, from room temperature to 200 °C. Samples were heated and cooled at a rate of 10 °C min^{-1} under a high flow of N_2 to prevent oxidation. The maximum temperature was limited to 200 °C in order to prevent structural changes during the experiment. No significant differences were observed between the resistivity curves measured during cooling and heating. The in-plane resistivity is equal to R_s t, with t is the film thickness.

Electrical Characterization of PCM Devices: The *R–I* curves (with *R* the resistance of a memory cell and *I* the current flowing during a programming pulse) were obtained by applying successive programming pulses of increasing voltage (staircase sequence, voltage step 0.1 V). The staircase sequence was stopped when the cell resistance reached a constant high resistance value (RESET state). The pulse duration was set at 300 ns, with a rise and fall time of 10 ns. This choice was made in order to use a programming scheme similar to that of standard PCM devices. To limit the current flowing through a memory cell, a 1 kΩ resistor was connected in series. Cell resistance was measured by applying a constant, low-voltage pulse (0.1 V) after each programming pulse. The 1 kΩ series resistance has been subtracted from the *R–I* curves shown in Figure 4. No forming pulse was applied before measuring the *R–I* curves due to proper preparation of the bottom electrode surface before the growth of SL.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

atomic structure, devices, phase-change memory, super-lattice, TEM

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[1] A. Sebastian, M. L. Gallo, G. W. Burr, S. Kim, M. BrightSky, E. Eleftheriou, *J. Appl. Phys.* **2018**, *124*, 111101.
[2] A. Sebastian, M. L. Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* **2020**, *15*, 529.
[3] *Phase Change Memory* (Ed.: A. Redaelli), Springer International Publishing, Cham, Switzerland, **2018**.
[4] P. Noé, C. Vallée, F. Hippert, F. Fillot, J.-Y. Raty, *Semicond. Sci. Technol.* **2018**, *33*, 013002.
[5] H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, K. E. Goodson, *Proceedings of the IEEE* **2010**, *98*, 2201.
[6] R. E. Simpson, P. Fons, A. V. Kolobov, T. Fukaya, M. Krbal, T. Yagi, J. Tominaga, *Nat. Nanotechnol.* **2011**, *6*, 501.
[7] N. Takaura, T. Ohyanagi, M. K. M. Tai, K. Akita, T. Morikawa, H. Shirakawa, M. Araidai, K. Shiraishi, Y. Saito, J. Tominaga, *in* IEEE International Electron Devices Meeting, San Francisco, CA, USA, **2014**, 29.2.1–29.2.4.
[8] M. Boniardi, J. E. Boschker, J. Momand, B. J. Kooi, A. Redaelli, R. Calarco, *Phys. Status Solidi RRL* **2019**, *13*, 1800634.
[9] D. Térébénec, N. Castellani, N. Bernier, V. Sever, P. Kowalczyk, M. Bernard, M.-C. Cyrille, N.-P. Tran, F. Hippert, P. Noé, *Phys. Status Solidi RRL* **2021**, *15*, 2000538.
[10] A. I. Khan, H. Kwon, M. E. Chen, M. Asheghi, H.-S. P. Wong, K. E. Goodson, E. Pop, *IEEE Electron Device Lett.* **2022**, *43*, 204.
[11] T. Chattopadhyay, J. X. Boucherle, H. G. von Schnering, *J. Phys. C: Solid State Phys.* **1987**, *20*, 1431.
[12] Y. Cheng, O. Cojocaru-Mirédin, J. Keutgen, Y. Yu, M. Küpers, M. Schumacher, P. Golub, J.-Y. Raty, R. Dronskowski, M. Wuttig, *Adv. Mater.* **2019**, *31*, 1904316.
[13] V. Sever, N. Bernier, D. Térébénec, C. Sabbione, J. Paterson, F. Castioni, P. Quéméré, A. Jannaud, J.-L. Rouvière, H. Roussel, J.-Y. Raty, F. Hippert, P. Noé, *Phys. Status Solidi RRL* **2024**, 2300402.
[14] X. Z. Kalikka, E. Dilcher, S. Wall, J. Li, R. E. Simpson, *Nat. Commun.* **2016**, *7*, 11983.
[15] J. Tominaga, A. V. Kolobov, P. Fons, T. Nakano, S. Murakami, *Adv. Mater. Interfaces* **2014**, *1*, 1300027.
[16] M. Tai, T. Ohyanagi, M. Kinoshita, T. Morikawa, K. Akita, S. Kato, H. Shirakawa, M. Araidai, K. Shiraishi, N. Takaura, in 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, **2014**, pp. 1–2.
[17] J. Momand, F. R. L. Lange, R. Wang, J. E. Boschker, M. A. Verheijen, R. Calarco, M. Wuttig, B. J. Kooi, *J. Mater. Res.* **2016**, *31*, 3115.
[18] P. Kowalczyk, F. Hippert, N. Bernier, C. Mocuta, C. Sabbione, W. Batista-Pessoa, P. Noé, *Small* **2018**, *14*, 1704514.
[19] F. d'Acapito, P. Kowalczyk, J.-Y. Raty, C. Sabbione, F. Hippert, P. Noé, *J. Phys. D: Appl. Phys.* **2020**, *53*, 404002.
[20] A. Lotnyk, I. Hilmi, U. Ross, B. Rauschenbach, *Nano Res.* **2018**, *11*,1676.
[21] A. Lotnyk, I. Hilmi, M. Behrens, B. Rauschenbach, *Appl. Surf. Sci.* **2021**, *536*, 147959.
[22] J. Momand, R. Wang, J. E. Boschker, M. A. Verheijen, R. Calarco, B. J. Kooi, *Nanoscale* **2015**, *7*, 19136.
[23] B. J. Kooi, J. Momand, *Phys. Status Solidi RRL* **2019**, *13*, 1800562.
[24] L. E. Shelimova, O. G. Karpinskii, V. S. Zemskov, P. P. Konstantinov, *Inorg. Mater.* **2000**, *36*, 235.
[25] H. Hardtdegen, S. Rieß, M. Schuck, K. Keller, P. Jost, H. Du, M. Bornhöfft, A. Schwedt, G. Mussler, M. vd Ahe, J. Mayer, G. Roth, D. Grützmacher, M. Mikulics, *J. of Alloys and Compounds* **2016**, *679*, 285.

[26] A. Lotnyk, U. Ross, S. Bernütz, E. Thelander, B. Rauschenbach, *Sci. Rep.* **2016**, *6*, 26724.
[27] T. Matsunaga, N. Yamada, Y. Kubota, *Acta Cryst. B* **2004**, *60*, 685.
[28] T. Matsunaga, N. Yamada, *Phys. Rev. B* **2004**, *69*, 104111.
[29] T. Matsunaga, R. Kojima, N. Yamada, K. Kifune, Y. Kubota, M. Takata, *App. Phys. Letters* **2007**, *90*, 161919.
[30] P. Urban, M. N. Schneider, L. Erra, S. Welzmiller, F. Fahrnbauer, O. Oeckler, *CrystEngComm* **2013**, *15*, 4823.
[31] H. Kwon, A. I. Khan, C. Perez, M. Asheghi, E. Pop, K. E. Goodson, *Nano Lett.* **2021**, *21*, 5984.
[32] S. Cecchi, E. Zallo, J. Momand, B. J. K. R. Wang, M. A. Verheijen, R. Calarco, *APL Mater.* **2017**, *5*, 026107.
[33] H. Hollermann, F. R. L. Lange, S. Jakobs, P. Kerres, M. Wuttig, *Phys. Status Solidi RRL* **2019**, *13*, 1800577.
[34] J. Momand, R. Wang, J. E. Boschker, M. A. Verheijen, R. Calarco, B. J. Kooi, *Nanoscale* **2017**, *9*, 8774.
[35] A. Lotnyk, U. Ross, T. Dankwort, I. Hilmi, L. Kienle, B. Rauschenbach, *Acta Mater.* **2017**, *141*, 92.
[36] J.-J. Wang, J. Wang, H. Du, L. Lu, P. C. Schmitz, J. Reindl, A. M. Mio, C.-L. Jia, E. Ma, R. Mazzarello, M. Wuttig, W. Zhang, *Chem. Mater.* **2018**, *30*, 4770.
[37] J.-J. Wang, H.-M. Zhang, X.-D. Wang, L. Lu, C. Jia, W. Zhang, R. Mazzarello, *Adv. Mater. Technol.* **2022**, *7*, 2200214.
[38] O. G. Karpinsky, L. E. Shelimova, M. A. Kretova, J.-P. Fleurial, *J. Alloys Compd.* **1998**, *268*, 112.
[39] J. E. Boschker, R. Calarco, *Advances in Physics:X* **2017**, *2*, 675.
[40] M. Frumar, L. Tichy, J. Horák, J. Klikorka, *Mat. Res. Bull.* **1972**, *7*, 1075.
[41] P. Chen, H. Wu, B. Zhang, Z. Zhou, S. Zheng, Y. H. L. Dai, D. Zhang, Y. Yan, K. Peng, G. Han, X. Lu, X. Zhou, G. Wang, *Adv. Funct. Mater.* **2023**, *33*, 2211281.
[42] D. Terebenec, P.-O. Noe (Commissariat à L'Energie Atomique et aux Energies Alternatives), Method for Manufacturing Phase Change Material, **2023**, FR3135161 (A1), EP4271166 (A1), US2024114806 (A1).
[43] G. M. Cohen, A. Majumdar, C.-W. Cheng, A. Ray, D. Piatek, L. Gignac, C. Lavoie, A. Grun, H.-Y. Cheng, Z.-L. Liu, H.-L. Lung, H. Miyazoe, R. L. Bruce, M. BrightSky, *Phys. Status Solidi RRL* **2024**, 2300426.
[44] F. Hippert, P. Kowalczyk, N. Bernier, C. Sabbione, X. Zucchi, D. Térébénec, C. Mocuta, P. Noé, *J. Phys. D: Appl. Phys.* **2020**, *53*, 154003.
[45] E. F. Rauch, J. Portillo, S. Nicolopoulos, D. Bultreys, S. Rouvimov, P. Moeck, *Zeitschrift Für Kristal* **2010**, *225*, 103.