# Hafnium Oxide-Based Ferroelectric Memories: Applications and Future Prospects

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## Abstract

This chapter provides a brief and concise overview of ferroelectric memories based on the hafnium-oxide. Ferroelectricity, discovered in Rochelle salt for the first time in 1920 by Joseph Valasek, has been with us for nearly a century but failed to get the attention other types of memories like charge-trapping flash, spin-based memory, or even resistive memories were getting. However, the discovery of better to say the *aha moment* of finding ferroelectricity in silicon hafnium oxide in 2007 entirely changed the paradigm. Hafnium oxide-based ferroelectric memories may be used as storage, synaptic, and high-density integration devices. This makes them a potential candidate for future memory technology, especially for reducing the performance metric between dynamic/static-random-access memory and external data storage. This article begins with an overview of the history and physics of ferroelectric materials before moving on to the many types of ferroelectric memory and their applications.

## 1 Introduction

Because of the striking resemblance in the hysteresis, ferroelectricity was named after Ferromagnetic, which was initially identified in 1921 in Rochelle salts. A ferroelectric material is a special group of non-linear dielectric that shows nonzero electrical polarization (two or more states of opposite polarities) even without applying an external electric field ($\xi_{ext}$), known as spontaneous polarization ($P_s$). $\xi_{ext}$ enables switching between these polarization states. In equilibrium, the ferroelectric (FE) materials usually feature non-centrosymmetric structures or broken symmetry. As a result, there is no elimination of generic/basis vectors by crystal symmetry. In the case of FE materials, the equilibrium state's vector attribute polarization exhibits re-orientable $P_s$. The structural genesis of ferroelectricity is frequently associated with the Lorenz or polarization catastrophes [1–3]. A crystal experiences a polarization catastrophe when the displacive transition of its constituent components causes the polarization, or any of its Fourier components, to grow beyond bound. The dielectric constant ($\epsilon$) and electronic polarizability are related by the Clausius-Mossotti relation, which may be expressed as [1]

$$\epsilon = \frac{1 + \frac{8\pi}{3}\sum N_i\alpha_i}{1 - \frac{4\pi}{3}\sum N_i\alpha_i} \tag{1}$$

The total polarizability of an ion of type "i", electronic and ionic, is $\alpha_i$, and the number of ions per unit volume is $N_i$. In the presence of an electric field, the prerequisite for polarization catastrophe, permitting finite polarization, is

$$1 = \frac{4\pi}{3}\sum N_i\alpha_i \tag{2}$$

As Charles Kittel stated, "In a polarization catastrophe, the local electric field caused by the ionic displacement is larger than the elastic restoring force, thereby giving an asymmetrical shift in the positions of the

ions. Higher-order restoring forces will limit the change to a finite displacement. The occurrence of ferroelectricity (and antiferroelectricity) in many perovskite-structure crystals suggests that this structure is favorably disposed to a displacive transition. Local field calculations clearly explain the reason for the favored position of this structure. $O^2$ ions do not have cubic surroundings, and local field factors are unusually large" [1].

Therefore, what happens to an FE crystal when $\xi_{ext}$ is applied? To understand this, we must understand the concept of "local electric field" ($\xi_{loc}$) in a lattice or an atom. The $\xi_{loc}$ of an atom in a crystal determines the dipole moment or the polarization of the atom, which is significantly different from the $\xi_{ext}$. $\xi_{loc}$ is the total electric field on an atom comprising an externally applied electric field and the electric field generated through the dipole moment originating from the arrangement of the lattice. The crystal's polarization can be expressed as the product of polarizability and local $\xi_{loc}$.

$$P = \sum N_j \alpha_j \xi_{loc}(j) \tag{3}$$

The Clausius-Mossotti related described in the equation:1 related $\epsilon$ with polarizability. $\epsilon$ is a parameter dependent on the crystal structure, whereas the polarizability is an atomic property. Now, what happens when the value of $\alpha$ increases in equation 1? The polarization gets bigger, and so does the local $\xi$. The relationship between $\xi_{loc}$ and the polarizability can be written as:

$$p_d = \alpha E_{loc} \tag{4}$$

$p_d$ is the dipole moment. Therefore, a bigger $\xi_{loc}$ will even polarize the atoms more, raising the value of $\alpha$ more. This feedback system causes the polarization to increase without the limit, whereas the crystal structure limits or locks the increases to a certain extent. As said by Feynmann "The 'runaway' condition occurs when N$\alpha$=3. The polarization does not become infinite, of course, because the proportionality between the induced moment and the electric field breaks down at high fields, so that our formulas are no longer correct. What happens is that the lattice gets 'locked in' with a high, self-generated, internal polarization" [2]. Considerable solid FE materials also exhibit a sizable ionic polarization, which is thought to be caused by positive ions with considerable lattice movement and electronic polarization. The ion travels a certain distance before jamming and stopping because the lattice cannot withstand large movements. However, this leaves a persistent dipole moment in the crystal cell, and thus, the FE property is engendered.

## 1.1 History of Ferroelectricity

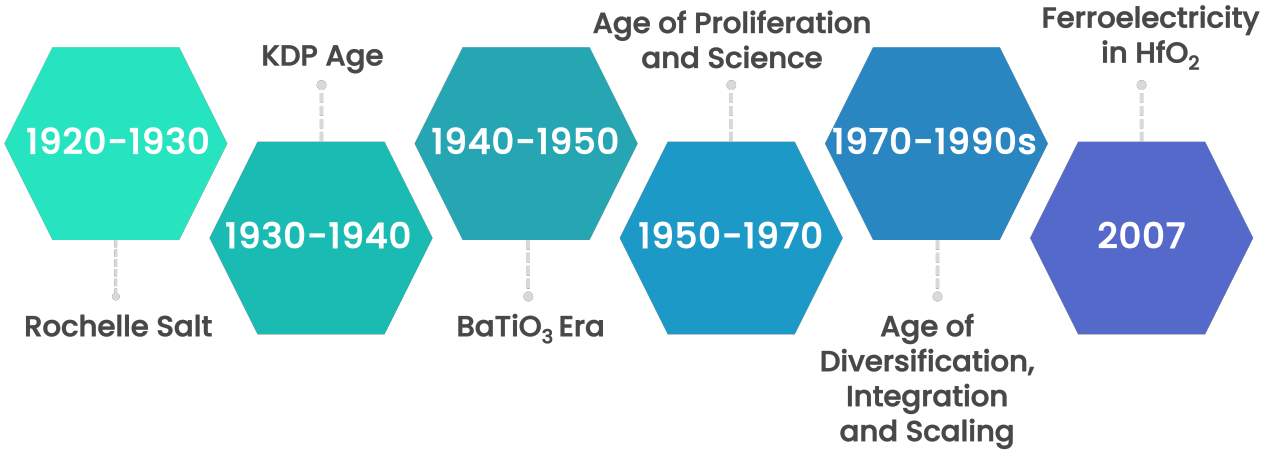


Figure 1: A glimpse of major landmarks in the findings and development of ferroelectricity and ferroelectric materials

In La Rochelle, a little but significant city on France's southwest coast, everything started with salt. Jehan Seignette succeeded his father in running a pharmacy. Then, his younger brother Elie inherited his father's business, while his son Pierre, born in 1623, studied medicine at the University of Montpellier. Dr. Seignette advised his brother to either develop or find some mineral medications. Even while "mineralia" had been used in eastern nations to treat a variety of illnesses since 2000 B.C., at the time, pharmacy in Europe mainly included the extraction of plants and the distillation of essences [4].

After much effort, Elie created a salt in 1665 that he named "sel polychreste," which is derived from a Greek word, which means a salt with several uses. The physical attributes of Rochelle salt started to spark curiosity almost two hundred years after its discovery, in the nineteenth century. Although Rochelle Salt was one of

the crystals in which David Brewster had first noticed the phenomena of pyroelectricity in 1824, the brothers Pierre and Paul-Jacques Curie's 1880 investigations may have been the first to be conducted methodically. In addition to adequately identifying Rochelle Salt and several other crystals as piezoelectric, this seminal study demonstrated the existence of the piezoelectric effect. Additionally, they discovered that Rochelle salt was significantly more active than all the other crystals they looked into, including quartz. However, they missed the intriguing dielectric properties of Rochelle salt [4–8].

Petrus Josephus Wilhelmus Debye, a Professor of Theoretical Physics at the University of Zurich, hypothesized that some molecules contain a permanent electric dipole moment, similar to the magnetic moment of paramagnetic material atoms. Debye arrived at an additional conclusion. He claims that the $\epsilon$ reaches infinity at a crucial temperature. He thus suggested that this temperature be the equivalent of a ferromagnet's Curie temperature. Even without an electric field, a permanent dielectric polarization should be anticipated for temperatures below the curie temperature. To his knowledge, he said that no such occurrence had before been noted. Ferroelectricity's fundamental characteristic was predicted. Erwin Schrödinger went one step further in his "Habilitations-Schrift", which he submitted to the University of Vienna around the end of 1912, the same year that Debye released his "Vorläufige Mitteilung". He attempted to expand Debye's basic concept to solids and added more details. Schrödinger reasoned that all solids should turn "ferroelektrisch" at a low enough temperature if this could be accomplished. Schrödinger used the word ferroelectric or ferroelectricity as early as 1912 [9].

Joseph Valasek was another important figure in the early Rochelle Salt era. In April 1920, Joseph Valasek gave a paper presentation on "Piezoelectric and allied Phenomena in Rochelle salt" at the American Physical Society meeting in Washington [8]. He said "Electric Hysteresis in Rochelle Salt.— On the doublet theory of dielectric action, the dielectric displacement D, electric intensity E, and the polarization P are analogous to B, H, and I in the case of magnetism. Rochelle salt shows an electric hysteresis in P analogous to the magnetic hysteresis in the case of iron. The loops obtained are displaced from the origin by an amount that measures the permanent polarization in the natural state. The moment per unit volume in the natural state is of the order of 5o e.s.u. /cm. '" [10].

The name Paul Scherrer comes into the scenario after Schrödinger and Valasek. He and his pupil Georg Busch perused the still-scarce literature. They stumbled onto a paper written by Gert Steulmann of the Dresden-based "Institut für allgemeine Elektrotechnik" of the "Technische Hochschule". $K_3PO_4$, $K_2HPO_4$, and $KH_2PO_4$ were among the potassium salts whose average value of $\epsilon$ were determined by immersion. For the first two salts, rather typical values of 7.75 and 9.05 were noted; nevertheless, a value greater than 30 was discovered for $KH_2PO_4$. This was unexpected, given the orthorhombic symmetry of potassium-dihydrogen phosphate. This confirmed Busch's hypothesis that ferroelectricity may be caused by mobile hydrogen atoms rather than water molecules, which was his supervisor's theory. These theories were validated when Busch and Scherrer discovered early in March 1935 that $KH_2PO_4$ was ferroelectric, with a critical temperature of around 123 K. [11]

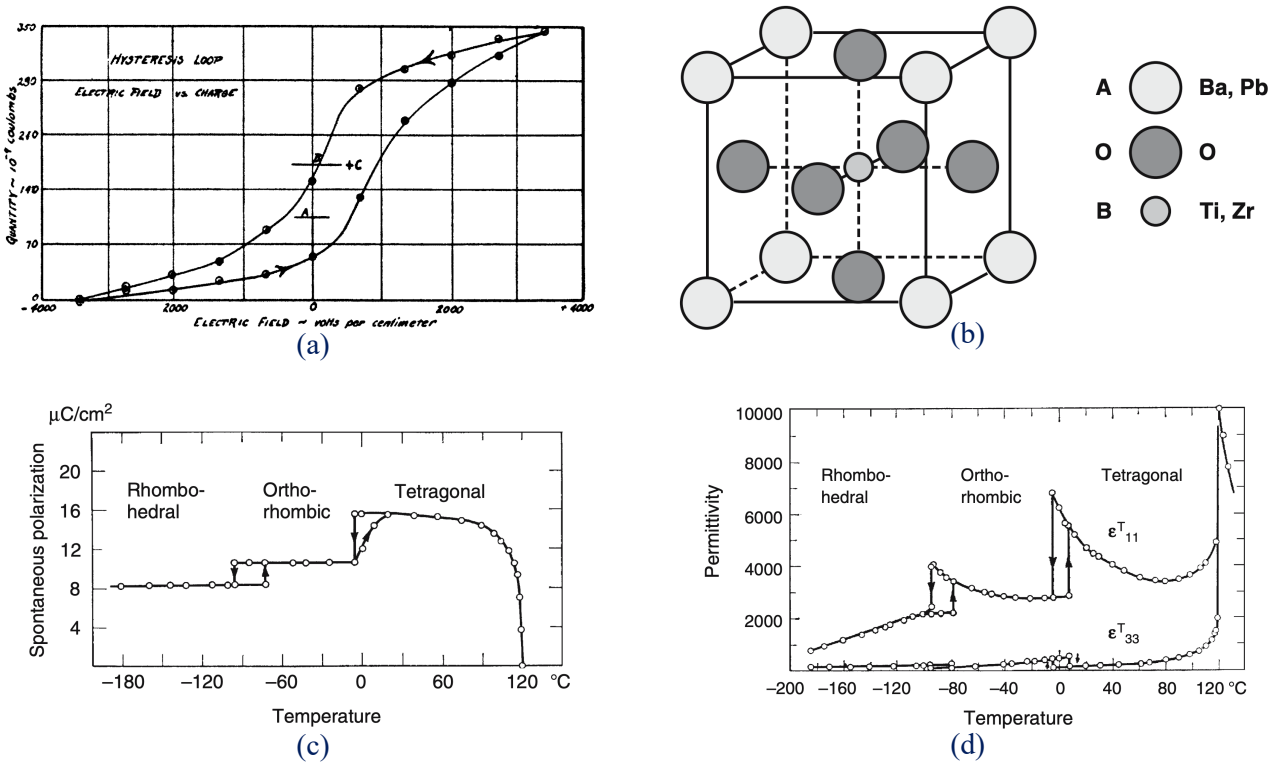


Figure 2: (a). First published hysteresis curve of FE materials. (b). Crystal structures of $BaTiO_3$. (c,d). Spontaneous polarization and permittivity relationship to curie temperatures. Figures reproduced with permission from [8, 12]

The first artificial perovskite FE material, barium titanate, or $BaTiO_3$, was found in the US, Russia, and Japan between 1942 and 1944. [12]. Doping experiments of titanium oxide ($TiO_2$) with barium-oxide ($BaO$) resulted in ceramic materials with improved dielectric permittivities, which formed the basis for the first reports. Thurnmaurer and Deaderick of the American Lava Corporation began producing mixed oxides in 1947 when U.S. Patent No. 2,429,588 was filed. Measurements at the "Erie Resistor Company" found extraordinary permittivities, with the value of $\epsilon \geq 1000$—ten times higher than any other known ceramic, such as $TiO_2$ ($\epsilon_r$=110) [13]. The finding that ferroelectricity might exist in simple oxide materials without being connected with hydrogen bonding was a significant step forward, leading to the discovery of ferroelectricity in $BaTiO_3$ ceramics. These materials' most essential theoretical foundations may be explored owing to the simplicity of inquiry afforded by the structure of $BaTiO_3$, which drew multiple studies to conduct x-ray diffraction (XRD) examinations of the structural alterations occurring during phase transitions. In 1951, A.F. Devonshire developed a phenomenological model of ferroelectrics based on the structural, thermal, and electromechanical properties of $BaTiO_3$ [14]. The most impactful and practical resource for understanding the physics of ferroelectrics remains the Landau-Devonshire-Ginzberg Theory.

$BaTiO_3$, the first ferroelectric based on oxide, has been one of the most researched materials in the history of ferroelectricity before 2006. This finding of ferroelectricity in $BaTiO_3$ ceramics was of utmost significance from both academic and production points of view. Helen D. Megaw (1945) in the United Kingdom gave the first comprehensive description of the crystal structure of $BaTiO_3$ in the high-temperature ferroelectric phase, and Miyake and Ueda's (1946) work shortly followed [15,16]. At regular room temperatures, the ferroelectric phase is tetragonal, with titanium and oxygen ions rearranging to create a spontaneous polarization. Subsequent research by Kay and Vousden (1949) revealed that $BaTiO_3$ has a sequence of ferroelectric-ferroelectric transitions at 5°C and –90°C, respectively, from orthorhombic to rhombohedral (R3m) and tetragonal (P4mm) to orthorhombic (Bmm2) [17].

Given the widespread success of the straightforward $BaTiO_3$-based ceramic transducer in the early 1950s, it made sense to look into alternative ferroelectric perovskite compounds for possible applications. In Japan, Shirane and Takeda, Shirane et al., and Sawaguchi conducted some of the very early fundamental work on pure $PbTi0_3$ and on the $PbTi0_3 : PbZr0_3$ solid solution system, which established the applicable high Curie temperature of lead zirconate and the outline of the phase diagram for this system [18]. Egerton and Dillon later showed a morphotropic boundary in the $NaNbO_3 : KNb0_3$ solid solution system at Bell Laboratories and piezoelectrics with compositions close to the $K_{O.5}Na_{0.5} : Nb0_3$ boundary were nevertheless hot-pressed for specific purposes by Bausch & Lomb [19].

Due to the wide range of uses ferroelectricity has from the nanoscale to the macroscopic scale, what was once a specialized area of study has expanded tremendously over the past century, with over 20,000 research articles published on the subject. The discovery of ferroelectricity in hafnium oxide in 2011 revolutionized the research and application related to it. Tim Böscke reported the presence of ferroelectricity in hafnium oxide [20]. 10 nm thick $HfO_2$ films doped with less than 4% $SiO_2$ crystallize in a monoclinic/tetragonal/orthorhombic phase combination in the presence of encapsulation shows ferroelectricity after annealing. $HfO_2$, a popular high-k material introduced in CMOS process flow, has an energy gap of around 5.3–5.7 eV, elastic modules of $\geq$200GPa, and a relative dielectric constant of around 17. Quintessentially, the most stable form of $HfO_2$ is the monoclinic structure. However, the ferroelectricity in $HfO_2$ results from a meta-stable polar orthorhombic phase, while the monoclinic or tetragonal phase shows no spontaneous polarization [21–34].

Ferroelectric behavior has even been discovered in biology; it may be observed, for instance, in amino acids and the pig aortic artery wall. It is also possible to create sensors with ferroelectrics that mimic various human "multifunctional sensory systems". So far, the best five applications of FE are as follow:

1. Storage systems.
2. Night-vision technology development system.
3. Ultrasound for medical purposes and underwater acoustics.
4. Actuators.
5. Energy harvesting.

## 2 Ferroelectricity in Hafnium Oxide

The Qimonda memory company's research and development team found the ferroelectricity in $HfO_2$ in 2007 [35] while examining materials with high-k for DRAM applications [20]. For several reasons, ferroelectricity in nanoscale $HfO_2$ films was considered a remarkable phenomenon beyond the scientific community's trivial explanation [36, 37]. It should be noted that before 2007, the polymorphs of $HfO_2$ were considered to have only a centrosymmetric crystal structure, unlike the other ferroelectric thin films with non-centrosymmetric structures. HKMG technology uses gate oxides with a higher k value than typical oxides like silicon oxide ($SiO_2$) or silicon oxynitride ($SiON$). With a permittivity about ten times higher than $SiO_2$ and potential applications as a resistive memory and in MOSFETs [38–52], $HfO_2$ was already a well-established material in the CMOS platform line. It has been utilized and is still used at most advanced CMOS technology nodes.

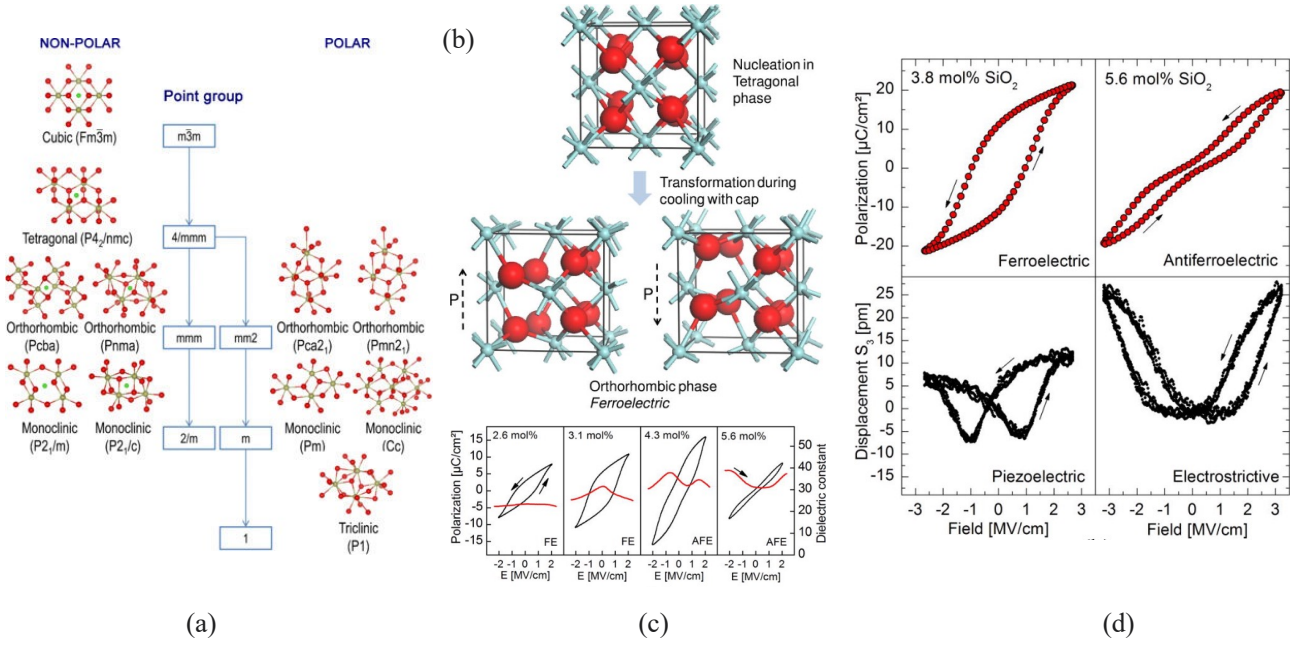


Figure 3: (a). Crystal structure variants of hafnium oxides. (b). Evolution of polar ferroelectric phase during thermal processing. (c). Polarization and switching current response of ferroelectric material to an $\xi_{ext}$ as a function of dopant concentration. [20, 36].

$HfO_2$ films are promising for single transistor FeFET devices, one transistor-one capacitor-based (FeMFETs), and other nanoscale FE devices. Second, $HfO_2$'s straightforward chemistry facilitates theoretical research, such as ab initio simulations, and lessens its susceptibility to several perturbing effects during the CMOS process, especially during multicomponent material-based thin film deposition processes. They also contain strong bonding between O and Hf and a high bandgap, which can help reduce leakage current and reliability issues frequently seen in perovskite ferroelectric. Despite significant advances in the underlying knowledge and device performance of $HfO_2$ thin films (which are polycrystalline), some limitations remain. First, $HfO_2$ films exhibit strong ferroelectricity, which is rare for perovskite equivalents, even at sample thicknesses of less than 5 nm. Despite several macroscopic trials, the microscopic process stabilizing the ferroelectric phase via the aforementioned components is barely understood. Second, the polycrystalline features of $HfO_2$ films—specifically, non-ferroelectric phases and grain boundaries—are detrimental to their ferroelectricity, engendering the statistical non-uniformity in ferroelectric characteristics and device instability. Apart from this, the $P^r$ of a pristine film increases with electric cycling, which is known by the "wake-up" process. We must understand these three crucial device-related challenges [53–55].

Moreover, the build-up of oxygen vacancies at grain boundaries creates a persistent conduction route that, in turn, causes device wear. Consequently, to precisely control the FE properties in $HfO_2$ films, systematic studies of $HfO_2$ thin films (with ferroelectricity) are required for microstructural characterization and microstructure-ferroelectric property investigation. This has been demonstrated by both fundamental research and real-world applications. The microstructures of ferroelectric materials, influenced by dopants, film thickness, thermal expansion, and epitaxial strain, are primarily responsible for their macroscopic performance. Ferroelectric $HfO_2$ materials' mechanical, electrical, electromechanical, and thermoelectric qualities are also essential for their device applications. These characteristics fluctuate in response to embedded microstructure modifications. Consequently, to comprehend their structure-property relationships, observing the related microstructural development under diverse growth factors and external stimuli is necessary.

The polymorphs of bulk $HfO_2$ crystals vary based on the temperature and pressure. At ambient temperature and air pressure, the most stable phase is the monoclinic phase, while at elevated pressure, bulk $HfO_2$ demonstrates two orthorhombic polymorphs. Under pressures ranging from 4 to 14.5 GPa, symmetry reduction converts one type of orthorhombic phase from the tetragonal phase. A pressure over 14.5 GPa is necessary for the interconversion between two orthorhombic phases, and the transition pressure is essentially temperature-independent. These polymorphs all feature a symmetry center. These structures' centrosymmetric characteristics cannot produce ferroelectricity [36].

The monoclinic phase is more energetically preferred than the ferroelectric Pca21 phase, which may be formed in films with thicknesses less than 40 nm, according to the bulk free energy theory. *Park et al.* examined the ferroelectric orthorhombic phase fraction and ferroelectric characteristics in films of $Hf_{0.5}Zr_{0.5}O_2$ ranging in thickness. A steady decrease in the $P^r$ and orthorhombic phase percentage was observed as layer thickness increased. Comparable outcomes were documented in $HfO_2$ films ranging in thickness from 4 to 20 nm. The $HfO_2$ films showed decreased Pr and permittivity as the thickness grew from 6 to 20 nm. Each grain grows towards the top electrode (TE) from the bottom electrode (BE), given that the horizontal and vertical dimensions are comparable to the film thickness [56–61].

## 2.1 Impact of Dopants

The dopants, such as silicon, zirconium [29], aluminum [62], yttrium [27], and lanthanum [63,64], used in $HfO_2$ films can modify the crystal structure and ferroelectric properties. Silicon-doped $HfO_2$ films were the first to demonstrate ferroelectricity [20]. They showed great promise for industrial use since silicon is the most widely used element with well-established process/technical characteristics. There has been a significant amount of systematic research on the choice of dopant, and it was found that the microstructure depends on the dopant's concentration and size. The paraelectric-ferroelectric-antiferroelectric transitions happen with increasing dopant concentration in films containing smaller-sized dopants, including silicon and aluminum [20,62,65]. While doped with silicon, the anti-ferroelectric properties appear when the concentration of dopants goes over 4.3%. At 4.8% molar concentration, aluminum doped $HfO_2$ demonstrates ferroelectric behavior, while at 8.5% Al, an explicit anti-ferroelectric behavior is seen. Since zirconium can replace hafnium over the complete composition range, it is another potential dopant to preserve the ferroelectric characteristics across a wide range of zirconium concentrations. It can be observed that ferroelectric behavior in hafnium oxide is established when the zirconium content reaches around 30%. Further increase beyond 70% makes the thin film anti-ferroelectric, while the highest $P^r$ was achieved at 50% concentration.

Large-sized dopants, such as Yttrium, Galadium, and Lanthanum, show distinct transitions with increasing concentrations, in contrast to small-sized dopants. Hafnium oxide is first paraelectric, changes to ferroelectric, and then returns to paraelectric with increasing doping concentrations [27, 63, 64, 66, 67].

FE-$HfO_2$ films, doped with dopants of different sizes, were compared by *Schroeder et al.* The range of the size of the dopant varied from 54pm, which is silicon to 132 pm, which is strontium [68]. The occurrence

of AFE behavior or the tetragonal phase in $HfO_2$ films containing smaller-sized dopants, like silicon (Si) and aluminum (Al), was ascribed to the unique phase transition pathway. As the doping concentration increases, monoclinilic-orthorhombic-tetragonal-cubic phase transitions occur. Conversely, a monoclinic-orthorhombic-cubic phase change occurs in $HfO_2$ films containing large dopants. Larger dopants like Yttrium, Galadium, Lanthanum, and strontium do not promote the creation of the tetragonal phase, which results in anti-ferroelectric behavior.

## 2.2 Superlattice Structure

Apart from the solid-solution-based hafnium oxide thin films, a recent trend in superlattice structures has been researched recently. Lehninger et al. conducted a systematic study on superlattice structure. That study investigated ferroelectric embeddings in the metal-ferroelectric-metal structures with five different superlattice stacks with varying sublayer thicknesses and a constant overall thickness of 10 nm. The details of the stacks are as follows:

1. 0.25 nm $HfO_2$/0.25 nm $ZrO_2$
2. 0.5 nm $HfO_2$/0.5 nm $ZrO_2$
3. 1 nm $HfO_2$/1 nm $ZrO_2$
4. 5 nm $HfO_2$/5 nm $ZrO_2$

Devices with solid solution films show nearly no pinching of the hysteresis loop in its pristine form, according to research conducted on the subject. In contrast, antiferroelectric-like solid properties are seen before wake-up cycling when the MFM capacitors include the superlattice films. According to the scientists' conclusions, the laminates either stabilize a more significant number of in-plane oriented domains that can behave antiferroelectrically within the o-phase or crystallize preferentially in the antiferroelectric-like tetragonal phase. On the other hand, these integrated superlattice devices can be fully woken up with fewer than 1000 field cycles [69–72]. Of course, several process conditions impact the crystallization process. The doping ingredient and its concentration have a significant impact on this. Since the discovery of ferroelectricity in Si-doped $HfO_2$, many dopants have been proposed. The choice of electrodes and substrates also played an essential role in dictating the ferroelectric properties in $HfO_2$ films.

## 2.3 Deposition Technique

The meta-stable O-phase with non-centrosymmetric structure of $HfO_2$ thin films is stabilized by doping: this is one of the possible explanations for ferroelectricity in $HfO_2$. We should remember that we are talking about thin films, not bulk. During film manufacturing, the FE phase Pca21 may be stabilized using various growth settings, such as ALD, PVD, CSD, and PLD.

Commercially accessible ingredients are utilized in the atomic layer deposition procedure to make ferroelectric $HfO_2$ films [20]. The most common precursors are tetrakis(ethylmethylamino)zirconium, tetrakis(dimethylamino) silane and SiCl4, and tetrakis(ethylmethylamino)hafnium and $HfCl_4$. Argon is a purge and carrier gas; oxygen sources include water and ozone. On titanium nitride (TiN) or tantalum nitride (TaN) BE, the first $HfO_2$ films formed are amorphous. A TE layer is capped and rapidly heated to annealed crystals to introduce ferroelectricity.

With physical vapor deposition techniques, it is possible to accurately manage the sputtering, sputter power, atmosphere, and deposition temperature to produce $HfO_2$ films with various phases and varying phase fractions, as well as the associated macroscopic ferroelectric performance. This is advantageous for investigating the structure-property connection of ferroelectric $HfO_2$ films, and it's also intriguing since it shows how the growth parameters regulate the phases in the $HfO_2$ films that are produced, particularly the ferroelectric Pca21 phase [73, 74].

## 2.4 Annealing and Capping Layer

$HfO_2$ films from atomic layer deposition that have been deposited generally have an amorphous form. It is best to anneal to crystallize. Because of the strain effect, a capping layer significantly promotes the induction of ferroelectricity during the annealing process. The strain caused by the variations in thermal expansion coefficients between the $HfO_2$ films and the capping layer is significant. BE substantially impacts the ferroelectricity of $HfO_2$ films. BE can control the growth and grain orientations of FE films and generate in-plane strain. *Park et al.* confirmed that $HfO_2$ films on (111)-oriented Pt bottom electrodes are (111)-textured, while grains in $HfO_2$/TiN have arbitrary orientations. Both types of films exhibit a high in-plane tensile strain of above 1.5%. 110-oriented t-phase can transition to the Pca21 phase because the c axis of the t-hase can be elongated by

applying in-plane tensile strain to form the axis of the o-phase. However, switching from the t-phase to the o-phase for (111)-textured films on (111)-oriented Pt BE requires more strain. [65, 75, 76].

## 2.5 Wake-up

The wake-up effect refers to forming a ferroelectric-like hysteresis curve from anti-ferroelectric-like pinched hysteresis features in $HfO_2$-based FE films. This is a fascinating scientific phenomenon that also has practical applications in a variety of gadgets. Surprisingly, these materials demonstrated a "wake-up effect", a rise in $P^r$ with higher $\xi$ cycles before the fatigue effect. The researchers employed the conventional, slowly varying $\xi_{ext}$ field stimulus and pulsed stimulus to examine the wake-up effect through the P-$\xi_{ext}$ hysteresis curve. While the latter can offer detailed quantitative data on the evolution of the HZO/TiN contact characteristics, coercive field ($E_c$), and potentially involved interfacial capacitance, the former helps investigate the evolution of FE-AFE features as the cycle number increases. Understanding the influence of interfacial capacitance is often more challenging for polycrystalline films like $HfO_2$ [60, 77–81]. Several research studies have investigated the underlying reason for the wake-up effect. However, the explanations have yet to merge into a single focal point, and the wake-up is a complicated event that may entail several underlying episodes. Several investigations have found electric field-induced phase transformations during wake-up. Transmission electron microscopy observations after various field cycles indicated that in virgin films, a nonpolar tetragonal phase exists in the bulk of the film and at the metal-ferroelectric interface. Field cycling leads this phase to transition into polar orthorhombic phases. However, because various capacitors were used for the experiments, it is questionable if there is any statistical significance given the limited sample regions found during local transmission electron microscopy (TEM) observations. Although the $P^r$ increases of 20–100% are recorded, synchrotron-based in situ XRD measurements conducted during field cycling are claimed to exhibit observed phase shifts generally in the sub 5% range. As a result, phase alterations occur during field cycling, but they are not the primary mechanism responsible for the wake-up effect. It should also be noted that all of these studies were conducted in ferroelectric films with a thickness of more than 10 nm. Ferroelectricity is known to be the aftermath of a "polarization catastrophe", where the crystals get locked in a position during the application of an external electric field, engendering the non-zero polarization with no electric field. During this lock-in period, the crystal will tend to move to the minimum energy state, and there is a probability that anharmonic restoring forces, as mentioned by Charles Kittel, lead to the change of the crystal properties. However, However, this may not be the case for ultra-thin ferroelectric films. In addition to the nonpolar-to-polar phase transition, several other mechanisms have been proposed to account for the changes seen during the wake-up phase when field cycling is applied. These include domain depinning, a shift in polarization orientation, and cycling-induced modifications to the depolarization field, which may be the primary mechanism responsible for the wake-up effect in ferroelectric films with various thicknesses. Figure 4 shows the dependence of polarization response concerning $\xi_{ext}$ on the operating temperature. The pinched hysteresis opens up with increasing temperature. This incident proves that although there might be an electric field-induced phase change in the interface or bulk hafnium oxide, that is not the only reason behind the wake-up [68, 82–85].

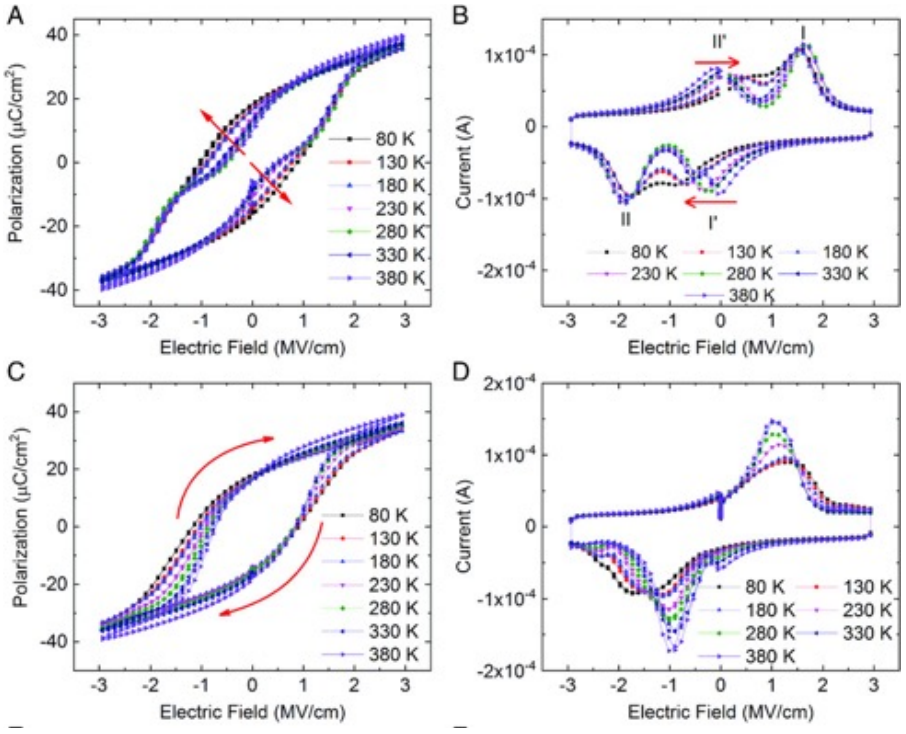


Figure 4: Measurements of dynamic hysteresis of pristine and woken-up films at ambient temperatures within the 80–380 K range. A) A virgin sample's hysteresis curves. B) the switching current is to the applied electrical field for a pristine film. C) A woken-up sample's hysteresis curve. D) Altering current in response to an electrical field for a film that awakens. Figures reproduced with permission from [82].

A recent study in [86] offers a thorough explanation and convincing experimental data, emphasizing the interfacial layer's (IL) critical function and its gentle disintegration in the wake-up phenomena. An FE wake-up model, considering multi-domain factors called inter-layer soft-breakdown (IL-SBD), is created to validate the suggested process, including trap-assisted tunneling within the interface, charge screening at the BE/HZO interface, and defect production. The model faithfully replicates the pattern of wake-up behavior's thickness dependency and highlights extra variability brought about by the wake-up process. It highlights the importance of keeping the IL as low as possible in ultrathin HZO devices. The voltage-dividing and depolarization effects are the two main ways the IL negatively impacts the ferroelectricity in the HZO device. The applied voltage should decrease across the FE layer in a perfect world without the IL. However, the IL splits The applied voltage, which lowers the voltage across the FE layer. As a result, the gadget reduces the $P^r$ value by operating inside a minor loop instead of the anticipated saturation loop. The depolarization impact is the second factor. Without the IL, the image charges at the electrodes thoroughly screen the HZO dipoles, allowing a similar $P^r$ read-out equal to the HZO's $P^r$. Nevertheless, the IL creates a depolarization field that reduces the image charges at the electrodes and jeopardizes the $P^r$ read-out.

## 2.6 Thickness Scaling

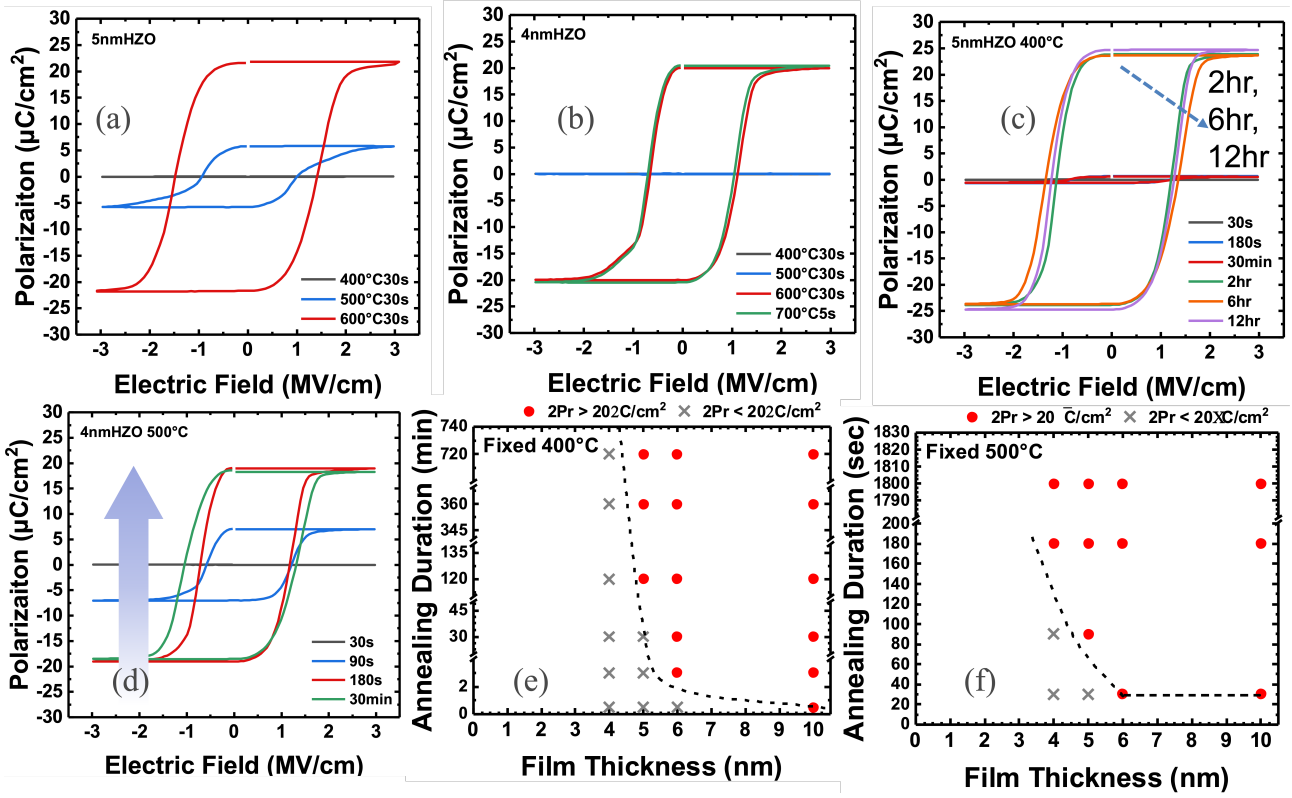


Figure 5: EThe P-E properties of (a) 5 nm and (b) 4 nm HZO following various temperatures of annealing. The P-E properties of (c) 5 nm and (d) 4 nm HZO following annealing for varying amounts of time at 400°C and 500°C, respectively. The PMA of (e) 400°C and (f) 500°C annealing time-film thickness mapping. There is a definite trade-off between thickness scaling and the thermal budget. Figures reproduced with permission from [87].

$HfO_2$ is amorphous when deposited, and annealing is required to initiate the ferroelectricity, which is only visible in its polar-orthorhombic phase in $HfO_2$-based ferroelectric films. Several variables determine the development of the crystalline phase in $HfO_2$ throughout the annealing process. While many research groups have high hopes for the BEOL integration of ferroelectric memories, a significant obstacle is the rising annealing thermal budget that comes with the ferroelectric film's growing thickness. Consequently, with a ferroelectric sheet thickness of about 10 nm, most BEOL ferroelectric memory demonstrations are above 130 nm nodes. A thick ferroelectric layer raises the required operating voltage, endangering the system's scalability.

Unlike PZT-based ferroelectric materials, $HfO_2$ based materials show ferroelectricity in ultra-thin films [88]. However, the requirement for high annealing temperature poses a bottleneck for BEOL integration. One of the earlier investigations showed that long-duration annealing (up to 180s) may support the ferroelectric phase in zirconium (20%) doped $HfO_2$ [75]. RTA was typically utilized to crystallize the HZO. Another study suggested that an increase in the m-phase fraction during long-term annealing at 500°C and 600°C or a prolonged rising time for RTA would result in a degradation of the ferroelectric characteristics of HZO. On the other hand, HZO films exhibit superior ferroelectricity by furnace annealing at ≤400°C for an extended annealing duration. Previous research has also demonstrated that the high annealing temperature lowers the residual polarization ($P_r$) value by causing HZO to generate a more significant fraction of the monoclinic (m)-phase due to the fast rise in grain size. These results suggest that the creation of the m-phase and degradation of the Pr value are not considerably caused by extending the annealing period at a comparatively lower temperature (dopant concentration-dependent). Most of the above research concentrates on hafnium zirconium oxide (HZO) films of ten nanometers or more.

The polarization against external electric field characteristics of ferroelectric capacitors with 5 nm and 4 nm thickness are displayed in Figure 5. Both types of HZO films show differential remnant polarization ($2P^r$) over 40 $\mu C/cm^2$ with PMA of 600°C, as can be seen in Figures 5(a) and 5(b). In this instance, the PMA's length was set at thirty seconds. Higher residual polarization raises the annealing temperature to a certain point since it raises the fraction of orthorhombic-phase crystallization. Further research is necessary because this PMA temperature is incompatible with the BEOL semiconductor process. Figures 5(c) and 5(d) make the

significance of PMA duration very evident. When exposed to PMA of 400°C for 30 minutes, 5 nm thick HZO films successfully obtain $2P_r \geq 40\ \mu C/cm^2$; at PMA of two hours and above, they do not exhibit ferroelectric characteristics. On the other hand, even after twelve hours at 400°C with PMA, 4 nm thick HZO films exhibit no ferroelectric characteristics. However, when the PMA length is greater than 90 seconds at 500°C, non-zero $P^r$, a sign of ferroelectricity, begins to occur in 4nm HZO. It saturates at about 40 $\mu C/cm^2$ for PMA duration longer than 180 seconds (Figure 5(d)). The thickness-dependent annealing time needed for HZO films at 400°C and 500°C, respectively, are summarized in Figures 5(a) and 5(b). Ferroelectricity in the device is indicated by the obtained 2Pr value greater than $\mu C/cm^2$. The outcome implies that the thinner HZO must be annealed for extended periods or at higher temperatures to obtain crystallization with adequate ferroelectricity.

# 3 Capacitive Ferroelectric Memory

FCMs rely on capacitance modulation for data storage and offer several advantages over conventional resistive memory technologies. These include minimal static power consumption, negligible read disturbance, and immunity to Intermediate Resistance Drop (IR) drop issues [89]. Memory architectures such as FRAM or single-selector-less FCM-based cross-bar arrays capitalize on this principle [**?**, **?**, 89–92]. In these memory devices, reading involves the application of a voltage pulse. Depending on the polarity of the polarization state, the capacitor allows a current flow between its terminals. Several vital characteristics define an optimal FRAM device.

1. High $P^r$.
2. Low operating voltage.
3. Polarization switching current should be higher than displacement current.
4. High endurance, typically exceeding $10^{15}$ cycles.
5. Retention of data for over ten years.

The quintessential bit-cell structure for using FRAM in a crossbar array is similar to the 1T-1$C_{FE}$ bit-cell structure of DRAM, as seen in figure.6. The transistor is an access transistor for the memory element in the bit-cell, the ferroelectric capacitor. In the 1T-1$C_{FE}$ configuration, one terminal of the FeCAP is connected to the plateline (PL). In contrast, the second terminal is attached to one source or drain terminal of the access transistor. Figure.6(a) shows the bit cell arrangement. This setup allows access to the memory cell for reading or writing data. During the write operation, write voltages of either polarity are applied to the ferroelectric capacitor's (FeCAP) terminals. To write a "1" into a memory cell, the BL is raised to $V_{DD}$, followed by increasing the WL to $V_{DD} + V_T$, where V$T$ represents the access transistor's threshold voltage. A suitable voltage pulse is then applied to the PL, first pulling it up to $V_{DD}$ and then down to 0V, as illustrated in figure.6(c). The *WL* remains active until the *PL* is pulled down and the *BL* is reset to zero. Finally, deactivating the WL maintains this condition until the subsequent access cycle. To write a "0" in the cell, the *BL* is driven to 0V before activating the WL. The subsequent process is the same as writing a "1" as shown in figure.6. The transistor is turned on again during the reading process, and a voltage pulse is supplied to the PL.

During the read operation, BL is precharged to 0V before the word line WL is activated. This sets up a capacitor divider between the PL and the ground, involving the capacitances of the ferroelectric capacitor ($C_{FE}$) and the bit line ($C_{BL}$). Subsequently, the PL is raised to $V_{DD}$, leading to a polarization reversal that transfers the polarization switching charge to the *BL*, depending on the stored polarization within the FeCAP. Therefore, relative capacitances of $C_{FE}$(which depend on the stored data) and $C_{BL}$ determine the voltage on the *BL* voltage. Specifically, the voltage signal developed is given by $\delta V_{BL} = 2P_r/(C_{FeCAP} + C_{BL})$. The actual read signal detected by a voltage sense amplifier depends on the array design. Typically, the SA is realized using a cross-coupled inverter. The reference input voltage of SA, denoted by $V_{ref}$ in figure6(a), is generated through the external input pad or reference bit-cells. The destructive nature of the read operation in FRAM typically necessitates a subsequent write-back procedure. Consequently, the energy required to read the FeCAP can be as much as twice that of a single write operation at the cell level, contingent upon the specific data being read. To increase the scalability of FeCAP-based memory cells using planar capacitors, it may be necessary to adopt a 2T-1C design, which includes an extra read transistor within each memory cell [93]. Unlike the 1T-1$C_{FE}$ arrangement, 2T-1C directly transfers the ferroelectric capacitor's polarization charge to the read transistor's gate. As a result, obtaining optimal alignment between the size of the read transistor and the ferroelectric capacitor is critical, as both the access and read transistors primarily determine the cell's dimensions. [94, 95].

Commercializing ferroelectric capacitor-based memory as a standalone product poses several challenges that need to be overcome, such as reducing the thickness of the ferroelectric layer to below 10 nm, ensuring effective Backend of the Line (BEOL) integration, enhancing read/write endurance, and improving sense margin, etc. The

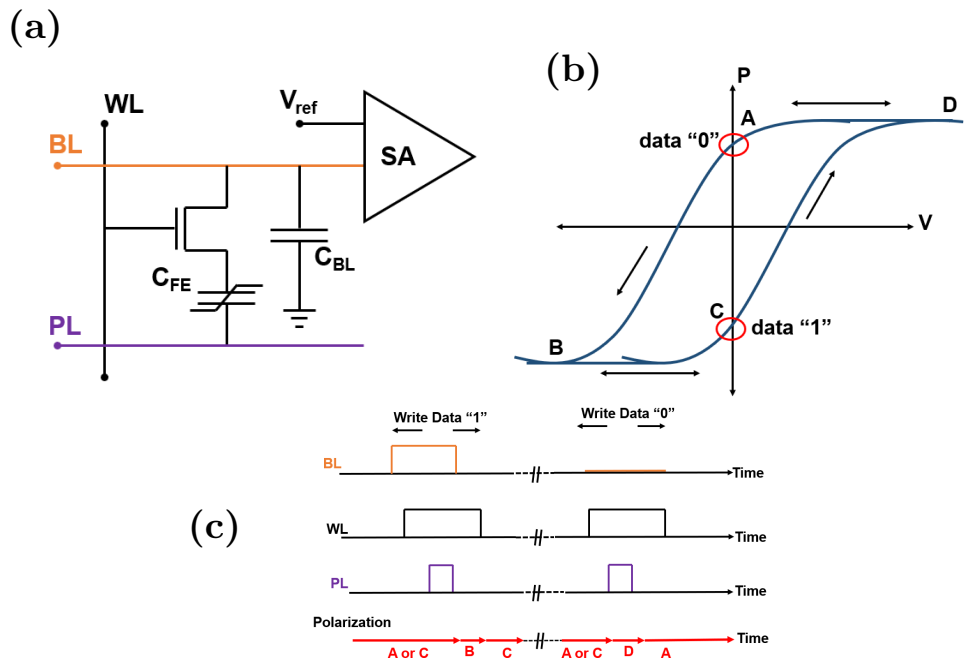


Figure 6: The ferroelectric 1T-1C$_{FE}$ memory cell. C$_{BL}$ represents the total parasitic capacitance of the bit line, and C$_{FE}$ denotes the ferroelectric capacitor. (b) The hysteresis loop characteristic of a ferroelectric capacitor shows the stable polarization states A & C. (c) Timing diagram associated with write operation in the 1T-1C$_{FE}$ memory cell.

following discussion will highlight recent advancements to tackle these issues. *J. Okuno et al.* have showcased a 64 kbit 1T-1C$_{FE}$ FRAM array featuring a dedicated circuit for array operations control. Their study utilized FRAM devices configured with TiN/$Hf_{0.5}Zr_{0.5}O_2$ (HZO)/TiN, integrated into theBEoL process [96]. Notably, the BEoL integration was meticulously optimized for sub-500$°C$ processes, demonstrating no degradation of the underlying CMOS logic. This research underscores high yield and excellent operational performance, with operation at a low voltage of 2.5 V, operating speed of 14 ns, and $2P^r$ exceeding 40 $\mu$C/cm$^2$ during array operation. Moreover, it boasts endurance surpassing $10^{11}$ cycles and data retention extending beyond 10 years at 85$°C$. Crucially, precise control over memory cells for programming and reading ensures 100% bit functionality. The findings reported in this work cater to the stringent specifications of LLC and embedded NVM for low-power System-on-a-Chip SoC applications, especially in IoT. In the subsequent phase of the study, the operational efficiency of this array is significantly enhanced through the thickness scaling of the ferroelectric HZO layer, resulting in the attainment of flawless 100% bit functionality at an impressively reduced operational voltage of 2.0V and an enhanced operating speed of 16 ns. Remarkably, the array exhibited exceptional cycling endurance, surpassing $10^8$ cycles, even under accelerated stress conditions of 3.5V at 85$°C$.

*T. Francois et al.* reported 130nm technology node-based BEoL integration of a 16kbit 1T-1C$_{FE}$ FRAM array with silicon doped $HfO_2$ [97]. Across a spectrum of capacitor areas, ranging from 0.36$\mu m^2$ to as low as 0.16$\mu m^2$, the authors achieved remarkable switching speeds as low as 4ns. Furthermore, the endurance performance of these devices is noteworthy, with capabilities extending up to $10^7$ cycles on a full 16kbit array. A wide memory window is observed for programming voltage as low as 2.5V, coupled with the absence of zero-bit failure at the array level. This milestone represents the first demonstration of BEoL-integrated $HfO_2$-based FRAM arrays, which offer solder reflow capability while providing data retention capabilities up to $10^4$ seconds at an elevated temperature of 125°C. These findings establish a cornerstone for developing ultra-low-power embedded eNVM at more advanced nodes in semiconductor technology.

In another work demonstrating 130nm technology node-based BEoL integrated HZO-based 9Mb FRAM memory, the authors have used 1Mb ECC along with the 8Mb main memory segment for achieving high robustness [98]. Temperature variation plays a vital role in the fidelity of operation of eNVM chips [99]. Therefore, the authors exploited the ECC functionality to design a write driver, which is adaptively immune to temperature variation. Also, a high write voltage refresh scheme was added through the ECC block to mitigate the $P_r$ degradation. Furthermore, these variation-aware capabilities enable dynamic voltage tuning, enhancing overall power efficiency. The SA made another level of improvement with the offset-cancelation facility. This is how the work mentioned in literature [98] avoids the negative impact of PVT variations in Mb-level FRAM chips with enhanced BER.

The traditional approach to reading FeCAPs is inherently destructive, relying on polarization switching and thus necessitating re-writing the stored memory state after each read operation. Consequently, the read endurance mirrors the write endurance. Regrettably, this coupling of read and write endurance renders the read endurance of FeCAPs inadequate for many FRAM or CiM applications [100]. However, a recently introduced innovative concept of an eNVM that exploits the CMW in terms of differences in permittivity or, in other words, capacitance ratios in FeCAPs in different programming states offers a promising solution. This concept facilitates read operation without destroying the stored state [91]. Through careful engineering of interfacial asymmetry between the electrodes of a fully BEOL-compatible HZO-based FeCAP, the authors achieve a notable CMW ($\epsilon_r$ difference at 0V: $\text{CMW}_{\epsilon_r}$). Interstingly, employing a conventional charge-based read operation, the authors demonstrate that the $\text{CMW}_{\epsilon_r}$ obtained from a C-V measurement correlates directly with a charge-based MW ($\text{MW}_Q$), showcasing pulse-based non-destructive readout (NDRO) of the $\text{CMW}_Q$. This NDRO strategy effectively decouples the read endurance (exceeding $10^{11}$ cycles) from the write endurance (approximately $10^7$ cycles).

Efforts are also underway to develop anti-ferroelectric (AFE) HZO-based FRAM, as highlighted in [101]. These AFE-based FRAM devices can be operated at 2ns speed, ranging from -1.6V to 1.2V, and inevitably show higher endurance ($\geq 10^{12}$)than any other operating modes. They also maintain a robust MW, even when subjected to a 20% variation in $V_{write}$ at elevated temperatures. Moreover, these devices exhibit minimal tail-bit variations of scaled capacitors across a 300mm wafer, even at elevated temperatures, operating at $4\sigma$. These findings strongly advocate developing AFE-based FRAM-based emerging memory for high-speed and high-density embedded memory applications in the future.

Apart from the above-mentioned advances, there are many challenges that we must overcome, such as the wake-up, fatigue, and imprint effects when aiming to realize larger FRAM arrays, as discussed in several literatures [102–104].

# 4 High-K Metal Gate Ferroelectric Field Effect Transistors

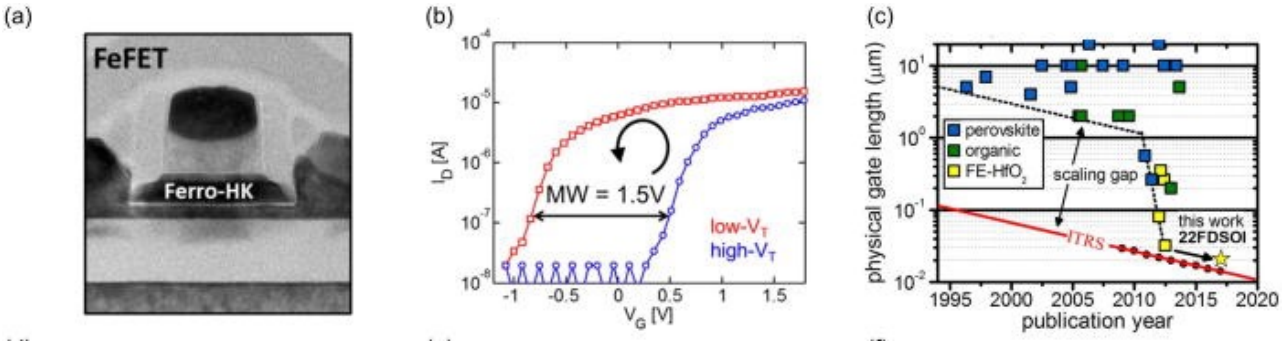


Figure 7: (a) An embedded FeFET memory cross-sectional TEM picture from the 22 nm FDSOI platform. (b) Transfer device characteristics with a 1.5 V memory window, LVT and HVT. (c) FeFET's physical gate length scaling about eNVM logic platforms. Figures reproduced with permission from [105]

Bell Labs first introduced employing a ferroelectric substance to modify a semiconductor layer's surface conductivity in 1957 [106–109]. One goal was to develop a device that could switch and store data in a nonvolatile way that could be read out without causing damage. In the 1960s, thin-film transistors based on cadmium sulfide (CdS) were placed onto a thin ferroelectric triglycine sulfate (TGS) layer. This led to the first experimental reports of such devices, now known as ferroelectric field-effect transistors (FeFETs). Moll and Tarui showed that the space charge in the CdS semiconductor may be controlled by the $P^r$ of the TGS crystal, leading to a 25% change in device resistance [110].

Integrating FE-$HfO_2$ into the gate stack, FeFETs have been introduced as embedded memory at 28nm-HKMG and 22nm FDSOI technology nodes. Dual integration (non-FE and FE) in standard CMOS technology was demonstrated with an 8nm FE-$HfO_2$ layer. Si-doped $HfO_2$ is typically used in gate-first integration due to the high thermal annealing needs [111, 112]. Increasing the ferroelectric layer's thickness requires a bigger memory window with good retention. However, greater switching voltages are needed; as a result, they are incompatible with advanced technology nodes. Therefore, a thinner ferroelectric layer is desired for advanced node integration.

Quintessentially, the gate stack of FeFET consists of a gate electrode (metal)- a ferroelectric layer-interfacial layer, and a semiconductor. A single transistor memory cell is created by integrating a ferroelectric layer, which stores data, into the transistor's gate stack. Ferroelectric materials often exhibit a distinct polarization–electric

field hysteresis. They have two polarization states, known as $P^r$, opposing yet comparable. Even in the absence of the applied electric field, they stay steady. The presence of persistent electric dipoles within the unit cell, resulting from the non-centrosymmetric crystalline structure of FE materials, is linked to the microscopic origin of the two PR values. There are two stable configurations for the dipoles, often known as polarization 'up' and 'down.'

The ferroelectric layer applies the field effect (electric) onto the channel or the active region of the FeFET through the charge associated with $P^r$, which is the fundamental working principle of a FeFET. Because the electric dipole moment per unit volume is represented by polarization inside the ferroelectric, the surface charge that results at the interface between the ferroelectric and the interfacial layer will use Coulomb coupling to regulate the conductivity of the channel. Using an n-channel FeFET as an example, the low threshold voltage state (LVT) is produced by the polarization pointing down, which draws minority carriers toward the channel and increases its conductivity. On the other hand, these carriers tend to be repelled by polarization that is oriented upward, which lowers channel conductivity and causes a high threshold voltage state, or HVT.

## 4.1 Interface and Reliability

The interface plays an important role in the reliability of ferroelectric FET, especially in silicon-based FeFETs. It has already been shown that the READ-Voltage and interface quality are critical to the FeFET's performance, particularly regarding low-frequency noise response, durability, and retention [113–117].

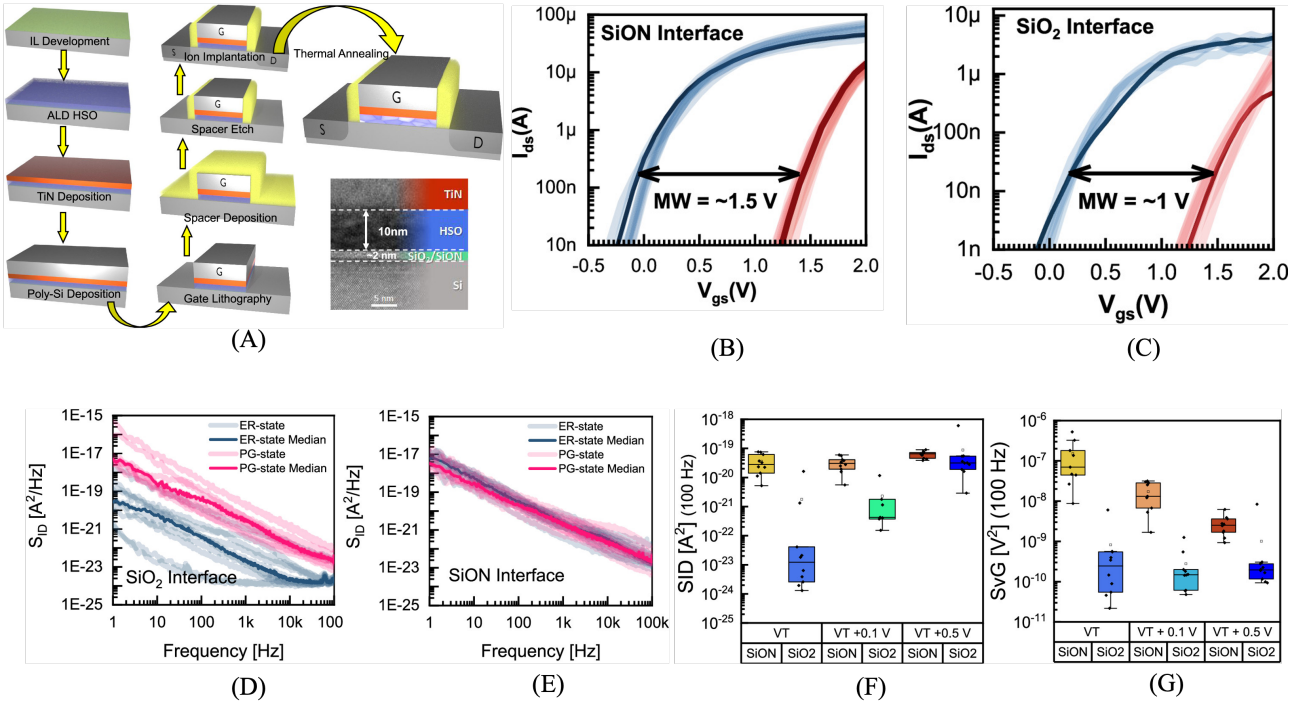


Figure 8: (a). Schematic representation of the process flow with transmission electron microscopic image of the HKMG FeFET cell. (b,c) Transfer characteristics and (d,e) power spectral density and no of FeFETs with $SiO_2$ and SiON interface. Endurance and retention characteristics of FeFET with SiON and $SiO_2$ interfaces. Figures reproduced with permission from [118].

Compared to $SiO_2$, FeFETs with SiON interfaces have a larger memory window. The trapping and de-trapping processes from the contact are responsible for this characteristic. An improved understanding of the underlying reason for memory window shrinking in $SiO_2$-based FeFETs may be obtained by further analyzing the low-frequency noise. On the other hand, for both interfaces, the variance across devices and the ratio of on-state current ($I_{on}$) to off-state current ($I_{off}$) are nearly unchanged. A 100 mV offset from the threshold voltage (VT) operation point was used to assess the spectral density of the drain current ($S_{ID}$). The $S_{ID}$ noise behavior for the 10 nm HSO $SiO_2$ interface structure is shown up to 100 kHz in an erased and programmed condition. The noise behavior for ER and PG does not differ from that of the other states. The PG-state has similar noise behavior in the lower frequency range compared to dielectric devices in 22 nm technology. There is a two-magnitude difference for the higher frequencies. The noise level for the $SiO_2$ interface structure exceeds the system limit at higher frequencies.

The SiON structure has a greater noise level than the $SiO_2$ structure when compared directly to the threshold voltage operating point. The noise level in the SiON structure decreases as the gate voltage Vg increases, whereas

the noise level in FeFETs with $SiO_2$ interface stays constant over a range of gate voltage values. As in the normalized SID, the SiON structure exhibits a continuous declining trend with rising gate voltage, while the $SiO_2$ interface structure has the same SvG at various operating points. For lower gate voltage operation points, SiON and $SiO_2$ differ from one another similarly in SvG and SID. For the SiON interface, the gate input for a higher working voltage is less than the overall noise level of this arrangement. An increase in operating voltage does not affect $SiO_2$ either.

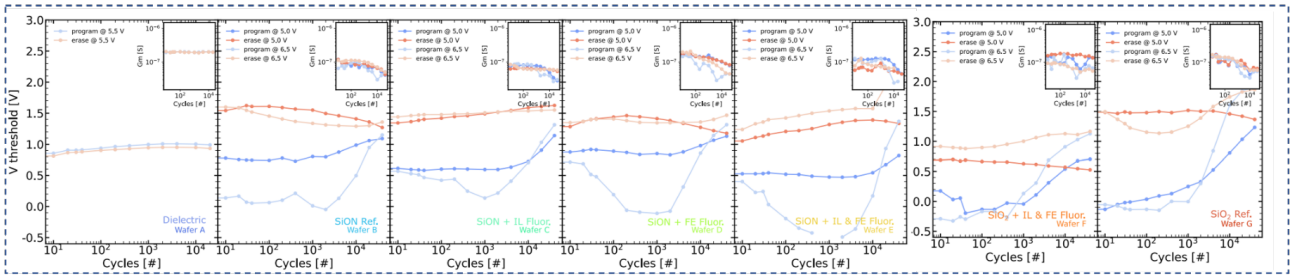


Figure 9: SiON and $SiO_2$ FeFET program and erase threshold voltage and gm over cycling. The dielectric wafer shows no discernible deterioration under cycling except for a tiny trapping window. For low write voltages, early memory window closing is seen in SiON-based wafers that are not fluorinated. Higher voltages cause a strong walk-out (electron trapping) to higher threshold voltages and enhanced hole trapping, as seen by the erase state's threshold voltage. Voltages for large cycle counts. For interface fluorination, an increase in stability is seen. Strong program state bulging at lower threshold voltages due to ferroelectric layer fluorination increases the memory window significantly. Figures reproduced with permission from [119].

Another recent work [119] demonstrates the impact of fluorination on the interface quality of FeFETs. FeFETs were created with a 10 nm Si: $HfO_2$ (HSO) layer with either $SiO_2$ or SiON interfaces. Fluorination was administered to both interfaces. Fluorination makes steady transconductance and enhanced high-voltage stability possible and typically exhibits a substantial memory window. However, a soft breakdown causes the memory window to shut again at higher cycling rates (up to $3 \times 10^4$ cycles). When comparing the extracted threshold voltage for program/erase, significant variations may be seen for the SiON FeFETs depending on the various fluorination processes.

A memory window closure is shown for the reference and the ferroelectric wafer that has been fluorinated at a 5 V cycling amplitude. Around $10^3$ cycles in the erase stage, more hole trapping is seen at larger cycling amplitudes—the presence of interface fluorination results in a substantial and steady memory window. A decrease in the program state to lower threshold voltage is present for ferroelectric layer fluorination and interface+ferroelectric layer fluorination, leading to a massive memory window of more than 2 V for the latter. It was concluded that even with SiON FeFETs with endurance optimization, fluorinating FeFETs can increase device endurance by a factor of ten. Additionally, interface fluorination makes steady transconductance and enhanced high-voltage stability possible.

## 4.2 Temperature and Reliability

Since an increase in junction temperature is a fundamental phenomenon in computer systems, a memory system's ability to withstand temperature increases is crucial. Numerous research described the effects of temperature fluctuation on memory window (MW), endurance, retention, and LTP–LTD properties. MW diminishes as the operating temperature rises, reaching its maximum value at 25 °C and its lowest at 120°C. The variation in the surface carrier concentration, $P^r$, and coercive field ($E_c$) may all be used to explain the MW's dependency on operating temperature. MW decreases due to a drop in carrier mobility ($\mu_(n,p)$), $P^r$, and $E_c$, despite the surface carrier density increasing with growing temperature. The number of programmable states in LTP–LTD also drops with increasing temperature.

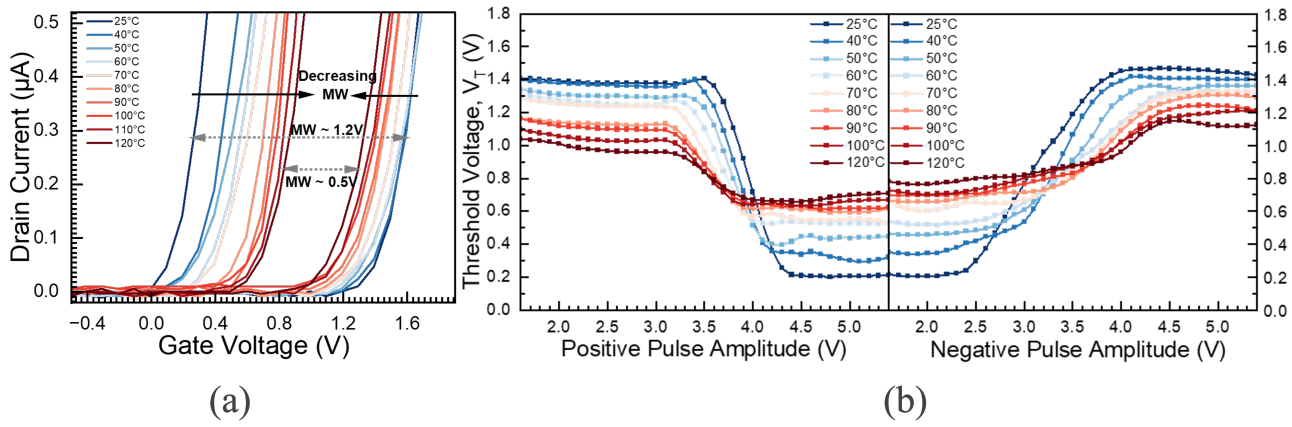


Figure 10: a) Measured drain current versus gate voltage characteristics demonstrate the shift in threshold voltage that causes a modification in the memory window in response to an increase in temperature. Transfer characteristics show that the response of surface charge, $P_r$, and $E_c$ to temperature has a significant cumulative effect. b) The MW of FeFETs decreases with temperature, which lowers the number of programming states and threshold voltage range. Figures reproduced with permission from [120].

## 4.3 FeFET as Storage Class Memory

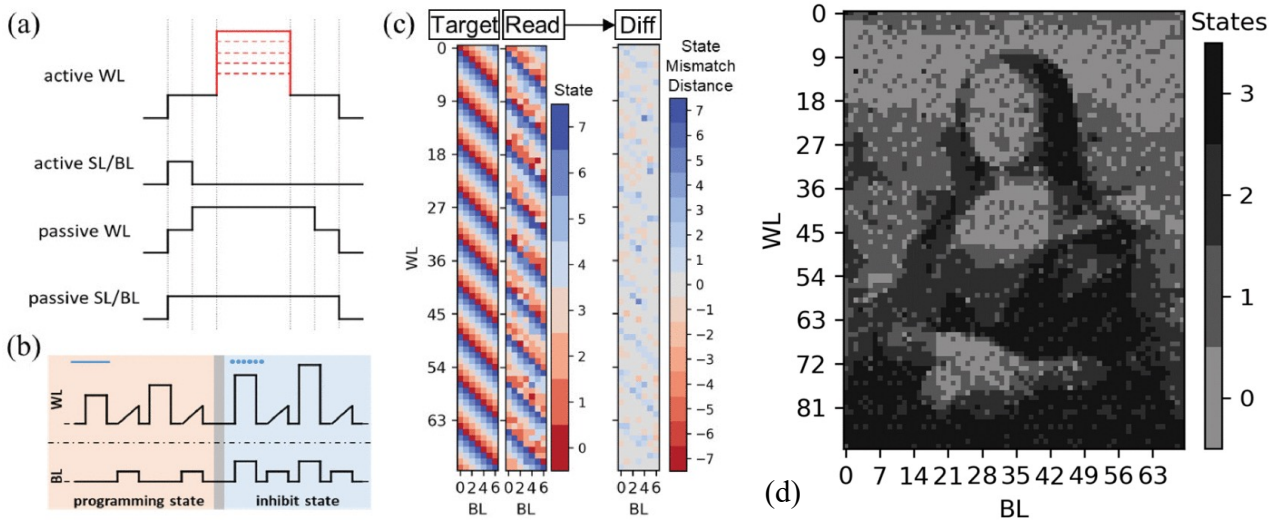


Figure 11: (a) Time the writing schedule to prevent interruptions. (b) The switch to inhibit-condition (c) from actively written FeFETs and their use in a continuous data pattern to confirm each FeFET's capacity to achieve each state. (d). One AND array is written with alternating patterns 100 times. When combined, they create the Mona Lisa's picture. Figures reproduced with permission from [121, 122].

Customers now have access to a large variety of edge devices thanks to the quick development of electronic circuits toward closely scaled technological nodes, dramatically increasing the amount of real-time data in recent years. It is necessary to adopt new architectural paradigms to handle the increasing volume of data generated in real time by end-user devices. Storage class memories (SCMs) have long been hailed as a potential technology to bridge the gap between main memory and storage, much as NAND flash and DRAM. A storage class memory has to be content addressable, non-volatile, and have low latency. SCMs should typically offer ten times quicker data programming and reading rates than NAND flash storage. Modern flash memory systems usually have a high operating voltage of 20 V, a short life of $10^4$ cycles, and a slow writing speed measured in milliseconds.

SCMs are getting increasingly well-liked because of their excellent performance and stability. SCM (ReRAM, PCM, and MRAM) has write/read speeds more than ten times quicker than NAND flash memory. For NAND flash blocks, a page functions as the write/read unit and a block as the erase unit. Because of the different write and erase unit sizes in NAND memory, in-place overwriting of pages is not permitted. Consequently, the write performance of NAND memory is not superior to its read performance.

On the other hand, SCM does not call for erasing before writing. Ferroelectric memories share a few characteristics with flash memories; therefore, they could someday take their position in the memory hierarchy. They can even be employed as SCM to fill the gap between DRAM and NAND Flash memory.

## 4.4 FeFET for Vector Matrix Multiplication

High-density FeFET-based memory arrays have been demonstrated on a 28nm HKMG node for VMM purposes. Despite various advances, a *a fly in the ointment* for the commercial-level wafer-scale operation of the FeFET-based memory array is caused by device-to-device fluctuations. Scaling and memory array size have an increasing effect on device variation [123–126].

On 300mm wafers, a new study focuses on FeFET-array operation. The influence of variation was successfully controlled by adding a transistor to one terminal of the cross-bar array. The transistor was operating in the linear-triode region for current limiting purposes. The FeFET array, access transistors, current limiting transistors, and analog-to-digital converters (ADCs) were all manufactured on the same wafer. Eight by eight segments were cut into the memory array to lessen the effect of voltage swing over word lines, bit lines, and select lines and to stop errors from accumulating over bit line current. The retention characteristics, conducted at an elevated temperature of 85∘C, demonstrate the reliability of the bit line current over $5 \times 10^4$ seconds, proving that the memory array is suitable for deployment for multiply and accumulate operation in an inference engine.

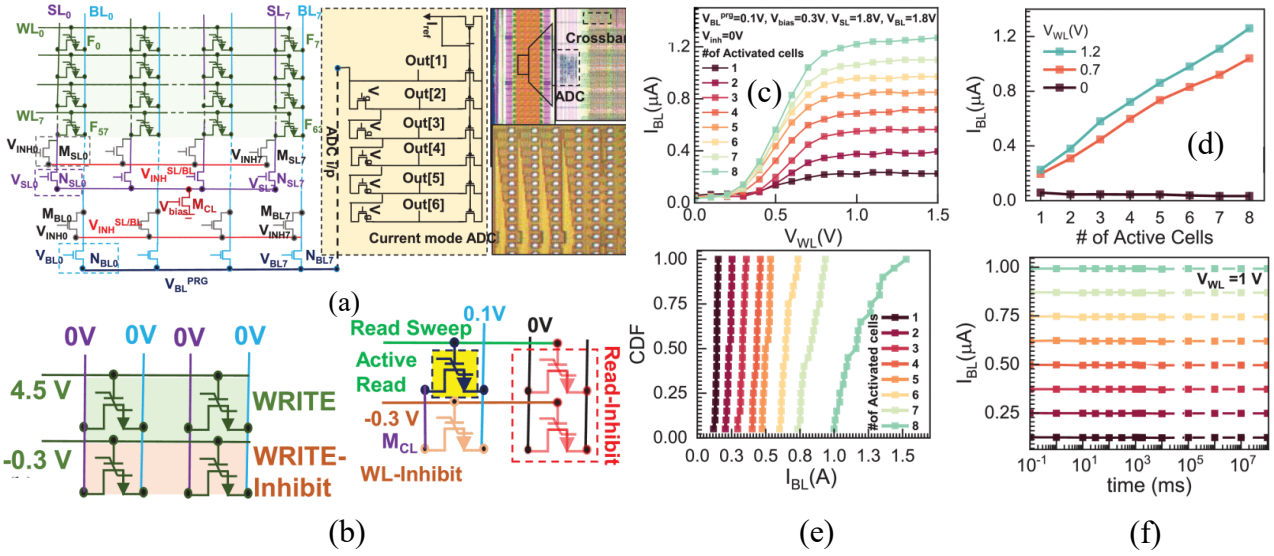


Figure 12: (a) An optical image and architecture are included in the schematic depiction of the ADC embedded memory array. (b). *Modus Operandi* of write operation. (c). The multiply and accumulate operation displays the bit line current measured for the word line voltage from an 8×8 crossbar array section. (d) Each tile's internal current limiter produces a very accurate linear multiply and accumulate operation. (e) The density plot of bit line current variation demonstrates stable array-level functioning. (f). The data retention characteristics demonstrate stable and extrapolated retention for up to 10 years. Figures reproduced with permission from [123]

## 4.5 Logic-in-Memory: Content Addressable Memory Operation

Because of its outstanding search parallelism capabilities, content addressable memory (CAM) is one of the most often employed technologies in data-centric applications. CAM designs were first implemented using SRAM cells. Instead, recent developments suggested adopting compact, nonvolatile memory. FeFETs were discovered as a multi-level NVM device with intriguing possibilities for CAM designs [120, 127].

A two-step search strategy using FeFETs was applied in a recent study [120] that suggested the 1FeFET-1Transistor-based CAM design, enabling the unique identification of the stored VT state. A search voltage above VT produced a significant ON-state current in the second step, whereas a search voltage below threshold voltage produced a small OFF-state current in the first. Thus, when a low drain current was detected in the first search phase and a high drain current in the second, the FeFET's threshold voltage state was primarily recognized. We may use the binary state of FeFETs to build a binary CAM (BCAM) or the multilevel states of FeFETs to implement a multilevel CAM (MCAM) by encoding information into the VT state of the FeFET and choosing appropriate search voltages.

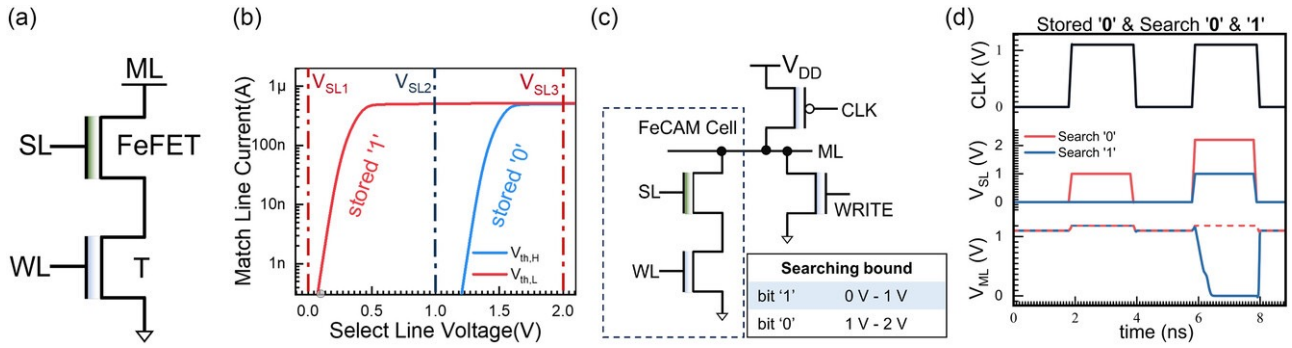


Figure 13: (a). A ferroelectric CAM (FeCAM) cell based on 1FeFET-1T. (b) FeCAM's transfer properties. To keep the ON current constant for both modes, a series current limiter restricts the FeFET drain current. (c,d) CAM cells in an array: their operation and transfer properties principle. Figures reproduced with permission from [120]

# 5 Other Types of Ferroelectric Memory

In the transmogrifying outlook of semiconductor technology for data-intensive AI applications, the demand for non-volatile memory solutions that offer high-speed performance, low power consumption, and compatibility with advanced manufacturing nodes is ever-increasing. As data processing tasks become more complex and energy efficiency becomes critical, memory technologies must adapt to meet these evolving needs. In this context, Advanced Node Compatible Ferroelectric FET Memory (Field-Effect Transistor Memory) emerges as a groundbreaking innovation to transform the memory technology landscape.

These factors can significantly deteriorate the performance metrics and reliability of the device when scaled down to nanoscale dimensions, leading to inconsistent and deteriorated behavior. For example, the devices reported in [128–130] show Multilevel cell (MLC) characteristics, but their devices suffer from limited endurance ($10^4-10^5$ cycles) and higher WRITE voltagerequirements. These parameters are not suitable for high-performance, energy-efficient compute-in-memory and high-density storage class applications, where high endurance ($> 10^{12}$ cycles) and low write voltage are desired [131, 132].

Integration of FE memory with finFET, gate-all-around, or metal-oxide-based transistor technologies is also underway for increasing the memory density [99, 133–143]. It has been hypothesized that compared to planar FeFET, the FefinFET structures have the potential to operate at lower voltage and also can have wider MW due to the impact from the fringing field. However, more investigations are required to consolidate the causes and effects. Two-dimensional semiconductor channel-based 2D-FeFETs have also been investigated in recent works by some industries. 2D material has sparked widespread interest as a platform for next-generation semiconductor materials for logic, memory, and brain-inspired computer circuits [**?**, **?**, 144–154].

Apart from the above-mentioned ferroelectric memories, there are BEOL and logic-compatible ferroelectric-metal field effect transistor (FeMFET) demonstrations with ±1.8V program/erase voltage with 100ns pulses. Eliminating charge trapping from the interfacial layer facilitates higher write endurance without retention penalty/trade-off. This structure was further improved to a 2T2C-based C$^2$FeRAM cell. With a specific area overhead, C$^2$FeRAM achieves the following highlights: In comparison to FeFET/FeMFET, C$^2$FeRAM achieves disturb-free CiM and higher write endurance (equal to FeRAM), resulting in 100x inference time with less than 1% accuracy drop for VGG8 in CIFAR-10 dataset, as well as enhanced endurance for weight updates, e.g., CiM-based transfer learning. Additionally, C$^2$FeRAM's disturb-free feature and CiM capability improve 4x energy, 200x speed, and better endurance cycles than the 1T1C FeRAM inference cache. These advantages highlight an appealing approach for future intelligent edge intelligence [155–158].

# Conclusion

Lastly, we would like to conclude via sketching a roadmap for ferroelectric memory in this section. Embedded NVM based on ferroelectric $HfO_2$ have come a long way since they were discovered in 2007. Though restricted to planar technology nodes, a deeper understanding of the underlying mechanics was obtained, especially on the material side, and conveyed to the device and system level. This resulted in the development of many memory devices centered around technologies such as FTJ, metal oxide-FeFET, FeFET, and FeMFET. Moreover, scaling these technologies to even more complex nodes is now feasible because of recent developments like Fe-finFETs, 3D-FeFETs, and FeTFTs. More research is still required to address problems with lower operating voltage, yield, durability, and lowering device variation with scaling. An ideal trade-off between robust multi-state/analog switching and scaling to more aggressive nodes must be engineered in neuromorphic applications,

such as matrix-vector multiplication or multiply and accumulate employing FeFET arrays. From this angle, sophisticated trench designs and 3D incorporation might be crucial elements. High leakage currents are another issue with scaled FeFETs. In an ideal scenario, minimal leakage currents would result from the hafnia system's huge bandgap. In actuality, however, the abundance of grain boundaries in ALD-grown polycrystalline oxides promotes trap-assisted oxygen vacancy mobility inside the $HfO_2$ layer and thus causes premature fatigue or failure. Leakage problems can be resolved, and device durability can be increased by appropriately modifying the stack crystallinity by optimization of annealing, electrodes, doping concentration, or introducing an extra dielectric layer. Hafnia-based devices performed well in cryogenic operations, demonstrating significantly better durability at low temperatures because of their restricted ion motions, which makes them appropriate for "cold-FeRAM" applications. However, the electrical working circumstances, such as voltage pulse durations, operating voltage, and refresh rates, will also have an equal impact on advanced FeFET performance. In this way, it is necessary to co-optimize circuit design, materials, and devices. We believe that a thorough grasp of the complex domain, defect dynamics, and device physics in hafnia-based systems will result in enhanced FeFET devices at scaled nodes and the commercial viability of some of the technologies above within the next ten years.

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## Symbols and Acronyms

| | |
|---|---|
| **AFE** | Anti ferroelectric |
| **BEoL** | Back end of line |
| **BER** | Bit error rate |
| **CMW** | Capacitive memory windeo |
| **CMOS** | Complementary metal-oxide semiconductor |
| **DRAM** | Dynamic random access memory |
| **eNVM** | Emerging non-volatile memory |
| **FE** | Ferroelectric |
| **FeCAP** | Ferroelectric Capacitors |
| **FCM** | Ferroelectric Capacitive Memory |
| **FDSOI** | Fully depleted silicon on insulator |
| **FeFET** | Ferroelectric field-effect transistors |
| **FRAM** | Ferroelectric random access memory |
| **high-k metal gate** | HKMG |
| **IoT** | Internet of things |
| **LLC** | Last level cache |
| **MW** | Memory Window |
| **NVM** | Non-volatile memory |
| **RTA** | Rapid thermal annealing |
| **PMA** | Post metallization annealing |
| **SA** | Sense amplifier |
| **SRAM** | Static random access memory |
| **SoC** | System on chip |
| **VMM** | vector matrix multiplication |
| $\xi$ | Electric field |
| $\epsilon$ | Dielectric constant |
| $P^r$ | Remanent Polarization |
| $P^s$ | Saturation Polarization |

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