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A Novel Isolation Approach for GaN Based Power Integrated Devices

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Abstract: This paper introduces a novel technology for the monolithic integration of GaN-based vertical and lateral devices. This approach is groundbreaking as it facilitates the drive of high-power GaN vertical switching devices through lateral GaN HEMTs with minimal losses and enhanced stability. A significant challenge in this technology is ensuring electrical isolation between the two types of devices. We propose a new isolation method designed to prevent any degradation of the lateral transistor's performance. Specifically, high voltage applied to the drain of the vertical GaN power FinFET can adversely affect the lateral GaN HEMT's performance, leading to a shift in the threshold voltage and potentially compromising device stability and driver performance. To address this issue, we introduce a highly doped n⁺ GaN layer positioned between the epitaxial layers of the two devices. This approach is validated using the TCAD-Sentaurus simulator, demonstrating that the n⁺ GaN layer effectively blocks the vertical electric field and prevents any depletion or enhancement of the 2D electron gas (2DEG) in the lateral GaN HEMT. To our knowledge, this represents the first publication of such an innovative isolation strategy between vertical and lateral GaN devices.

Keywords: Vertical GaN FinFET, GaN HEMT (Highly Electron Mobility Transistor), TCAD-Sentaurus, isolation, highly doped GaN, integrated circuits.

1. Introduction

Gallium Nitride (GaN) has recently emerged as a transformative material, poised to replace silicon (Si) in a wide range of applications due to its superior physical properties [1]. With its exceptional breakdown field, high saturation velocity, and wide bandgap, GaN-based devices exhibit outstanding performance in high-voltage and high-switching-frequency applications [2–5]. This has spurred the development of advanced GaN-based components, including GaN High Electron Mobility Transistors (HEMTs) [6–9] and vertical GaN devices [10,11].

As GaN-based power converters advance, they are projected to dominate the semiconductor market over the next decade, delivering significant economic advantages, particularly in the Electric Vehicle (EV) sector with Power Electronic Conversion Systems (PECS) [12,13].

In this study, we introduce a pioneering technology that integrates GaN vertical and lateral devices on a single wafer. This novel integration enables the realization of a high-power switch device that is seamlessly combined with a HEMT-based gate driver, thus enhancing the performance and efficiency of power converters.

A critical challenge in this integration is achieving effective electrical isolation between the GaN devices. The vertical GaN power FinFET is constructed on an n-doped GaN substrate, which is also utilized by the HEMT. This configuration exposes the HEMT's backside to high voltages, potentially compromising its performance [14]. Notably, the high backside voltage can induce significant drift in the threshold voltage (V_{th}) of the GaN HEMT, leading to instability that adversely affects the gate driver output signal. This instability introduces unpredictable timing delays, undermining the switching performance of GaN power devices and diminishing overall power conversion efficiency, which could even result in device failure.

The impact of the substrate voltage on the threshold voltage of the HEMT device is presented in the literature as a major problem that leads to an instability of the device operation mode [15,16]. In this paper, a new approach is proposed to make the device unresponsive to the voltage applied to the back side of the substrate and improve the stability and robustness of the device.

To address this challenge, we utilize TCAD-Sentaurus simulations to investigate a novel isolation technique that separates vertical from lateral GaN transistors on the same wafer (refer to **Figure 1**). This approach aims to advance the integration capabilities of GaN technology and improve device performance in high-power applications.

2. Structure description

To elucidate the influence of bias conditions on GaN-HEMT devices integrated alongside high-power vertical devices on the same die, an additional ohmic contact has been strategically incorporated into the backside of the GaN-HEMT structure, as illustrated in **Figure 2**. This fourth contact facilitates the application of varying voltages, thereby replicating the operational scenarios encountered by the vertical device. Under these tailored conditions, the electrical behavior of the GaN-HEMTs was rigorously examined.

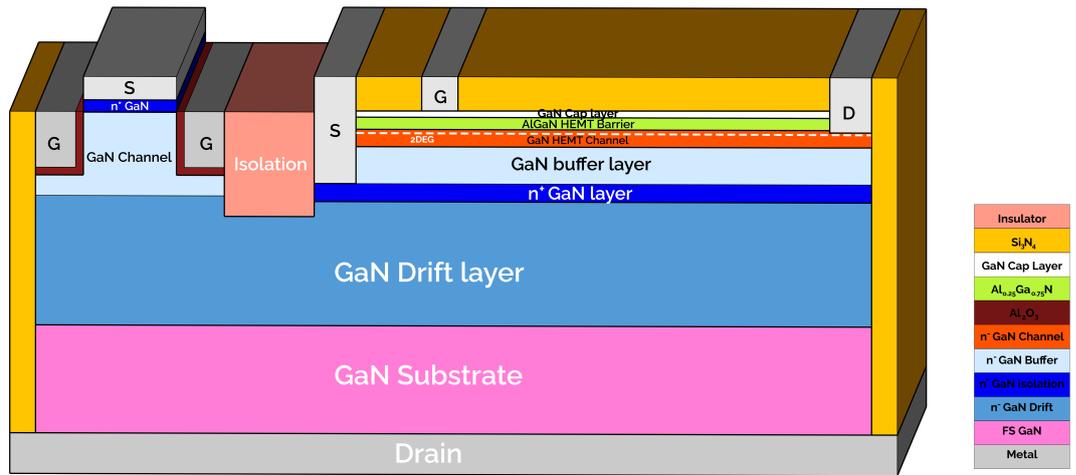


Figure 1. Detailed schematic cross-sectional illustration depicting the advanced monolithic integration of vertical and lateral GaN-based devices on a unified GaN substrate.

The realization of this complex device architecture on actual wafers is achieved through a precise process. Initially, the GaN vertical device's epi-layer structure is grown using epitaxy reactor. Subsequently, the designated HEMT fabrication area undergoes etching down to the drift region. Following this, the HEMT epi-structure is selectively grown within the etched region, employing masking techniques to shield the corresponding GaN vertical device epi-layers.

The comprehensive schematic cross-sectional depiction of the AlGaIn/GaN HEMT structure utilized in the simulation is provided in **Figure 2**. The epitaxial structure, which is grown on a n^+ doped GaN substrate, commences with a 300 nm-thick drift layer. This is followed by the active HEMT region, which is composed of a 500 nm-thick buffer layer, a 50 nm GaN channel layer, a 20 nm AlGaIn layer, and a final 2 nm-thick GaN cap layer.

The GaN HEMT model was developed within Sentaurus TCAD through an extensive calibration procedure. This process relied on empirical data obtained from a HEMT device fabricated by Prof. Hassan Maher's team at Université de Sherbrooke (UdS-LN2). The simulation's physical parameters for the epitaxial layers were carefully adjusted to closely match the characteristics observed in the actual fabricated devices. For instance, electron mobility was calibrated to 1810 $\text{cm}^2/\text{V}\cdot\text{s}$, and the density of deep, single-level trap states was set to $7.8 \times 10^{12} \text{ cm}^{-2}$. While specific citations are not available in this context, these parameters are in alignment with those documented in scholarly literature concerning high-performance GaN HEMTs. As an example, Altuntas et al. reported high-quality AlGaIn/GaN heterostructures exhibiting impressive electrical properties, with a sheet carrier density of $1.28 \times 10^{13} \text{ cm}^{-2}$ and mobility of 1930 $\text{cm}^2/\text{V}\cdot\text{s}$ [17], which are comparable to the values used in this study.

The epitaxial layers thicknesses and doping concentrations are detailed in **Table 1**. The simulation was carried out using the TCAD-Sentaurus Device Simulator by Synopsys Corporation [18]. Calibration of the simulator was based on experimentally measured I-V characteristics from a previously fabricated HEMT device. In this simulation, a reduced thickness of the drift region was used in the vertical device to enhance the effect of the backside electrode voltage on the GaN HEMT device's performance.

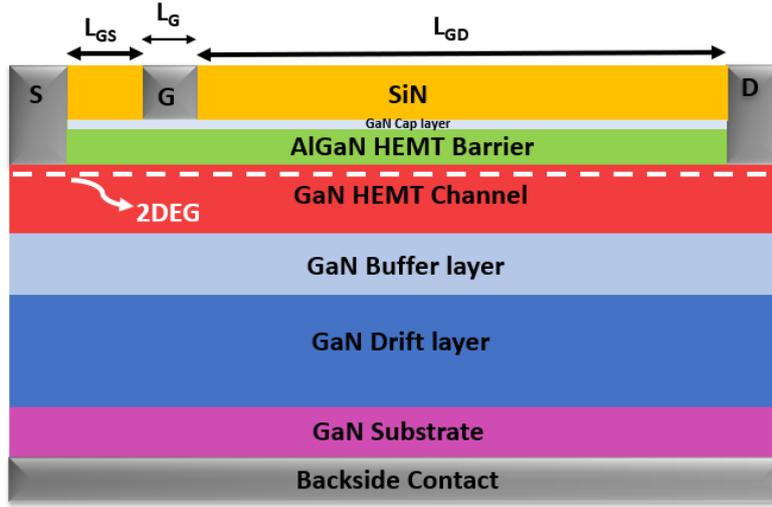


Figure 2. Advanced schematic cross-sectional representation of the AlGaN/GaN HEMT structure, incorporating a strategic backside contact, as implemented in TCAD-Sentaurus simulations.

The source-to-gate (L_{GS}) and drain-to-gate (L_{GD}) extensions used are $0.5 \mu\text{m}$ and $1.5 \mu\text{m}$ respectively, with a gate length (L_G) of $0.4 \mu\text{m}$.

Table 1. Thicknesses and donor doping concentrations of the different layers for the simulated HEMT device by TCAD-Sentaurus.

Layer	Thickness (μm)	Doping concentration (cm^{-3})
GaN Cap	0.002	1×10^{16}
AlGaN	0.02	1×10^{16}
n-GaN HEMT Channel	0.05	1×10^{16}
n-GaN Buffer	0.5	1×10^{16}
n-GaN Drift	0.3	1×10^{16}
n ⁺ GaN Isolation	0.01	1×10^{19}

3. Results and discussion

3.1. Influence of the high voltage applied on the backside contact

After the calibration phase, the GaN epitaxial structure of the HEMT device was modified by adjusting doping concentrations and layer thicknesses to be compatible with the design for vertical device structures intended for monolithic integration, as depicted in **Figure 1**. The outcomes illustrated in **Figure 3** correspond to this modified HEMT structure.

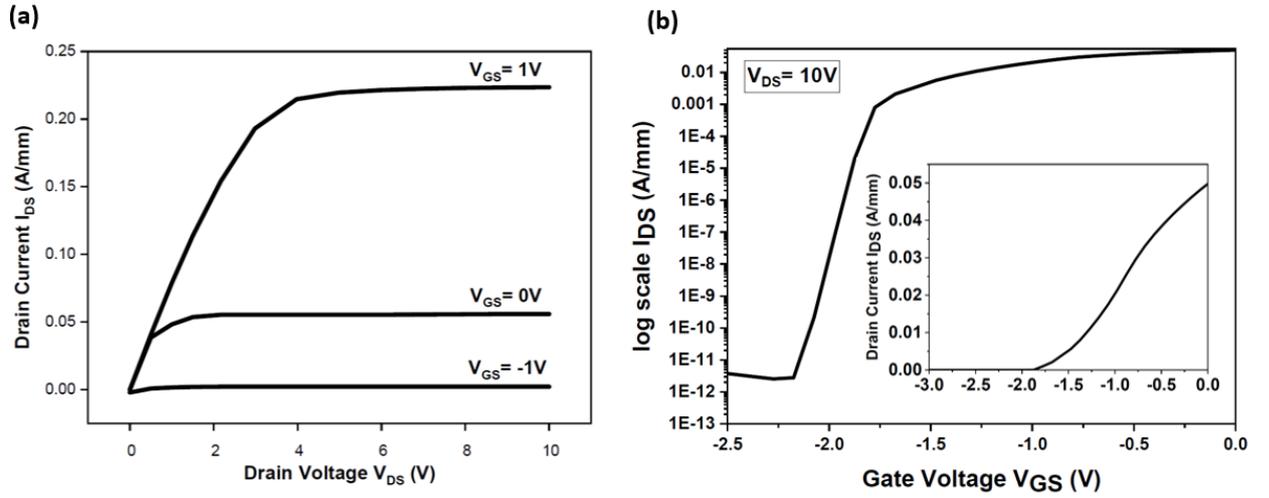


Figure 3. a) $I_{DS}(V_{DS})$ output and b) $I_{DS}(V_{GS})$ transfer characteristics of the GaN HEMT structure simulated by Sentaurus TCAD

The output characteristics depicted in **Figure 3** demonstrate the device's performance across a range of operating conditions, exhibiting good functionality.

Upon completing the calibration, the epi-structure shown in **Figure 2** was employed to analyze the effects of applying high voltage to the backside contact (V_{sub}) of the HEMT. The voltage was varied from $V_{sub} = -50$ V to $+100$ V. **Figure 4-a** shows the output characteristics $I_{DS}(V_{DS})$ obtained at $V_{GS} = 1$ V for different applied backside voltage values.

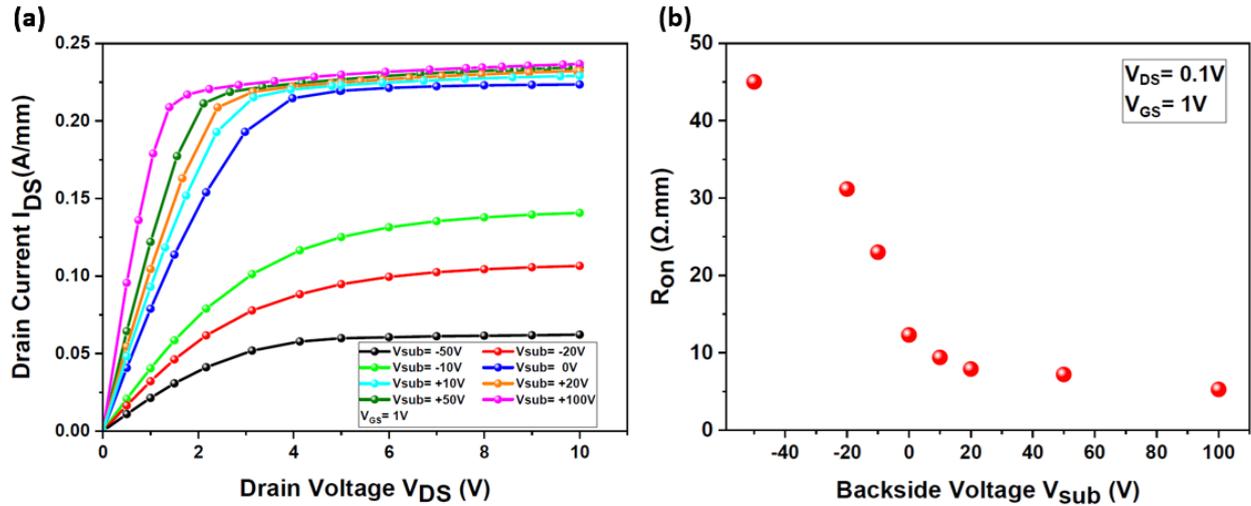


Figure 4. Impact of the applied backside voltage (V_{sub}) on the ON-state Resistance (R_{ON}) of the simulated HEMT: a) $I_{DS}(V_{DS})$ output characteristics of the HEMT for different applied backside voltages (V_{sub}) from -50 V to $+100$ V; b) ON-state resistance variation as a function of V_{sub}

Applying a positive voltage to the backside contact of the HEMT increases the electron sheet density in both the 2DEG channel beneath the gate and the access region. The ON-state Resistance (R_{ON}), derived from the output characteristics under various backside voltages at $V_{DS} = 0.1$ V (**Figure 4-a**), is shown in **Figure 4-b**. Notably, R_{ON} decreases from $45 \Omega \cdot \text{mm}$ to $5.3 \Omega \cdot \text{mm}$ as the applied voltage varies from -50 V and $+100$ V. This reduction in R_{ON} is attributed to the higher free carrier concentration within the 2DEG, as previously discussed. The backside contact functions as an additional gate, directly influencing the drain current of the device [19].

Another critical parameter to assess is the threshold voltage (V_{th}) response to the applied backside voltage. Threshold voltage instability is a significant challenge that must be addressed to advance the use of GaN HEMTs in integrated circuits [20]. **Figure 5-a** illustrates the $I_{DS}(V_{GS})$ transfer characteristics (log scale) of the HEMT with different applied backside voltages ranging from -50 V to $+100$ V, while **Figure 5-b** shows the threshold voltage variation as a function of V_{sub} . Notably, the current study, conducted under conditions of low trap densities, did not reveal significant hysteresis effects. The threshold voltage (V_{th}) is determined at $I_{DS} = 1$ mA/mm. With V_{DS} set to 10 V and V_{sub} at 0 V, the device

exhibits a threshold voltage of -1.7 V. However, when the backside voltage is increased to +100 V, V_{th} shifts negatively to -2.95 V. Conversely, a decrease in V_{sub} to -50 V results in a positive shift in V_{th} to -0.2 V. This significant threshold voltage instability, induced by variations in the backside voltage, can severely impact the output signal of the gate driver circuit and, consequently, the performance of the high-power vertical device. Clearly, this presents a substantial issue that must be resolved to prevent the lateral device from being affected by the polarization conditions of the vertical one.

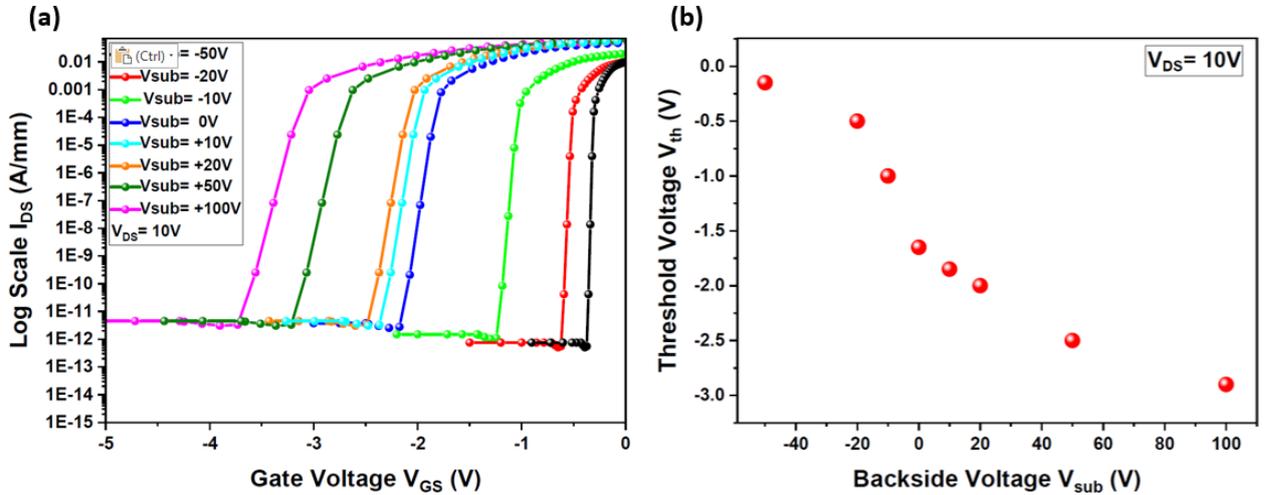


Figure 5. Impact of backside Voltage (V_{sub}) on the threshold Voltage (V_{th}) of the simulated HEMT: a) $I_{DS}(V_{GS})$ transfer characteristics (log scale) of the HEMT under varying backside voltages (V_{sub}) ranging from -50 V to +100 V; b) Variation in threshold voltage as a function of V_{sub} .

3.2. Effective Isolation to Mitigate Backside Voltage Influence on the HEMT Device

To counteract the impact of the backside voltage originating from the monolithically integrated high-power vertical transistor on the HEMT device, efficient electrical isolation between the two devices is essential. To achieve this, a highly n-doped GaN layer (n^+ GaN) is strategically inserted between the epitaxial layers of the two devices. This n^+ GaN layer, connected to the source contact, is designed to enhance the stability of the HEMT device characteristics. By grounding the n^+ GaN layer, it acts as a field-blocking barrier, effectively isolating the HEMT transistor from the voltage applied to the backside of the device.

Figure 6 illustrates the schematic cross-section of the simulated AlGaIn/GaN HEMT structure with the added highly doped n^+ GaN layer. To validate this approach, TCAD simulations were performed with the inclusion of the additional layer, featuring a thickness (t_{iso}) of 10 nm and an n-doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$.

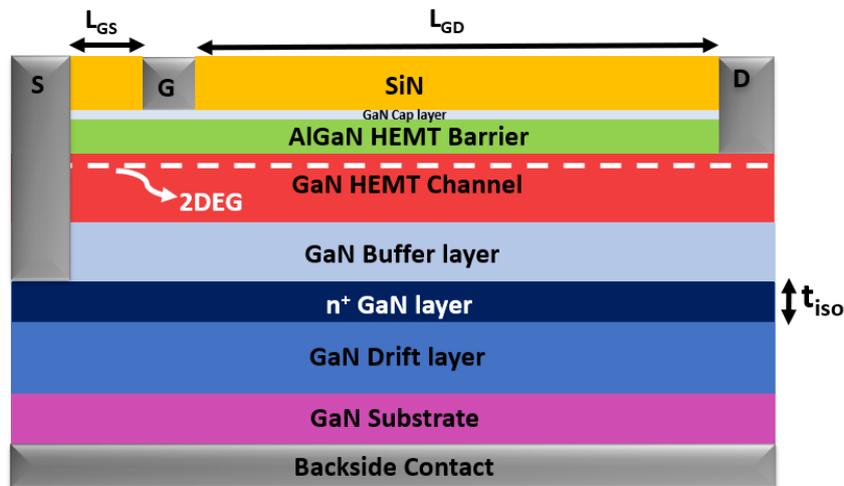


Figure 6. Schematic Cross-Section of the AlGaIn/GaN HEMT Featuring a Backside Contact and n^+ GaN Insulation Layer: The n^+ GaN layer is strategically connected to the source contact, as implemented in the TCAD-Sentaurus simulations.

The output characteristics presented in **Figure 7** demonstrate that the inclusion of the n^+ GaN layer effectively shields the device from the influence of the backside voltage. As the backside voltage is increased from 0 V to +100 V, there is no observable change in the output characteristics, indicating successful isolation. The sub-threshold slope (SS) values for the simulated GaN HEMT with and without the isolation layer are 61.5 mV/decade and 72 mV/decade, respectively. The simulated GaN HEMT demonstrates improved sub-threshold slope (SS) with the isolation layer, achieving 61.5 mV/decade compared to 72 mV/decade without it. This reduction in SS indicates enhanced gate control and switching efficiency. The contrast between the output characteristics of the HEMT with and without the n^+ GaN layer at +100 V backside voltage clearly confirms the effectiveness of this isolation technique, ensuring that the HEMT remains unaffected by the high-power device integrated alongside it.

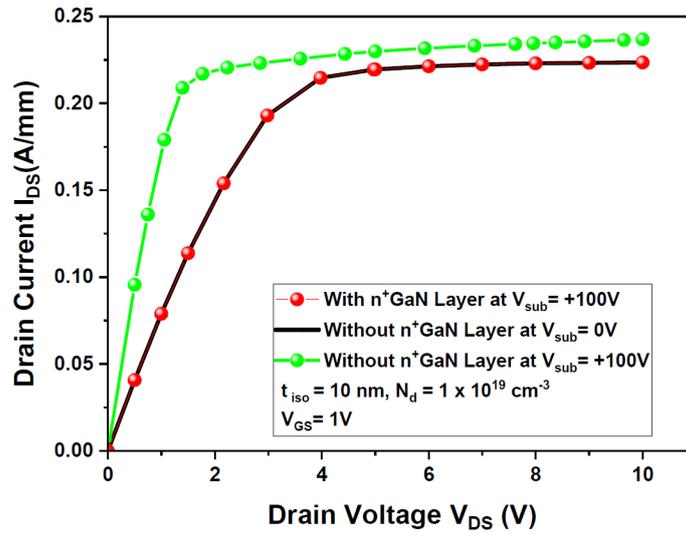


Figure 7. I_{DS} (V_{DS}) output characteristics of the simulated HEMT with and without n^+ GaN layer at $V_{sub} = +100$ V applied on the backside contact.

Figure 8 illustrates the electric field distribution within the HEMT device both with and without the n^+ GaN layer. The results demonstrate that the n^+ GaN effectively blocks the high electric field generated by the backside voltage from reaching the HEMT. Consequently, the 2DEG in the lateral GaN HEMT remains unaffected by the applied backside voltage, ensuring that the device's performance remains stable and free from degradation.

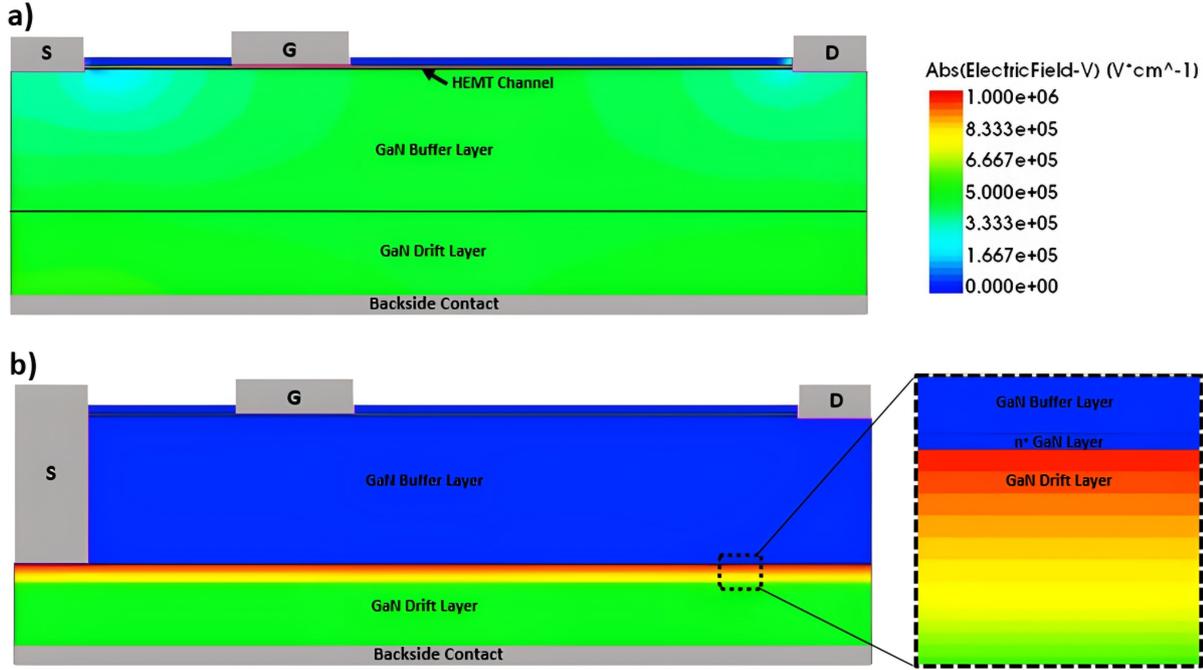


Figure 8. 2D TCAD-Sentaurus simulation of the HEMT showing the electric field distribution at +100 V: a) Without the n⁺ GaN layer, and b) With n⁺ GaN layer, highlighting the differences in electric field distribution across the device layers (zoomed view).

Figure 9-a unveils the output characteristics of the HEMT device across a spectrum of n⁺ GaN isolation layer thicknesses (t_{iso}) doped at $1 \times 10^{19} \text{ cm}^{-3}$ and ranging from 0 nm to 50 nm. The results irrefutably confirm that robust electrical isolation is attained only when the n⁺ GaN layer achieves a pivotal thickness of 10 nm. **Figure 9-b** further reinforces that V_{th} of the HEMT device remains unwaveringly stable at -1.7 V, even under the duress of a formidable backside voltage of up to +100 V, provided that the n⁺ GaN isolation layer upholds this crucial 10 nm minimum thickness. Accordingly, this 10 nm thickness will be rigorously employed in forthcoming simulations to delve into the profound influence of n⁺ GaN layer doping on the isolation capabilities of the device.

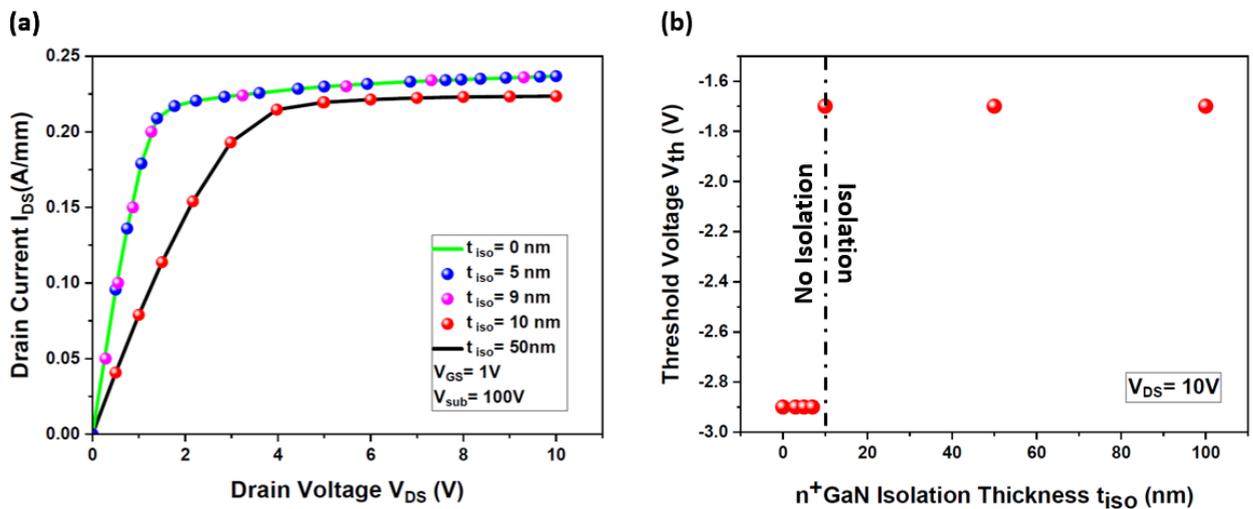


Figure 9. Impact of the thickness of the n⁺ GaN isolation layer (t_{iso}) on the threshold voltage (V_{th}) of the simulated HEMT: a) $I_{DS}(V_{DS})$ output characteristics of the HEMT for different thickness values of n⁺ GaN layer (t_{iso}) at an applied backside voltage $V_{sub} = +100 \text{ V}$; b) threshold voltage variation as a function of t_{iso} . In these simulations, the doping concentration of the n⁺ GaN isolation layer is $N_d = 1 \times 10^{19} \text{ cm}^{-3}$.

We have rigorously examined the isolation efficacy of the n⁺ GaN layer as a function of its doping concentration, spanning from $N_d = 1 \times 10^{16} \text{ cm}^{-3}$ to $N_d = 1 \times 10^{19} \text{ cm}^{-3}$. As depicted in **Figure 10-a**, it becomes evident that doping

concentrations below $1 \times 10^{18} \text{ cm}^{-3}$ render the layer inadequate in mitigating the high electric field emanating from the backside voltage, thereby failing to secure the necessary isolation for the HEMT device. Remarkably, the threshold voltage (V_{th}) exhibits unwavering stability at $V_{th} = -1.7 \text{ V}$, even under the imposition of a substantial backside voltage of $+100 \text{ V}$, provided the doping concentration (N_d) of the n^+ GaN isolation layer meets or exceeds the critical threshold of $1 \times 10^{18} \text{ cm}^{-3}$, as illustrated in **Figure 10-b**. This outcome underscores the quintessential role of the n^+ GaN layer's precise doping specifications in fortifying the HEMT device against the deleterious effects of backside voltage. The strategic selection of doping levels and layer thicknesses emerges as paramount in engineering the requisite electrical isolation between the vertically and laterally integrated devices.

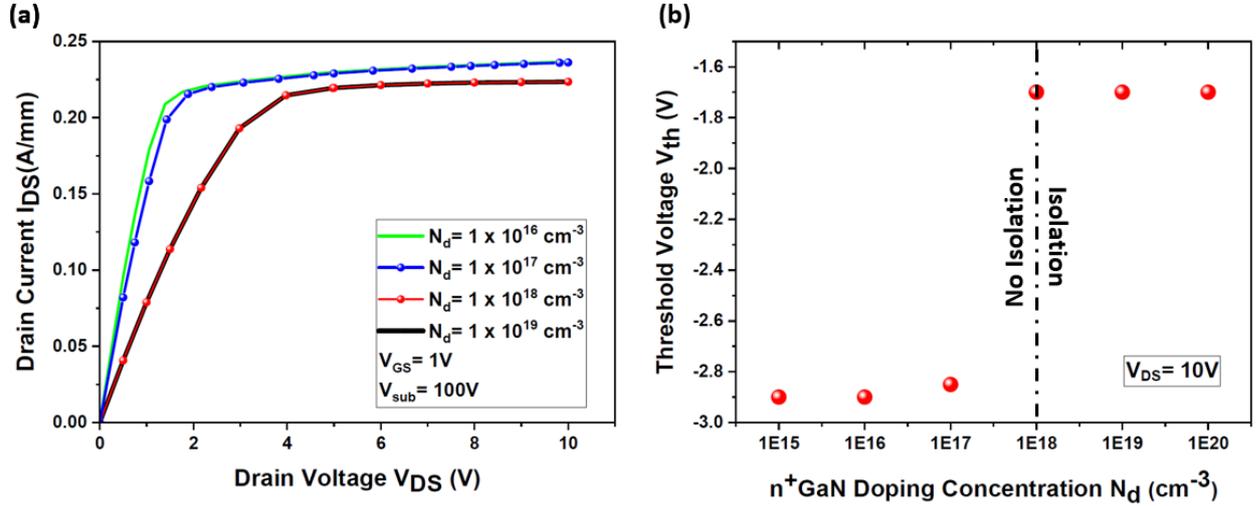


Figure 10. Impact of the doping concentrations of the n^+ GaN layer (N_d) on the threshold voltage (V_{th}) of the simulated HEMT: a) $I_{DS}(V_{DS})$ output characteristics of the HEMT for different doping concentration values of n^+ GaN layer (N_d) at an applied backside voltage $V_{sub} = +100 \text{ V}$; b) threshold voltage variation as a function of N_d . In these simulations, the n^+ GaN isolation layer thickness is equal to 10nm.

The isolation capability of the n^+ layer depends on the quantity of charges present in this layer. These charges will screen the electric field induced by the voltage applied to the device's backside electrode. Thus, for the same V_{sub} , different thicknesses and doping levels will be effective in stabilizing the device's V_{th} . For a thin n^+ layer, the doping must be high enough to achieve our objective. On the other hand, for a thick n^+ layer, the doping can be reduced while maintaining the good isolation behavior of this layer.

4. Conclusions

The monolithic integration of vertical and lateral devices on a single chip is contingent upon achieving robust electrical isolation between these components. To address this, we employed a highly doped n-type GaN layer (n^+ GaN) with a donor concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and a thickness of 10 nm, simulated using TCAD-Sentaurus. The electrical output characteristics, $I_{DS}(V_{DS})$, reveal that without this critical isolation layer, the backside contact effectively acts as a back-gate, destabilizing the device threshold voltage. By incorporating the n^+ GaN layer within the HEMT epi-structure, we successfully neutralize this destabilization, ensuring that the output characteristics remain stable across varying backside voltages. This innovative solution not only resolves a significant obstacle but also paves the way for the reliable monolithic integration of vertical and lateral devices on a unified chip architecture.

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References

1. He Li; Chengcheng Yao; Lixing Fu; Xuan Zhang; Jin Wang Evaluations and Applications of GaN HEMTs for Power Electronics. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia); IEEE: Hefei, China, May 2016; pp. 563–569.
2. Al Taradeh, N.; Frayssinet, E.; Rodriguez, C.; Morancho, F.; Sonnevile, C.; Phung, L.-V.; Soltani, A.; Tendille, F.; Cordier, Y.; Maher, H. Characterization of M-GaN and a-GaN Crystallographic Planes after Being Chemically Etched in TMAH Solution. *Energies* **2021**, *14*, 4241, doi:10.3390/en14144241.
3. Chub, A.; Zdanowski, M.; Blinov, A.; Rabkowski, J. Evaluation of GaN HEMTs for High-Voltage Stage of Isolated DC-DC Converters. In Proceedings of the 2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG); IEEE: Bydgoszcz, Poland, June 2016; pp. 375–379.
4. Su, M.; Chen, C.; Rajan, S. Prospects for the Application of GaN Power Devices in Hybrid Electric Vehicle Drive Systems. *Semicond. Sci. Technol.* **2013**, *28*, 074012, doi:10.1088/0268-1242/28/7/074012.
5. Heckel, T.; Rettner, C.; Marz, M. Fundamental Efficiency Limits in Power Electronic Systems. In Proceedings of the 2015 IEEE International Telecommunications Energy Conference (INTELEC); IEEE: Osaka, Japan, October 2015; pp. 1–6.
6. Li, G.; Wang, W.; Yang, W.; Lin, Y.; Wang, H.; Lin, Z.; Zhou, S. GaN-Based Light-Emitting Diodes on Various Substrates: A Critical Review. *Rep. Prog. Phys.* **2016**, *79*, 056501, doi:10.1088/0034-4885/79/5/056501.
7. Ng, J.H.; Tone, K.; Asubar, J.T.; Tokuda, H.; Kuzuhara, M. High Breakdown Voltage AlGaIn/GaN HEMTs on Free-Standing GaN Substrate. In Proceedings of the 2015 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK); IEEE: Kyoto, Japan, June 2015; pp. 54–55.
8. Chakroun, A.; Jaouad, A.; Bouchilaoun, M.; Arenas, O.; Soltani, A.; Maher, H. Normally-off AlGaIn/GaN MOS-HEMT Using Ultra-Thin Al_{0.45}Ga_{0.55}N Barrier Layer: Normally-off AlGaIn/GaN MOS-HEMT. *Phys. Status Solidi A* **2017**, *214*, 1600836, doi:10.1002/pssa.201600836.
9. Rolland, G.; Rodriguez, C.; Gommé, G.; Boucherif, A.; Chakroun, A.; Bouchilaoun, M.; Pepin, M.C.; El Hamidi, F.; Maher, S.; Arès, R.; et al. High Power Normally-OFF GaN/AlGaIn HEMT with Regrown p Type GaN. *Energies* **2021**, *14*, 6098, doi:10.3390/en14196098.
10. Sun, M.; Pan, M.; Gao, X.; Palacios, T. Vertical GaN Power FET on Bulk GaN Substrate. In Proceedings of the 2016 74th Annual Device Research Conference (DRC); IEEE: Newark, DE, USA, June 2016; pp. 1–2.
11. Pépin, M.-C.; Maher, H.; Rodriguez, C.; Soltani, A. Simulation of a Normally off GaN Vertical Fin Power Fet Transistor to Study Its Breakdown Mechanism 2019.
12. Letellier, A.; Dubois, M.R.; Trovao, J.P.; Maher, H. Gallium Nitride Semiconductors in Power Electronics for Electric Vehicles: Advantages and Challenges. In Proceedings of the 2015 IEEE Vehicle Power and Propulsion Conference (VPPC); IEEE: Montreal, QC, Canada, October 2015; pp. 1–6.
13. Cipolletta, G.; D'Avanzo, G.; Delle Femine, A.; Gallo, D.; Landi, C.; Luiso, M. A Laboratory for Testing E-Mobility Power Electronics. In Proceedings of the 2021 IEEE International Workshop on Metrology for Automotive (MetroAutomotive); IEEE: Bologna, Italy, July 1 2021; pp. 82–87.
14. Zhang, Y.; Sun, M.; Piedra, D.; Hu, J.; Liu, Z.; Lin, Y.; Gao, X.; Shepard, K.; Palacios, T. 1200 V GaN Vertical Fin Power Field-Effect Transistors. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM); IEEE: San Francisco, CA, USA, December 2017; p. 9.2.1-9.2.4.
15. Xia, F.; Sun, H.; Liu, Z.; Xia, X.; Tan, X.; Ma, J.; Zhang, M.; Guo, Z. Investigation of High Threshold Voltage E-Mode AlGaIn/GaN MIS-HEMT with Triple Barrier Layer. *Results in Physics* **2021**, *25*, 104189, doi:10.1016/j.rinp.2021.104189.

16. Mahaboob, I.; Yakimov, M.; Hogan, K.; Rocco, E.; Tozier, S.; Shahedipour-Sandvik, F. Dynamic Control of AlGaIn/GaN HEMT Characteristics by Implementation of a p-GaN Body-Diode-Based Back-Gate. *IEEE J. Electron Devices Soc.* **2019**, *7*, 581–588, doi:10.1109/JEDS.2019.2915097.
17. Altuntas, P.; Lecourt, F.; Cutivet, A.; Defrance, N.; Okada, E.; Leseq, M.; Rennesson, S.; Agboton, A.; Cordier, Y.; Hoel, V.; et al. Power Performance at 40 GHz of AlGaIn/GaN High-Electron Mobility Transistors Grown by Molecular Beam Epitaxy on Si(111) Substrate. *IEEE Electron Device Lett.* **2015**, *36*, 303–305, doi:10.1109/LED.2015.2404358.
18. Sentaurus™ Device User Guide. *Version K-2015.06*.
19. Hwang, Y.-H.; Dong, C.; Hsieh, Y.-L.; Zhu, W.; Ahn, S.; Ren, F.; Pearton, S.J.; Kravchenko, I.I. Improvement of Drain Breakdown Voltage with a Back-Side Gate on AlGaIn/GaN High Electron Mobility Transistors. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2015**, *33*, 042201, doi:10.1116/1.4922022.
20. Dai, P.; Wang, S.; Lu, H. Research on the Reliability of Threshold Voltage Based on GaN High-Electron-Mobility Transistors. *Micromachines* **2024**, *15*, 321, doi:10.3390/mi15030321.