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Tunable isolated gate driver supply for automated switching loss measurement of Power Field Effect Transistors

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***Abstract*—The switching losses of power Field Effect Transistors (FETs) such as Silicon IGBTs, MOSFETs, SiC MOSFETs, GaN HEMTs and Diamond FETs are highly dependent on the gate driver currents. These currents are typically set by gate resistors. However, it is then difficult to change the switching speeds, especially during the characterization of switching losses, and integrate such changes in automated design of experiments. In this work, we report a simple circuit to add margining (trimming) capability to any isolated gate driver DC/DC supply, which can be changed online and controlled by a supervisor through an isolated bidirectional series communication. This technique allows 1024 different positive gate voltage levels, which can then be used for characterization of switching losses. The driving voltages can be adjusted online and the effect on switching speeds is demonstrated experimentally by double pulse tests.**

***Index Terms*—Gate drivers, Field effect transistors, digital control, DC-DC converters, switching loss.**

I. Introduction

Power Field Effect Transistors (FETs) such as Silicon (Si), SiC MOSFETs, GaN HEMTs, Si IGBTs, and Diamond FETs require specific gate driving voltages. For examples, with SiC power MOSFETS, the recommended V_{GS} voltage range can be -4 V / +15 V or -5 V / +20 V [1], [2], or -2 V / +6 V or 0 / 5 V for GaN transistors [3]–[5]. In the case of diamond FETs, transistors based on the depletion of a thick boron doped channel have been demonstrated, with a large range of threshold voltage such as in [6]–[8] and other architectures are also under current development [9]. In all cases, the gate driving voltage levels are typically fixed by an isolated DC/DC converter, which also provides the gate driver power supply. In the half bridge configuration and any derived power converter, the isolation of the gate driver supply is required for the high side power transistor, but can be also implemented for the low side. Most of the commercially available isolated DC/DC converters are with fixed and regulated output voltages such as [10]. These types of regulated isolated DC/DC converters have suitable specifications in terms of DC and AC isolation, power ratings and voltage levels. However, they cannot be adjusted online, for cost, simplicity reasons and as being designed accordingly to specific power devices with typical voltage levels. To adjust the switching speeds of power transistors, and consequently the switching losses, the external gate resistors are set, but cannot be changed online and soldering/unsoldering is required. Other gate driver architectures offer tunable gate current levels [11]–[13], but are not the most commonly used gate driver circuits. In this work, we propose a simple circuit to adjust the positive voltage level of any commercially available isolated, regulated and fixed DC/DC converter for gate driver supply of power FETs. Our circuit can be added to any isolated DC/DC converter in high side and low side. The technique is based on margining (trimming) of a fixed Low Drop Out (LDO) linear regulator, supplied by a fixed isolated DC/DC converter. The margining is done by a microcontroller, which generates a variable voltage from a buffered 10-bit Digital to Analog Converter (DAC), similarly to the technique introduced in [14], [15]. This principle is applied here in the context of automated switching loss measurements, either in Double Pulse Tests [16] or opposition method [17], [18]. A proof of concept is shown here with 1.2 kV SiC power MOSFETs and can be applied to any other power FET. With our technique, the positive gate driving voltage can be adapted online, from a supervisor referenced to the digital ground, which sends the desired voltage level through an isolated UART series communication, and read back the sensed value from a multiple channel 10-bit Analog to Digital Converter (ADC). The important outcome of our approach is that it can be applied to any isolated DC/DC converter, and offers online adjustments of the positive gate driver supply. Moreover, a supervisor can easily change the positive gate driver voltage level, and control design of experiments, for automated characterization, adjust switching speeds and investigate changes in switching losses. It can be noticed that changing the driving voltages are effective to change the switching speeds, but will also have an impact on the on state voltage drop of the power FET.

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II. Approach and design methodology

A. Adjustable regulated voltage through a Digital to Analog Converter

The schematics of the proposed approach is presented in figure 1, as proposed for example in [14], [15]. The core principle is introduced: typically only R_1 and R_2 are used in the feedback resistor bridge of a LDO, to regulate its output voltage, from the input voltage labeled here +20 and as a function of the closed loop control of the feedback voltage (V_{ref}).

This circuit will be connected to the reference potential of the power transistor, its Kelvin Source labeled KS. An extra third branch is added here, through R_3 and a variable voltage source V_{DAC} which can be digitally controlled through a DAC. This added branch allows a source / sink current to flow through R_3, as a function of the V_{DAC} value and the regulated reference voltage V_{ref} at the feedback node of the LDO. The LDO, through its feedback loop, will regulate and maintain V_{ref}, which is also the voltage drop across R_2. The current derived from the third branch will modify the output voltage. The equations 1 to 4 are describing the different design parameters: equation 1 calculates a scaling factor k, from the desired range of the output voltage (V_M and V_m are respectively the maximum and minimum output voltage), the maximum DAC output voltage V_{DM} and the internal reference voltage of the LDO V_{ref}. The minimum output voltage of the DAC is assumed to be 0 V. Equations 2 and 3 show the relationship between the three resistors R_1, R_2, R_3 and the scaling factor k. Equation 4 calculates the evolution of the LDO output voltage V_{cc} as a function of the DAC voltage V_{DAC}. The DC transfer characteristics of the LDO output voltage, as a function of the V_{DAC} value is plotted in figure 2. Although the LDO internal feedback voltage V_{ref} is maintained at 1.235 V, the output of the LDO can be adjusted over a wide range, here from 18.6 V to 5.1 V, through a DAC voltage ranging from 0 to 3.3 V. These values comply with the chosen LDO (reference: LP2951), and the desired output voltage range.

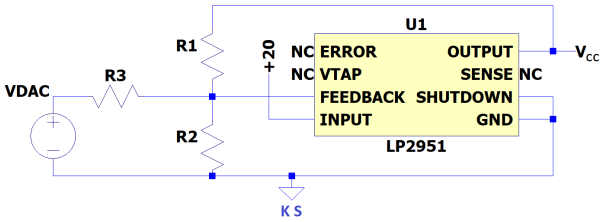

Fig. 1. Schematics of a LDO with an additional third branch for margining (trimming) through R_3 and V_{DAC}. Capacitors are not shown, for clarity.

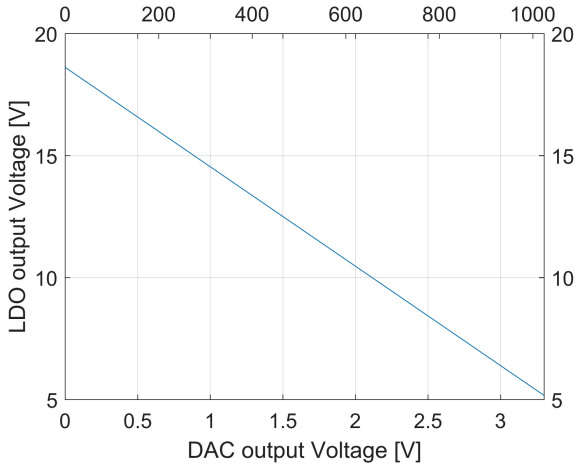

Fig. 2. Variable output voltage V_{cc} as a function of DAC output voltage achieving margining of the fixed LDO. The parameters are: $R_1 = 110k\Omega$, $R_2 = 11k\Omega$, $R_3 = 27k\Omega$ and $V_{ref} = 1.235$ V (accordingly to its datasheet). The top X-axis represents the digital value of the DAC (10 bits, from 0 to 1023, corresponding to voltages from 0 V to 3.3 V).

$$k = \frac{V_{ref} \cdot (V_M - V_m)}{V_{ref} \cdot (V_m - V_M - V_{DM}) + V_{DM} \cdot V_M} \quad (1)$$

$$R_1 = \frac{k \cdot R_3 \cdot (V_M - V_{ref})}{V_{ref} \cdot (k+1)} \quad (2)$$

$$R_2 = k \cdot R_3 \quad (3)$$

$$V_{cc} = \frac{V_{ref} \cdot (R_1 \cdot R_2 + R_1 \cdot R_3 + R_2 \cdot R_3)}{R_2 \cdot R_3} - \frac{V_{DAC} \cdot R_1 \cdot R_2}{R_2 \cdot R_3} \quad (4)$$

Even with such a wide range of adjustable output voltages from a small range of DAC voltages, the resolution is expressed by equation 5, where $nbBitDAC$ is the resolution of the DAC, V_{DM} the maximum DAC output voltage and ΔV_{cc} the resolution at LDO output. With the parameters used in figure 2 and a 10 bit DAC, the resolution at the output ΔV_{cc} is 13.1 mV. These equations considered only the DC performances of the trimmed LDO, while transient performances must be further investigated (e.g. start up, transient response to load or trim voltage changes).

$$\Delta V_{cc} = \frac{V_{DM} \cdot R_1 \cdot R_2}{R_2 \cdot R_3 \cdot 2^{nbBitDAC}} \quad (5)$$

B. Design of the isolated gate driver supply with adjustable voltages

In a half bridge converter, both the low side and high side power FETs must be each driven by a dedicated isolated gate driver, connected to its respective isolated gate drivers supply. Hence, the simple schematics of figure 1 could be applied directly to the low side FET, whose Kelvin Source reference could be connected to the control or digital ground. However, this cannot be applied as is for the high side FET, where static and dynamic isolation is required between the Kelvin

N. Rouger and F. Devilliers, "Tunable Isolated Gate Driver Supply for Automated Switching Loss Measuremen

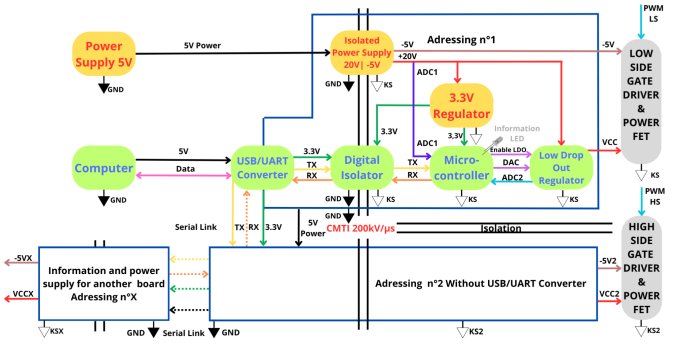

Fig. 3. Principle of isolated gate driver supply with adjustable voltages, applied identically at High Side and Low Side, with isolated digital control.

Source and the control or digital ground. In this context, the principle of margining a LDO through a variable voltage has been applied for a fully isolated gate driver supply, which can be applied both at high side and low side. The schematics of the whole circuit is shown in figure 3.

Compared to the simple schematics of figure 1, an additional isolated DC/DC converter is added, with fixed output voltages. A 2W Murata isolated DC/DC converter is used, with a 5V supply at the primary side, and a +20 V / -5 V isolated dual output (ref: MGJ2D052005SC), referenced to the Kelvin Source of the power transistor (floating reference). The isolated +20 V is then connected to a LDO (ref: LP2951) with a fixed resistor divider and also referenced to the Kelvin Source (KS). A third connection is added to the buffered 10-bit DAC output of a simple microcontroller (ref: PIC16F1769, 8 bit architecture), which is also referenced to the Kelvin Source and supplied through a fixed 3.3V LDO (ref: L78L33) connected to +20 V output of the isolated DC/DC converter. This third connection realizes the margining of the LDO, according to figure 1 and associated equations 1 to 5. The microcontroller is clocked by the internal 32 MHz oscillator.

Taking benefits of the microcontroller referenced to the Kelvin Source, an ADC peripheral is connected to two channels: the +20 V output of the isolated DC/DC, and the output of the LDO which is controlled through margining. Both channels are sensed through resistor dividers, to comply with maximum voltages of 3.3 V. From a digital control point of view, a supervisor sends the requests for voltage change or read the data. The supervisor is referenced to the external digital ground, labeled GND in figure 3, isolated from the Kelvin Source of the power transistor. The supervisor sends different requests, through an USB // UART bridge (ref: MCP2221A), followed by a digital bidirectional isolator (ref: ADUM341E). The microcontroller reads UART hex codes, which can be programmed to any desired behavior. As a first proof of concept, a simple bidirectional communication has been programmed, where the microcontroller waits for a byte AA as a code to adjust the DAC value. This code for action is then followed by the 8 most significant bits of the desired DAC value in hexadecimal. For example, the host can send AA 00 to set $V_{DAC} = 0$ V, or AA 80 to set the hex value of 80, which results in $V_{DAC} = 3.3V \cdot \frac{512}{1023}$ V (considering the two less significant bits of the 10 bit DAC are 00, and 80 for the 8 MSB, so 512 in decimal for 80). The relationship between V_{DAC} and the output voltage was given in equation 4 and figure 2. At the moment, one single host can send the same UART code to all boards, which will react while adjusting the DAC values to the same requested values. As a next step, an address can be programmed in each gate driver supply board, for a single host to address to a specific board, while keeping a simple UART communication. It is also possible to send an ADC reading request from the host: if the microcontroller receives a byte FF, the microcontroller will read both channels and send back 6 bytes such as $AD\ C1\ XX\ AD\ C2\ YY$. The values XX and YY correspond to the reading of the ADCs connected to +20 V and the output pin of the LDO between 0 and 3.3 V (8 Most Significant Bits), referenced to the floating Kelvin Source. Thanks to the microcontroller, it is also possible to give some additional feedback such as a blinking LED, whose frequency or intensity can be a function of the measured ADC values, and Under/Over Voltage LockOut. The shutdown pin of the LDO is also controlled digitally through the microcontroller, to ensure safe operation and remove a risk of false driving. The references for the chosen circuits were mentioned here as an application example: many other references can be used in place of the proposed ones. For example, any simple microcontroller with a DAC, ADC, UART RX and TX can be used. Although this circuit looks rather ”complex”, it is actually very similar to a typical isolated gate driver supply and gate driver board; only an extra isolated bidirectional communication is required, which can be already offered by the PWM isolator circuit, and also a microcontroller referenced to the Kelvin Source.

III. Experimental results and proof of concept

A. Digitally controlled isolated gate driver power supply

The schematics and principle have been validated experimentally with and without power FETs. First tests are done without any power FET, with the circuit described previously in figure 1 and 3, and a 1 μF capacitor + 1 kΩ resistor as loads. Figure 4 shows the adjustment of the positive voltage through various codes generated by the supervisor, with action AA for DAC margining, followed by different values. The isolated positive voltage can be easily controlled as demonstrated. It can be noticed that the transient response must be further analyzed under these specific load conditions. Five different output voltages V_{cc} were recorded, and one example is shown for triggering signal and DAC output V_{DAC} change corresponding to a change at the LDO output from 6 V to 18.5 V.

Figure 5 shows the received data at the supervisor, following a reading request sent by the supervisor, which then reads values of the first channel ADC (here +20 V) and second channel ADC (here +12.5 V) in hex.

N. Rouger and F. Devilliers, "Tunable Isolated Gate Driver Supply for Automated Switching Loss Measuremen

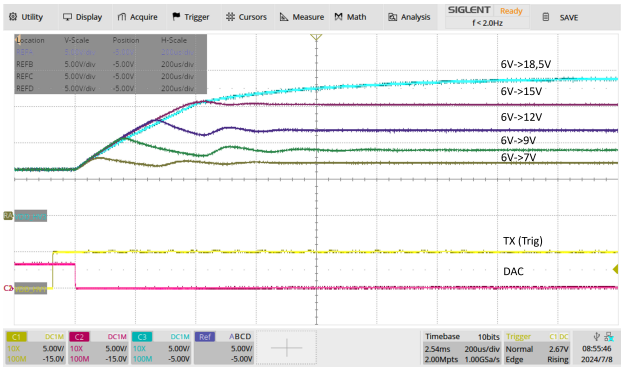

Fig. 4. Digital control of LDO over UART.

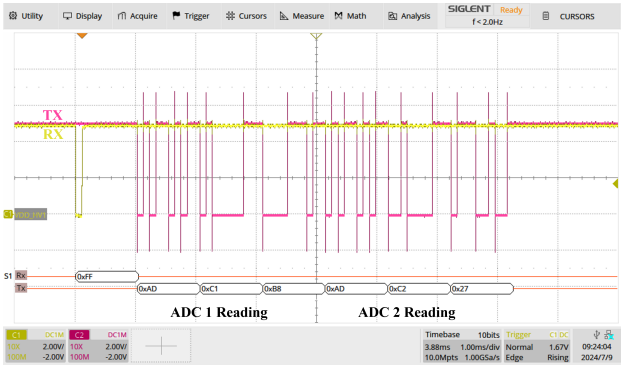

Fig. 5. ADC reading following an UART request.

B. Digital control of switching speeds

The circuit has then been connected to an evaluation board from Infineon (ref: EVAL-1ED3142MU12F-SIC), a half bridge power board which includes two isolated gate drivers (ref: 1ED3142MU12F) and 1.2 kV 20 $m\Omega$ SiC MOSFETs (ref: IMZA120R020M1H), but does not include the isolated gate driver supplies for high side and low side transistors. PWM signals are generated by another microcontroller, which produces synchronized PWM signals for high side and low side devices. Two identical Printed Circuit Boards (PCB) of the tunable isolated gate driver supply circuits have been fabricated and connected to the evaluation board, as shown in figure 6. The two PCBs are connected to the same UART host via the USB // UART bridge (MCP2221A). As a consequence, each board RX receives the same TX signal sent from host and further adjust the isolated voltage values, but only one PCB sends back the ADC values to the host RX and one microcontroller TX. The input capacitor of one SiC power MOSFET is around 3.5 nF, which requires around 140 mW when driven at 100 kHz and with a 20 V V_{GS} amplitude. Considering a typical total gate charge of 109 nC when switching 800 V, 41 A and 20 V V_{GS} amplitude, the minimum isolated gate driver power is 218 mW at 100 kHz.

Figure 7 shows the successful online change of the isolated gate driver supply positive voltages, when operating for example at a PWM frequency of 50 kHz and changing by UART

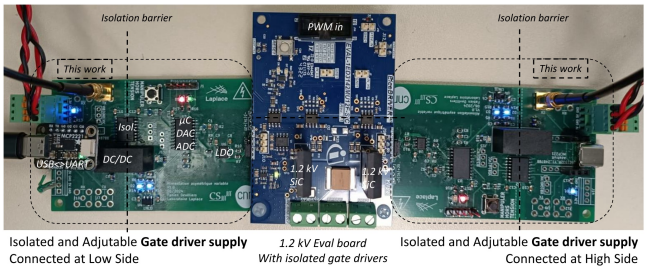

Fig. 6. Two boards connected to a half bridge.

host from 12.1 V to 18.6 V while sending AA 80 (12.1 V) and then AA 00 (18.6 V). To improve clarity and show both high side and low side V_{GS}, the dead time was increased to 1.28 μs. Please note that for these tests, the high voltage DC bus voltage was null, meaning that there was no Miller plateau neither power switching. Figure 7 also shows a zoom at turn OFF (high side) and turn ON (low side), with a dead time reduced to 300 ns and three values of positive gate driver supply voltages adjusted by the UART host from 12.1 V to 18.6 V at the same time for both high side and low side. At low side, V_{GS} and the digitally adjusted positive voltage V_{cc} were probed by a passive voltage probe with KS as reference (200 MHz bandwidth), whereas at high side, V_{GS} was probed with a 150 MHz differential probe. A 180 MHz 4 channel oscilloscope was used, with 10 bit resolution for these tests, limiting the bandwidth at 100 MHz. These results confirm the correct operation during PWM and that V_{GS} voltages at both high side and low side can be easily adjusted online through the single UART host.

Various operating points have been measured, during continuous PWM operation of both high side and low side gate drivers, each supplied by a dedicated PCB with our proposed technique as in figure 6. The 1.2 kV SiC MOSFETs were connected and driven, providing the required gate charge at high side and low side. The DC current supplied to both PCBs has been measured, while supplying 5V, as labeled *5V Power* in figure 3. The measured DC power is shown in table I. The power measured at the primary side of the DC/DC converters represents the total power supplied to both gate driver supply boards (including digital isolator, LEDs, microcontroller, minimum load at output of DC/DC), the secondary sides of the isolated gate drivers in the half bridge, and the gate charge of both power FETs. The measurements confirm the correct operation under various conditions. At 200 kHz and the highest voltage setting of isolated driver supply (i.e. lowest DAC value), the total output current is limited by the isolated DC/DC converters, leading to a maximum voltage of 18 V.

To confirm the capability of the tunable isolated gate driver supply to further impact the switching losses, double pulse tests were performed. A high voltage low power DC voltage source was connected to the half bridge evaluation board, with

N. Rouger and F. Devilliers, "Tunable Isolated Gate Driver Supply for Automated Switching Loss Measuremen

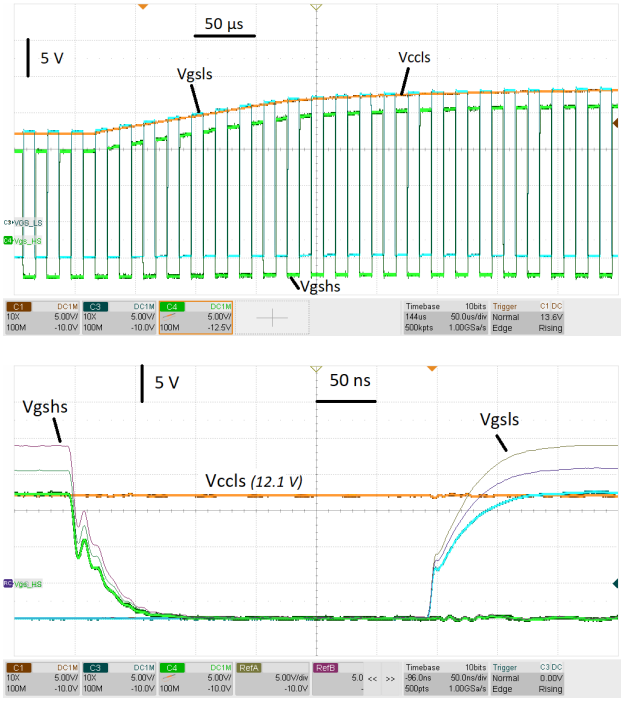

Fig. 7. Change of PWM V_{GS} during operation at both high side and low side. Top: the isolated gate driver supply is changed by UART at both high side and low side, during PWM operation. Please note that the V_{GShs}'s reference has been shifted down to improve clarity. Bottom: zoom at the V_{GShs}, V_{GSls} and dead time, for three different isolated gate driver supply values adjusted by UART.

an additional decoupling capacitor. A 180 μH inductance was connected in parallel of the high side power FET, and the same configuration of figure 6 was used, with two PCBs for high side and low side, driven by the same UART host. The double pulse signal for the low side transistor was generated by another microcontroller with a 2.5 ns time resolution, with a typical duration of 13 μs and 1.3 μs for the first and second pulses. The zoom at the low side turn ON at 200 V and 15 A is shown in figure 8. The inductor current was probed with a current probe (hall effect), the low side Drain to Source voltage was probed by a 150 MHz differential probe, and its Gate to Kelvin Source voltage probed by a 200 MHz passive

Sw. freq.	Adj. voltage	DC current	DC power
0 kHz	18.6 V	465 mA	2.33 W
0 kHz	12.2 V	440 mA	2.20 W
50 kHz	18.6 V	530 mA	2.65 W
50 kHz	12.2 V	490 mA	2.44 W
100 kHz	18.6 V	590 mA	2.95 W
100 kHz	12.2 V	530 mA	2.65 W
200 kHz	18 V	707 mA	3.5 W

TABLE I

MEASURED POWER CONSUMPTION OF THE ISOLATED GATE DRIVER UNDER VARIOUS CONDITIONS. MEASURED AT 5V POWER (PRIMARY SIDE OF THE ISOLATED DC/DC CONVERTER). TWO BOARDS ARE CONNECTED TO THE SAME PRIMARY (I.E. TOTAL POWER FOR HIGH SIDE AND LOW SIDE) AND LOADED BY THE HALF BRIDGE BOARD WITH TWO POWER FETS.

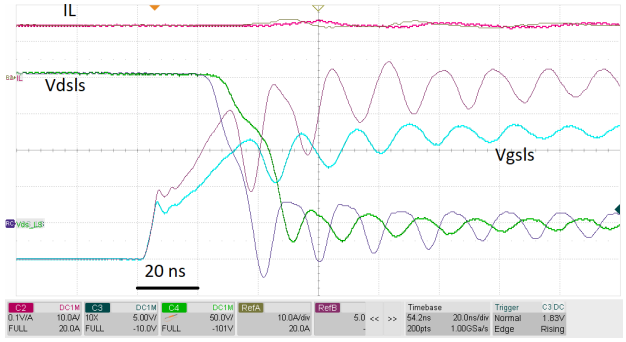

Fig. 8. Double Pulse Test at 200 V and 15 A, for two values of positive driving voltages: zoom at the turn ON of the active transistor (Low Side).

probe, connected to a four channel oscilloscope in 8 bit resolution. Two double pulse sequences were recorded, for two values of the adjusted positive driving voltage (AA 80, 12.1 V and AA 00, 18.6 V). The switching speed is easily controlled by the UART host, under the same other conditions.

IV. AVAILABILITY OF SOURCE CODES, SCHEMATICS, PRODUCTION FILES, AND FUTURE WORKS

The complete schematics, Gerber files and microcontroller codes are available in a Gitlab repository [19] with open source licenses. The same approach can be applied to any other specification, such as other isolated gate driver supply power levels, driving voltages, isolation levels or switching frequencies. Future works will consider an additional address code in the series communication, from the TX host to the multiple RX PCBs. Different addresses will be programmed to each board (or stored to a memory), for high side and low side, and multiple commutation cells. This way, only one supervisor will be able to change any chosen isolated DC/DC gate driver supply related to the programmed address of the microcontroller used in the margining approach. Similarly, at the moment only one board TX can communicate to the host RX, to receive the measured and digitized values of the ADCs. A change in hardware schematics can remove this limitation, with diodes and pull up resistors or logic gates, to share the RX bus with multiple TX from the PCBs (albeit without simultaneous communication). In the experiments, further tests can be done in double pulse at nominal power, with the High side power FET as active switch, and a load inductor in parallel to the passive low side switch. Moreover, tests in continuous mode operation (sync DC/DC or half bridge inverter) can be done, also at nominal power, to confirm the correct operation. Finally, further integration in automated tests and design of experiments will be offered by our contribution, for example with a Python supervisor that can communicate with the PWM signal generators, the proposed UART channel for driving voltages adjustments, and hardware (oscilloscope, voltage source, ...). Additional functionalities can be implemented in the microcontroller, for example to reduce its consumption

N. Rouger and F. Devilliers, "Tunable Isolated Gate Driver Supply for Automated Switching Loss Measuremen

while using a sleep mode and reducing its clock frequency. Finally, zener diodes can be added to prevent any risk of dangerous voltages at the microcontroller I/O.

V. Conclusion

We have successfully introduced a circuit to adjust the positive voltage of fixed isolated DC/DC converters for gate drivers. This circuit offers the capability for automated switching losses measurements, without having to solder / unsolder gate resistors, and online adjustment of the positive gate driving voltage level. Experimental results show the online adjustment of the driving voltages following UART requests, and effect on switching speeds in double pulse tests. The codes and schematics are available in open access in a public repository. The digitally controlled isolated gate driver supply offer an additional degree of freedom both in operation and for characterization, an easy integration with a cross platform supervisor and further automation.

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