Losses Analysis of a Three-Phase Bidirectional Active Split Source Inverter for Traction Applications

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Losses Analysis of a Three-Phase Bidirectional Active Split Source Inverter for Traction Applications

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***Abstract*—In automotive applications, industrials use DC-DC boosting stages interfaced upstream of the Voltage Source Inverter (VSI) to increase the DC bus voltage. These topologies enable the motors to be driven with higher DC bus voltage than that delivered by the battery. Apparently, the use of extra DC-DC converter decreases the efficiency of the whole system. Recently a single-stage topology called the Split Source Inverter (SSI) was derived. This topology enables the boosting function. Unfortunatly, it exhibits very poor utilization of the DC bus voltage, thus preventing its use for traction applications. In previous work, the authors introduced a new single-stage topology called the Bidirectional Active Split Source Inverter (B-ASSI). It enables the boosting function with bidirectional power flow capability and a large utilization of the DC bus voltage. However, its efficiency was not thoroughly studied and comparison with conventionnal two-stage solution not conducted. This paper proposes an in-depth losses analysis of the B-ASSI. Analytical expression of the currents are proposed and validated by simulation. An extensive experimental validations are carry out on a permanent magnet synchronous machine (PMSM) test-bench. The derived expressions and proposed approadh enables a theoretical comparison of the B-ASSI to two-stage solutions and to the SSI but also giving insights about the design of the converter. This theoretical comparison is performed on a normalized driving cycle. It demonstrates that for the given design constraints the B-ASSI exhibits lower losses than the classical two-stage solution and the SSI for low-speed operating conditions corresponding to urban drive profiles.**

***Index Terms*—DC–AC converter, Voltage source inverter (VSI), single-stage converter, Z-source inverter (ZSI), Split Source inverter (SSI)**

I. Introduction

In automotive applications, the DC voltage provided by the battery can fluctuate widely depending on the state of charge of the battery. Furthermore, at high speeds, the usage of flux weakening strategies may impact efficiency. To maintain a higher and constant DC bus voltage, a second stage of conversion has been added to boost the battery voltage. This enables the motor to be fed with a higher voltage, increasing the maximal speed and maximal output power achievable by the drive. Those solutions also benefit from the delayed use of flux-weakening strategies. In recent years, these boosting topologies have gained momentum and have been adopted in some commercial vehicles [1], [2].

Recently, an attractive single-stage topology called the split source inverter (SSI) has been proposed [3]. This architecture presented in Fig. 1a, offers several advantages, such as a continuous input current and a low component count.

The SSI nevertheless suffers from unequal current distribution and stresses among its switches. Furthermore, the SSI suffers from a low DC bus voltage utilization ratio, meaning that an over elevation of V_{DC} is necessary than what would be required with a two-stage solution. This, in turn, will increase the losses.

While the SSI has gained interest in the literature, a few alternative architectures and modulation schemes have been proposed [4]–[6]. In [7], the authors replace the input diode with active switches to enable bidirectional power flow. Another study in [8] attempts to reduce component count and cost of the SSI but does not address the low DC bus utilization ratio issue. Various studies [9]–[13] propose variation of the SSI to increase boost factor. However, these increased boost factors exacerbate the issue of low DC bus utilization ratio and lead to increased costs due to higher voltage stresses on the switches.

The authors in [14] propose a topology called the Active Split Source inverter (ASSI) to address the low DC bus voltage utilization ratio of the SSI. However, the topology has only been proposed for photovoltaic single-phase applications with unidirectional power flow. In automotive applications, the regenerative braking necessitates the use of an three-phase inverter with bidirectional power flow capability.

Lately, a new topology based on the ASSI was dervied in [15]. This topology called the Bidirectional Active Split Source Inverter (B-ASSI) is a three-phase converter and has bidirectional power flow capability. It addresses the inherent limitation of the SSI which presents a very low DC bus voltage utilization ratio. Althougt the B-ASSI was modeled and analyzed in [15], its extensive losses analysis was not carried out. To the authors knowledge, the losses analysis are also not yet addressed for three-phase split source topologies. The B-ASSI being a complex topology with numerous possible satte, the expression of the RMS currents, responsible for conduction losses, are not easily derived. This paper aims to analyze the losses of the B-ASSI and propose an analytical comparison between the B-ASSI, the SSI and the classical two-stage solution of a DC-DC Boost with VSI.

This paper is organized as follows : In Section II, the previously proposed B-ASSI and its working principle are recalled. Section III briefly presents the modulation scheme implemented for the B-ASSI, which will be needed for the losses analysis. Section IV presents the main contribution of this paper, consisting of the losses analysis highlighting the

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merits of the B-ASSI. A new and extensive experimental validation will be presented for both the working principle and the losses analysis in Section V. Finally, Section VI concludes with a theoretical efficiency analysis on normalized drive cycles for the considered application.

II. Working principle of the Bidirectional Active Split-Source Inverter

The topology of the B-ASSI is presented in Fig. 1b. The process to change an initial inductor charging state during an active state V_{100} to a discharging state is depicted in Fig. 2. The new degree of freedom (Dof) in the inductor discharging time in any active state is conserved.

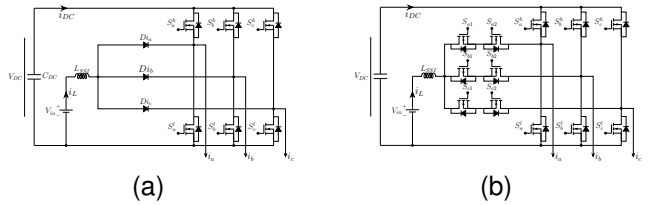

Fig. 1. Existing split source topologies, (a) - three-phase uniderectionnal SSI [3], (b) - three-phase bidirectional Active Split Source Inverter in [15]

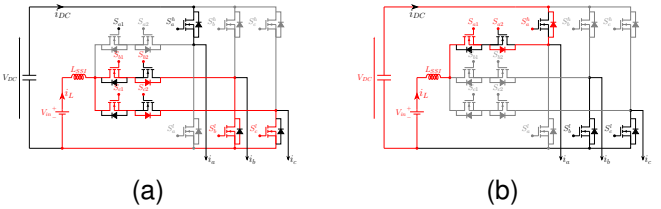

Fig. 2. One possible active state for both Inductor Charging (also possible for the SSI)) and Discharging state (impossible state for a classical SSI). V_{100} Inductor Discharging and Charging

The averaged model of the converter is thus expressed by (1).

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_{DC}} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-M_{DC}}{L_{SSI}} \\ \frac{1-M_{DC}}{C_{DC}} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_{DC} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{SSI}} & 0 \\ 0 & -\frac{1}{C_{DC}} \end{bmatrix} \begin{bmatrix} V_{in} \\ i_{load} \end{bmatrix} \quad (1)$$

Where M_{DC} represents the elevation ratio, and i_{load} the equivalent current absorbed by the machine.

And the static characteristic can be obtained and is unchanged since it is expressed as (2).

$$\frac{V_{DC}}{V_{in}} = \frac{1}{1-M_{DC}} \quad (2)$$

III. Modulation Scheme

A. Generation of the duty cycles

The modulation of the B-ASSI was proposed in [15] and is reminded here since the losses analysis will consider the definition of those duty cycles. For simplicity, only the motor mode is secribed here. The modulation is designed specifically to enable simple modelling of the B-ASSI, it also limits the number of states and simplifies the loss analysis. The modulation is presented in Fig. 3. Overall it enables the avoidance of undesired states of the converter. Namely, the continuity of the inductor current must be ensured : The three clamping switches S_{a1}, S_{b1} and S_{c1} should not be turned off simultaneously. The clamping switches S_{a1}, S_{b1} and S_{c1} as well as S_{a2}, S_{b2} and S_{c2} must not create a state where the DC bus would be experiencing a shoot-through phenomenon, dead-times are also still mandatory. The proposed modulation scheme that respects all three conditions is illustrated in Fig. 3. The general scheme is depicted for phase A only. The duty cycles of the phases of the inverter α_{abc} are always clamped to unity. Their lower envelope is set by the actual modulation index M_{ac}, meaning there are fixed by the load operating conditions. Since the value of M_{DC} can be controlled independently, three new duty cycles are generated for the switches S_{abc1}. Those duty cycles α_{abc1} can be adjusted to change the desired DC bus voltage. The duty cycles generate the inverse command signals. After comparison with a triangular carrier, the results requires to be complemented to obtain the correct command signals C_{abc1}. In this mode of operation, since the α_{abc} are clamped, it is referred as saturated operation mode.

If the desired V_{DC} is high enough, such that $M_{DC} \geq M_{ac}$, there is no need to discharge the inductor during an active state. The B-ASSI can then be operated as a classical SSI, with the inductor discharging only in the zero-sequence state V_{111}. This mode of operation is called the non-saturated mode. The switches S_{abc1} need to be always ON and thus their duty cycles are set to 0 since the command signals are NOT-ed. The additional duty cycles α_{abc1} can thus be expressed by (3).

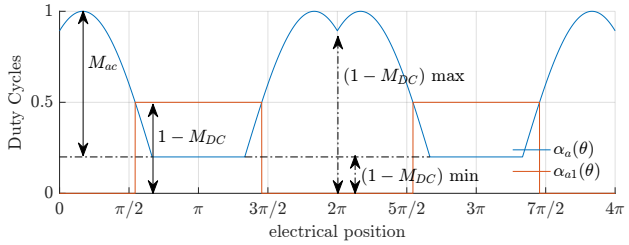

Fig. 3. Definition of the proposed Modulation for phase A in one switching cycle.

$$\alpha_{abc1} = \begin{cases} (1-M_{DC}) & \text{when } (1-M_{DC}) \geq \alpha_{abc} \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

In the case of tis non-saturated mode, the lower envelope of the duty cycles α_{abc} is determinates by the desired V_{DC}, whereas in saturated mode, it is determinated by the load operating condition . The lower envelope of the duty cycles α_{abc} can be set by (4).

$$\begin{cases} (1-M_{DC}) & \text{when } M_{ac} \leq M_{DC} \\ (1-M_{ac}) & \text{when } M_{ac} > M_{DC} \end{cases} \quad (4)$$

The Fig. 4 illustrates the DoF of the B-ASSI over the SSI. Since the inductor discharging time can be freely controlled, the DC bus voltage can be minimized by maximazing the

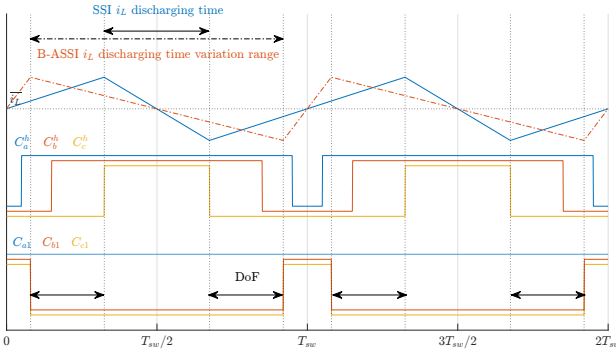

Fig. 4. Illustration of the degree of freedom in inductor current discharging time in one switching period

discharging time. This results in lower voltage stress for the B-ASSI compared to the SSI under the same load operating condition. However, for safety reasons, a new restriction is imposed on the maximal duration of the inductor discharging time. It is expressed as $M_{DC} \geq (1-\sqrt{3}/2)\cdot M_{ac}$. This will in turn mean that a minimal elevated V_{DC} is still required. The minimal elevation ratio as a function of the modulation index is stated by equation (5) :

$$\frac{V_{DC}}{V_{in}} \geq \frac{1}{1-\frac{2-\sqrt{3}}{2}\cdot M_{ac}} \tag{5}$$

IV. Losses and Stresses Analysis

With the gained degree of freedom, the DC bus voltage V_{DC} does not need to be elevated as much as the SSI to attain the same phase voltage. Depending on the sizing and the boost ratio required for the application, this could result in the selection of lower component ratings, which could be advantageous considering the cost of the converter. However, the proposed topology requies more active switches. On the other hand, the lower requested V_{DC} implies that the inductor current will decrease as well as its current ripple. Thus, the losses of the inductor, as well as the conduction and switching losses, could be reduced compared to a classical SSI, even with a higher component count. This section aims to analyze the efficiency of the B-ASSI. Further comparison with other single-stage solutions will also be discussed.

A. Conduction losses

For the conduction losses of the B-ASSI architecture, the analysis differs from that of a classical inverter. Indeed, one of the disadvantages of any Split Source topology is the unequal current distribution among the switches. In practical terms, each switch will conduct a portion of the phase current, as well as the inductor input current, depending on the state. The mean inductor current and the current ripple can be expressed in (6)

$$\overline{i_L} = \frac{\sqrt{3}M_{ac}I_{max}\cos(\phi)}{2(1-M_{DC})} \qquad \Delta i_L = \frac{V_{in}M_{DC}}{L_{SSI}f_{sw}} \tag{6}$$

With I_{max} the peak value of the phase current, ϕ the phase angle between the phase-neutral voltage and the phase current and f_{sw} the switching frequency. The RMS value of the inductor current is used for the joules losses of the inductor with its internal resistance r_L. This RMS current can be calculated by the integration over a switching period of the inductor current. The result is given in (7) with the joules losses :

$$i_L^{RMS\,2} = \overline{i_L}^2 + \frac{\Delta i_L^2}{12} \qquad P_{joules,L} = r_L \cdot i_L^{RMS\,2} \tag{7}$$

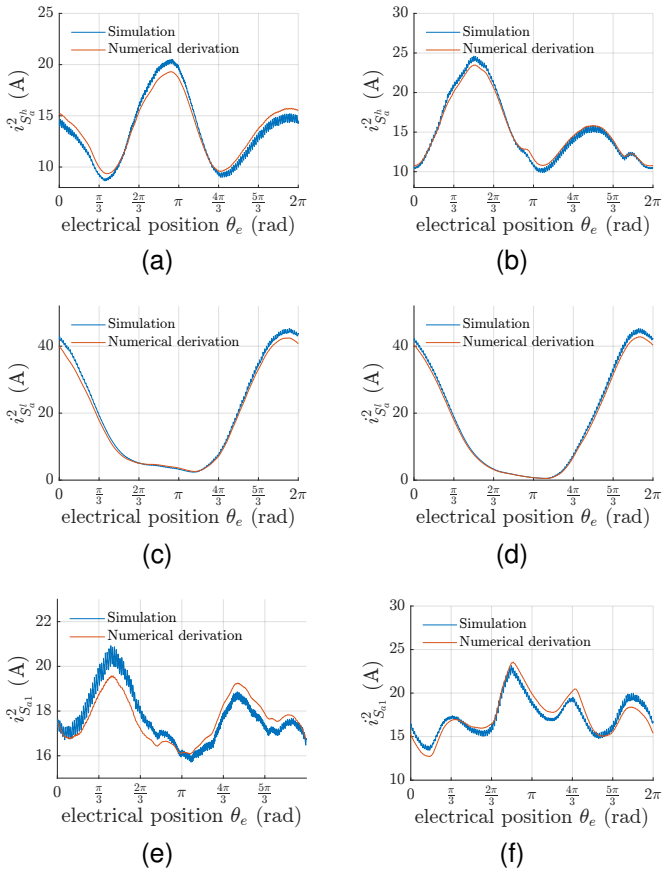

Fig. 5. Comparison of the square of the current obtained in simulation and by numérical differentiation : (a)-upper side MOSFET and diode in non-saturated Mode, (b)-upper side MOSFET and diode in saturated Mode, (c)-Lower side MOSFET and diode in non-saturated Mode, (d)-Lower side MOSFET and diode in saturated Mode, (e)-DC side MOSFET in non-saturated Mode, (f)-DC side MOSFET in saturated Mode

Here, only the analysis for MOSFETs will be derived. Taking into account the bidirectionnality of these transistors, synchronous rectification is considered. Also conduction losses during dead-times are neglegted. Thus, in non-saturated Mode, the high-side switch conducts the phase current for any state except the zero sequence state V_{111}. During the inductor discharging time, the phase current and the inductor current will have opposing directions. The phase current will be divided between the high side switch S_a^h and the clamping switches S_{a1} and S_{a2}. Considering MOSFETs, the resulting current can be expressed as follows:

$$i_{MOSFET,h}^{111} = \frac{2}{3}i_a - \frac{1}{3}i_L \tag{8}$$

TABLE I
MATHEMATICAL EXPRESION OF THE DUTY CYCLE $\alpha_a(\theta)$

	$\alpha_a(\theta)$	
Sector	non-saturated Mode	saturated Mode
I & IV	$M_{ac}\sin(\theta+\frac{\pi}{3})+(1-M_{DC})$	$M_{ac}\sin(\theta+\frac{\pi}{3})+(1-M_{ac})$
II & V	$M_{ac}\sin(\theta+\frac{\pi}{3})+(1-M_{DC})$	$M_{ac}\sin(\theta+\frac{\pi}{3})+(1-M_{ac})$
III & VI	$1-M_{DC}$	$1-M_{ac}$

The RMS value of the current flowing through the switch in non-saturated Mode operation for the positive current during half electrical period is then expressed in (9).

$$(i_{MOSFET,h}^{RMS,SSI})^2 = \frac{1}{2\pi}\Bigg[\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\frac{1}{T_{sw}}\Bigg(i_a^2(\theta)\cdot(\alpha_a(\theta)-T_{sw}(1-M_{DC})) + (\frac{2}{3}i_a(\theta)-\frac{i_L}{3})^2\cdot T_{sw}(1-M_{DC})\Bigg)d\theta\Bigg] \tag{9}$$

with T_{sw} the switching period, $\alpha_a(\theta)$ the duty cycle depending on the sector (Tab. I). In the general case, positive and negative phase current polarities are separated. This is done to take into account the potential antiparallel diode that would conduct for half of the electrical turn. The calculation is differentiated in a separate $i_{Diode,h}^{RMS,SSI}$ not given here. For simplicity reasons, conduction of the diodes during dead-times are not taken into account.

The RMS value of the current flowing through the switch in saturated Mode operation is a little more complex. First of all, the new duty cycle creates a new condition for each PWM sector. This condition is stated when the duty cycle α_{abc} is equal to $\alpha_{abc1}=1-M_{DC}$. In the first sector, there is change at $\theta=arcsin(\frac{M_{ac}-M_{DC}}{M_{ac}})$. When the B-ASSI operates in satured mode, the inductor is discharged through only two or one DC side switches. If two of the three switches S_{abc1} are ON, the current of the high side MOSFET of the inverter leg can be expressed in sector I as follows :

$$i_{MOSFET,h}^{110} = \frac{2}{3}i_a - \frac{1}{6}i_c - \frac{1}{2}i_L \tag{10}$$

For the other case where only one of the three switches S_{abc1} is ON, during the inductor discharging time the current will be equal to :

$$i_{MOSFET,h}^{100} = i_a - i_L \tag{11}$$

Finally, depending on the inductor discharging time duration, if it is greater or not than the duration of C_a^h, the current flowing through the MOSFET is defined in (12).

$$\begin{aligned}(i_{MOSFET,h}^{RMS,ASSI})^2 = \\ \frac{1}{2\pi}\Bigg[&\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\frac{1}{T_{sw}}\Bigg(i_a^2(\theta)\cdot(\alpha_a(\theta)-T_{sw}(1-M_{DC}))\Bigg)d\theta \\ +&\int_{\arcsin(\frac{M_{DC}+m-1}{M_{ac}})}^{\frac{\pi}{3}}\frac{1}{T_{sw}}\Bigg((\frac{2}{3}i_a(\theta)-\frac{1}{6}i_c(\theta)-\frac{i_L}{2})^2\cdot(T_{sw}(1-M_{DC}))\Bigg)d\theta \\ +&\int_{-\frac{\pi}{3}}^{-\arcsin(\frac{M_{DC}+m-1}{M_{ac}})}\frac{1}{T_{sw}}\Bigg((\frac{2}{3}i_a(\theta)-\frac{1}{6}i_b(\theta)-\frac{i_L}{2})^2\cdot(T_{sw}(1-M_{DC}))\Bigg)d\theta \\ +&\int_{-\arcsin(\frac{M_{DC}+m-1}{M_{ac}})}^{\arcsin(\frac{M_{DC}+m-1}{M_{ac}})}\frac{1}{T_{sw}}\Bigg((i_a(\theta)-i_L)^2\cdot(T_{sw}(1-M_{DC}))\Bigg)d\theta\Bigg]\end{aligned} \tag{12}$$

The same definition of the conducting current can be applied to all the switches. As the computation of these integrals is not straightforware and their analysis can be complex, they are computed numerically for the considered operating conditions for each switch with the knowledge of the peak phase current and the desired DC bus voltage. To validate this method of RMS current computation, a simulation of the B-ASSI converter is conducted under the same conditions. The simulation of the B-ASSI converter is carried out with a Permanent Magnet Synchronous Machine (PMSM) in Matlab/Simulink and SimScape, and SimPowerSystems toolboxes. The motor is speed-controlled using classical Field Oriented Control (FOC), and the different parameters used for the simulation are the same as the experiments and are reported in Tab. VI. It is necessary to validate the instantaneous expression of the anlytical calculations. The Fig. 5 shows the comparison of squared currents flowing through the considered switches between the derived expressions and the instantaneous simulated current for a chosen operating point. It demonstrates good agreement among all currents flowing through the switches for the entire electrical period, meaning instantaneous values of the derived current expressions are correctly defined. The current expression as well as the new sectors definiton are correctly described. This indicates that numerical calculation of the defined integral can be utilized to quickly and accurately estimate the RMS currents. The new conditions appearing in each sector due to the modulation can be clearly seen for the saturated Mode.

Finally, an estimation of the conduction losses using all the calculated RMS currents in the switches for MOSFETs is given in (13).

$$\begin{aligned}P_{cond,tot}^{ASSI} = &\ 3\cdot R_{DS(on)}\cdot(i_{MOSFET,h}^{RMS})^2 \\ &+3\cdot R_{DS(on)}\cdot(i_{MOSFET,l}^{RMS})^2 \\ &+6\cdot R_{DS(on)}\cdot(i_{MOSFET,DC}^{RMS})^2\end{aligned} \tag{13}$$

B. Switching losses

The switching losses, in the general case, of the high-side inverter transistor and its antiparallel diode are estimated in the equation (14). Here, since MOSFETs are considered and losses during dead times negleted, the antiparallel diode is not taken into account. The expressions are derived in such a way

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TABLE II
SWITCHED CURRENTS IN NON-SATURATED MODE FOR AN ENTIRE ELECTRICAL TURN

Electrical Position θ	$[0;\frac{\pi}{3}]$	$[\frac{\pi}{3};\frac{\pi}{2}+\phi]$	$[\frac{\pi}{2}+\phi;\frac{2\pi}{3}]$	$[\frac{2\pi}{3};\pi]$	$[-\pi;-\frac{2\pi}{3}]$	$[-\frac{2\pi}{3};-\frac{\pi}{2}+\phi]$	$[-\frac{\pi}{2}+\phi;-\frac{\pi}{3}]$	$[-\frac{\pi}{3};0]$
Sector	I	II	II	III	IV	V	V	VI
Upper Switch	$i_a(\theta)$	$i_a(\theta)$	0	0	0	0	$i_a(\theta)$	$i_a(\theta)$
Upper freewheeling diode	0	0	$i_a(\theta)$	$\frac{2}{3}i_a(\theta)-\frac{i_L}{3}$	$\frac{2}{3}i_a(\theta)-\frac{i_L}{3}$	$i_a(\theta)$	0	0
Lower Switch	0	$\frac{2}{3}i_a(\theta)+\frac{i_L}{2}-\frac{1}{6}i_b(\theta)$	$\frac{2}{3}i_a(\theta)+\frac{i_L}{2}-\frac{1}{6}i_b(\theta)$	$i_a(\theta)-i_L$	$i_a(\theta)-i_L$	$\frac{2}{3}i_a(\theta)+\frac{i_L}{2}-\frac{1}{6}i_c(\theta)$	$\frac{i_L}{2}-\frac{2}{3}i_a(\theta)-\frac{1}{6}i_c(\theta)$	0
Lower freewheeling diode	$\frac{i_L}{3}-\frac{2}{3}i_a(\theta)$	0	0	0	0	0	0	$\frac{i_L}{3}-\frac{2}{3}i_a(\theta)$
DC Side first Switch	0	0	0	0	0	0	0	0
DC Side second Switch	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{3}+\frac{1}{3}i_a(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)\end{bmatrix}$	0	0	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_c(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_c(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{3}+\frac{1}{3}i_a(\theta)\end{bmatrix}$

TABLE III
SWITCHED CURRENTS IN SATURATED MODE FOR AN HALF ELECTRICAL TURN

Electrical Position θ	$[0;\arcsin\frac{M_{ac}-M_{DC}}{M_{ac}}]$	$[\arcsin\frac{M_{ac}-M_{DC}}{M_{ac}};\frac{\pi}{3}]$	$[\frac{\pi}{3};\frac{\pi}{2}+\phi]$	$[\frac{\pi}{2}+\phi;\frac{2\pi}{3}-\arcsin\frac{M_{ac}-M_{DC}}{M_{ac}}]$	$[\frac{2\pi}{3}-\arcsin\frac{M_{ac}-M_{DC}}{M_{ac}};\frac{2\pi}{3}]$	$[\frac{2\pi}{3};\frac{2\pi}{3}-\arcsin-\frac{M_{ac}-M_{DC}}{M_{ac}}]$	$[\frac{2\pi}{3}-\arcsin-\frac{M_{ac}-M_{DC}}{M_{ac}};-\pi]$
Sector	I	I	II	II	II	III	III
Upper Switch	$i_a(\theta)$	$i_a(\theta)$	$i_a(\theta)$	0	0	0	0
Upper freewheeling diode	0	0	0	$i_a(\theta)$	$i_a(\theta)$	$i_a(\theta)$	$i_a(\theta)$
Lower Switch	0	0	$\frac{i_L}{2}-\frac{2}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)$	$\frac{i_L}{2}-\frac{2}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)$	$i_a(\theta)$	$i_a(\theta)$	$i_a(\theta)$
Lower freewheeling diode	$\frac{i_L}{3}-\frac{2}{3}i_a(\theta)$	$\frac{2}{3}i_a(\theta)-\frac{i_L}{3}$	0	0	0	0	0
DC Side first Switch	0	0	0	0	$\frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)$	$\frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)$	i_L
DC Side second Switch	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ i_L\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_c(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)+\frac{1}{3}i_b(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_c(\theta)\end{bmatrix}$	$\begin{bmatrix}\frac{i_L}{3}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_b(\theta)\\ \frac{i_L}{2}+\frac{1}{3}i_a(\theta)+\frac{1}{6}i_c(\theta)\end{bmatrix}$	0	0	0

that the swicthing losses labelled as diode are here considered dissipated in the MOSFET.

$$\begin{cases} P_{sw}^{MOSFET} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+phi}^{\frac{\pi}{2}+phi}\frac{1}{T_{sw}}\frac{V_{DC}i_{sw}(\theta)}{V_{ref}I_{ref}}(E_{on}+E_{off})d\theta \\ P_{sw}^{diode} = \frac{1}{2\pi}\int_{\frac{\pi}{2}+phi}^{-\frac{\pi}{2}+phi}\frac{1}{T_{sw}}\frac{V_{DC}i_{sw}(\theta)}{V_{ref}I_{ref}}(E_{rec})d\theta \end{cases} \tag{14}$$

Where E_{on}, E_{off} and E_{rec} are the energies dissipated during turn-on, turn-off and reverse recovery of the diode respectively. The switched voltage is always V_{DC} for all the switches, but the switched current i_{sw} is the one listed in Tab. II and Tab. III, for SSI and saturated Modes respectively. All switches of the inverter side as well as the switches S_{abc1} will exhibit only one turn-on and turn-off for each PWM period. Only the switches S_{abc2} will turn-on and turn-off twice each per PWM period. This is also the case for the SSI. Each switched current can be different for the two transisitions. Therefore the tables represent the two switched currents for S_{abc2}. Each current must be taken into account once for each reverse recovery event that occurs during the switching period.

C. Voltage and current stresses comparison

This section aims to provide insight into the comparison betwween the proposed B-ASSI and the classical three-phase SSI. As stated earlier, the proposed B-ASSI adresses the issue of low DC-bus voltage utilization, meaning that to achieve the same phase voltage, lower V_{DC} is required. The induced voltage stresses for the two topologies are summarized in Tab. IV. Where both the boosting ratio and the attainable phase voltage are derived for several topologies. Considering a classical two-level inverter (noted 2L-VSI), the DC bus voltage is fixed unless a two stage solution is implemented. The maximal phase voltage is bound by $V_{DC}/\sqrt{3}$ for SVPWM. The Fig. 6 shows the elevation ratio V_{DC}/V_{in} versus the phase voltage V_ϕ normalized by the input voltage V_ϕ/V_{in}. This plot actually translates the minimal elevation V_{DC} that would be required to attain the same phase voltage. On this plot, the highlighted area clearly shows that for all operating points, the B-ASSI generates less voltage stress than the SSI independently of the modulation used. The B-ASSI presents the lowest voltage stress among the single-stage topologies. The Z-source is slightly better for low-phase voltages, as the DC bus voltage can be chosen to not be elevated at all. However, due to the proposed modulation, the B-ASSI requires a minimal elevation-ratio as stated in (5). The current stresses are the same as the SSI when operating in non-saturated mode. However, since the B-ASSI can operated at lower DC bus voltage than the SSI in saturated mode, this mode will be favored. In facts, in this mode the current stresses are also reduced and expressed in Tab. V. In this table, the current stresses are compared to the ones derived for the Boost+VSI topology. There lower compared to the SSI but would be slightly higher compared to the Boost+VSI due to the currents flowing though the low-side MOSFETs during charging states.

TABLE IV
INPUT/OUTPUT RELATIONSHIP OF CLASSICAL TWO-LEVEL INVERTER AND DIFFERENT CONSIDERED SINGLE STAGE TOPOLOGIES

Architectures	V_{DC}/V_{in}	V_ϕ/V_{in}
2L - VSI	1	$\frac{M_{ac}}{\sqrt{3}}$
ZSI - constant Boost [16]	$\frac{1}{\sqrt{3}M_{ac}-1}$	$\frac{M_{ac}}{2(\sqrt{3}M_{ac}-1)}$
SSI - SPWM [3]	$\frac{4\pi}{2\pi-3\sqrt{3}M_{ac}}$	$\frac{2\pi M_{ac}}{2\pi-3\sqrt{3}M_{ac}}$
SSI - MSVPWM [3]	$\frac{1}{1-M_{ac}}$	$\frac{M_{ac}}{\sqrt{3}(1-M_{ac})}$
Proposed B-ASSI	$\frac{1}{1-M_{DC}}$	$\frac{M_{ac}}{\sqrt{3}(1-M_{DC})}$

TABLE V
COMPARISON OF CURRENT STRESSES

	B-ASSI	Boost+VSI
Upper transistor	I_{max}	I_{max}
Upper freewheeling diode	I_{max}	I_{max}
Lower switch	$i_L+\Delta i_L+I_{max}$	I_{max}
Lower freewheeling diode	$\frac{2}{3}I_{max}-(i_L+\Delta i_L)$	I_{max}
DC side transistors	$i_L+\Delta i_L$	$i_L+\Delta i_L$

D. Efficiency comparison

The B-ASSI is the only topology that can closely operate as well as a two-stage solution without the need to over-elevate

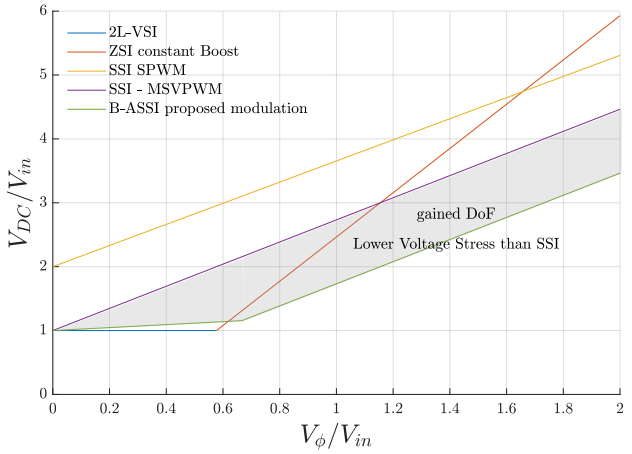


Fig. 6. Voltage stresses : boost ratio V_{DC}/V_{in} versus normalized peak voltage V_ϕ/V_{in}

the DC-bus voltage, thus minimizing the losses as well. The efficiency of the B-ASSI considered in this paper is derived in (15), primarily considering the conduction and switching losses in the switches, and the joules losses of the inductor and DC link capacitors.

$$\eta = \frac{P_{out}}{P_{out}+P_{cond,tot}+P_{sw,tot}+P_{joules,L,C_{DC}}} \quad (15)$$

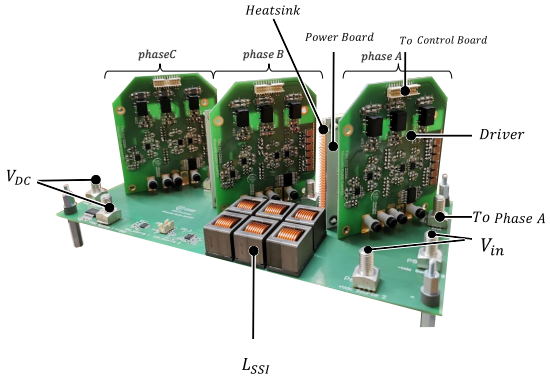
To iron losses are calculated with steinmetz equation. However, the Steinmetz parameter are not well known with the used inductor. This is why the iron losses are used to calibrate the losses to the one measured experimentally. The efficiency of the SSI can be easily derived from the equation with a few modifications. First, for the conduction losses, the term considering the three switches S_{abc1} can be omitted, as there are only three diodes. This is also true for the switching where the first DC side MOSFET that is not taken into consideration. Finally, the last difference lies in the boosting factor M_{DC} taken into account, which would be higher for SSI, thereby increasing all losses since the inductor current i_L as well as its high-frequency ripple are increased.

V. Experimental Results

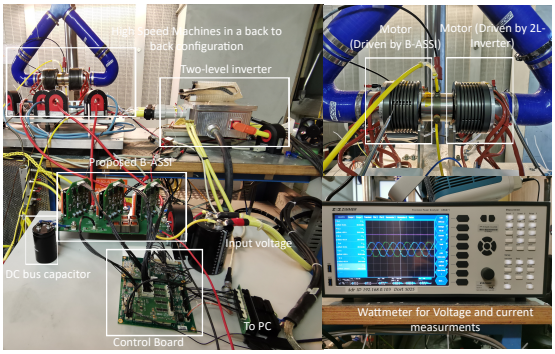
TABLE VI
Experimental Motor and Converter Parameter.

Parameter	Symbol	Value
Input Voltage	V_{in}	20V
Split source Inductor	L_{SSI}	6μH
DC bus Capacitor	C	460μF
Motor Nominal Voltage	V	48V
Switching frequency	f_{sw}	30kHz
Number of pole pairs	p	1
Motor Inductance	L_s	5μH
Motor Resistance	R_s	3mΩ
Flux linkage	ϕ_f	0.9mWb
Speed reference	Ω^*	[0-60 000 rpm]

A prototype of the B-ASSI has been developed, using MOSFETs NTMTS6D0N15MC from ON-semiconductors. Fig. 7 illustrates the prototype as well as the experimental setup on the test bench. The converter is designed as a proof of concept, and is therefore oversized. Only the inductor is undersized to reduce its volume while maintaining having high inductor current. Since the B-ASSI always operates in continuous conduction mode, high ripple current does not affect its correct operation. The proposed modulation of the B-ASSI is implemented in MATLAB/Simulink environment. Automatic code generation is used for rapid prototyping purposes. The code is then uploaded to a custom ARM target called the control board via Code Composer Studio software. The converter is used to drive a PMSM in a back-to-back configuration. An 2L-VSI is used to drive the second machine. Thus being able to control the torque and speed of the common shaft. The parameters of the B-ASSI prototype and the driven PMSM are given in Tab. VI.



(a)



(b)

Fig. 7. Experimental validation : (a) – Proposed B-ASSI prototype, (b) – experimental setup

The converter is firstly tested in open-loop configuration to validate its correct operation. Fig. 8 presents the experimental validation of the converter operating in saturated Mode. Indeed, the graph depicts the gate-to-source voltages generated by the drivers from the command signals C^h_{abc} along with the inductor current. It can be clearly seen that the inductor discharging state begins in one of the active states of the inverter. Whereas for a classical SSI, this inductor discharging time could only occur during the zero-sequence state V_{111}. These graphs validate that the converter operates as intended.

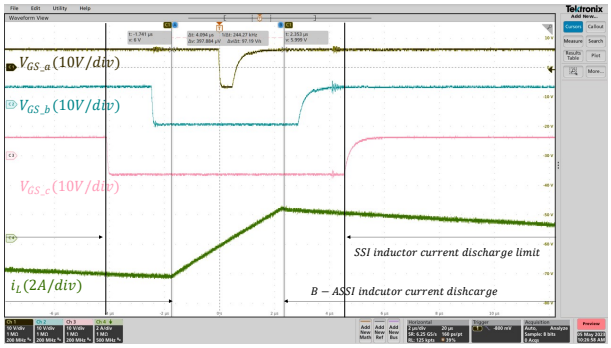


Fig. 8. Experimental validation of the inductor current discharge during an active state

The Fig. 9 presents the converter driving the PMSM. A speed of $20000rpm$ and a torque generating a peak phase current of $5A$ are imposed. An input voltage of $V_{in} = 20V$ is applied. Without changing the load operating condition, a smooth transition in open-loop is performed from the B-ASSI to an SSI operation mode. This transition is accomplished by changing the DoF M_{DC}. It changes from an arbitrary value of $V_{DC} = 24.2V$ in saturated Mode with $M_{DC} = 0.21$ to another value of $V_{DC} = 27.1V$in non-saturated Mode with $M_{DC} = 0.35$. This figure validates the conditions implemented to change from saturated Mode to non-saturated Mode. Furthermore, a reduction of almost $10A_{pk-pk}$ in current ripple can be observed. It highlights one of the advantage of the B-ASSI over the simple SSI: the current ripple can be significantly reduced by minimizing the boosting factor. Not only does the B-ASSI improve the DC bus voltage ratio, but it also reduces the mean inductor current as well as its ripple.

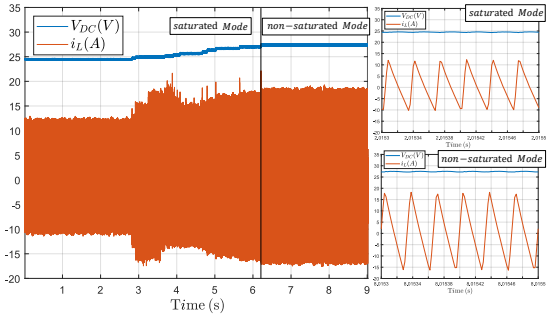


Fig. 9. Difference in the experimental inductor current ripple level between the proposed B-ASSI saturated mode and the SSI equivalent non-saturated Mode

The Fig. 10 depicts the B-ASSI operating in motor-only or generator-only mode. The speed is set at $50000rpm$ with a resistive torque, generating a peak phase current of $30A$ in motor mode, and $15A$ in generator mode.

Finally, the efficiency of the proposed converter is experimentally assessed using a wattmeter. The experimental efficiency is compared to the one calculated theoretically on the same conditions. The analysis is done for two different load torque currents of 20 and $30A$, where the efficiency versus the output power is plotted in Fig. 11a and, Fig. 11b respectively. The speed of the motor is gradually increased from 20 to $60krpm$.

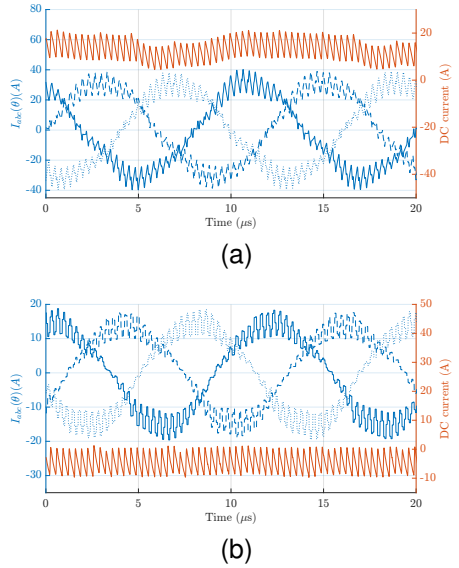


Fig. 10. Experimental validation : (a)-motor mode, (b)-generator mode

The converter is tested in the two different operation modes, SSI and B-ASSI. Two different values of M_{DC} are chosen to represent both operation modes. For the ASSI operation mode, an $M_{DC} = 0.05$ is set in open-loop for the entirety of the points. This value does not represent the minimal value that could be achieved at all points, but is close to the saturation value for the higher output power points tested. As mentioned, the minimal V_{DC} achievable is dependent on the modulation index M_{ac}. If the operating point requests more power, the minimal value V_{DC} will increase. For this test, to show that V_{DC} becomes a total DoF, a constant high enough V_{DC} is chosen. Since its value is still very low, it represents, in reality, an over-elevation of $V_{DC} = 21.05V$ at most. On the contrary, for the SSI, V_{DC} cannot achieve the same point with a value as low as the B-ASSI. It is also much more dependent on M_{ac}. For a fair comparison, the value chosen for V_{DC} for all points is always the lowest that the SSI can achieve. This represents a variation of $V_{DC}\epsilon[23.6V, 30.4V]$ from the lowest to the highest requested power point.

It can be seen that due to its capability to achieve a lower DC bus voltage, the saturated Mode exibites higher efficiency at all operating points compared to the non-saturated Mode. The efficiency depicted from the B-ASSI operating in non-saturated Mode, would exhibit higher conduction losses than a classical SSI, since the three switches S_{abc1} are not needed. However, the joules losses and conduction losses for all other switches remain the same. It was verified in simulation that the efficiency of the SSI would be very close to the efficiency of the B-ASSI operating in non-saturated Mode, with a difference not higher than 1% in efficiency. The difference in efficiency between the two modes is attribuated to the addition of the component, compromising the conduction losses while enhancing the ability to truly decouple the load operating condition from the control of V_{DC}. Thus, the converter would be able to operate in optimal conditions and reduce losses.

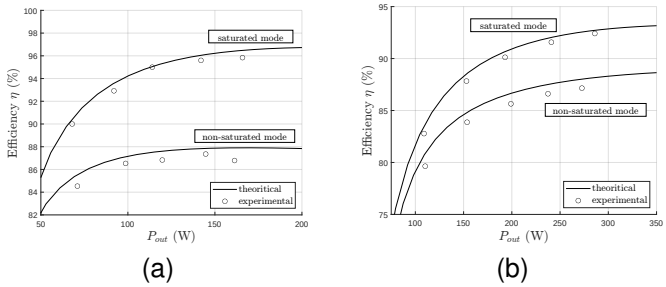


Fig. 11. Experimental and theoretical efficiency versus load power : (a)-for $I_{max} = 20A$, (b)-for $I_{max} = 30A$

VI. Case study : Application of the proposed loss analysis

TABLE VII
Simulated Motor for theoretical comparison.

Parameter	Symbol	Value
Input Voltage	V_{in}	175 V
Motor Nominal Voltage	V	350V
Switching frequency	f_{sw}	30kHz
Number of pole pairs	p	4
Motor Inductance	L_s	250μH
Motor Resistance	R_s	6.9mΩ
Flux linkage	ϕ_f	87.78mWb
Motor inertia	J	$2.8.10^{-6} kg.m^2$
Friction coefficient	f	$5.2.10^{-6} N.m.s/rad$
Maximal Speed	Ω^*	20 000 rpm

Finally, the validated losses analysis is used for an analytical study of the benefits of the B-ASSI for traction applications. An application-specific traction PMSM is emulated, with parameters presented in Tab. VII. The two converter are compared considering same weight and size. Since the B-ASSI uses four more transistors, the cost would be higher. The efficiency of the proposed converter, as well as for the two-stage Boost+VSI topology, are calculated for the entire torque-speed characteristic. Three operating region are considered independently due to the boosting function and are represented in Fig. 12a. Firstly, a classical Maximum Torque Per Ampere (MTPA) strategy is considered where the input voltage is two times lower than the nominal DC link voltage of the motor. In the second region, V_{DC} is progressively increased. When V_{DC} reaches its defined maximal value, flux-weakening is used. For this case, the maximal V_{DC} is set as $2V_{in}$. The gain in efficiency of the B-ASSI over the two-stage Boost+VSI is presented in Fig. 12b. This difference denoted as $\eta_{B-ASSI} - \eta_{Boost}$, where a positive value indicates a higher efficiency of the B-ASSI over the two-stage solution. It can be seen that the difference is lower than 1% in across a wide range of operating points. However, the B-ASSI shows its merits for the lightly-loaded points. This can be explained by the unequal distribution of currents in the B-ASSI. Specially, for low speeds, the high-side MOSFETs conduct the difference between the phase current and the input inductor current, which is not the case for the two-stage solution.

To further elaborate on this gain in efficiency at low-power operating points, a comparison on a Worldwide harmonized Light

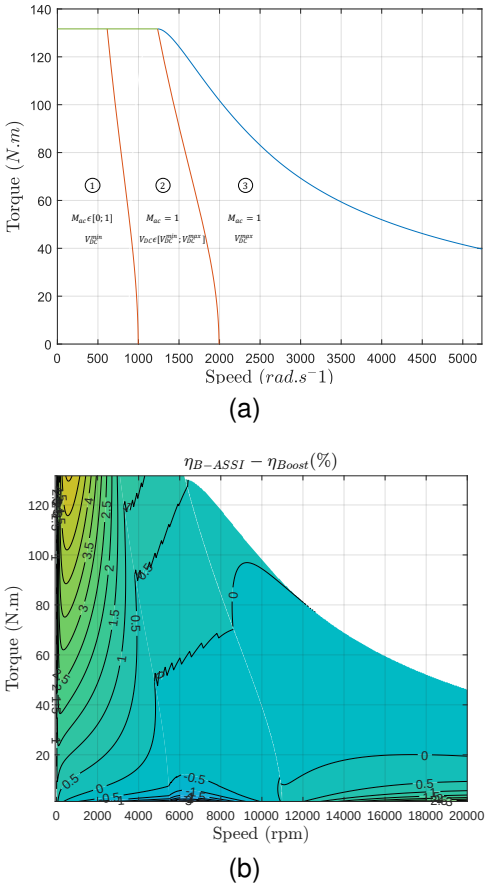
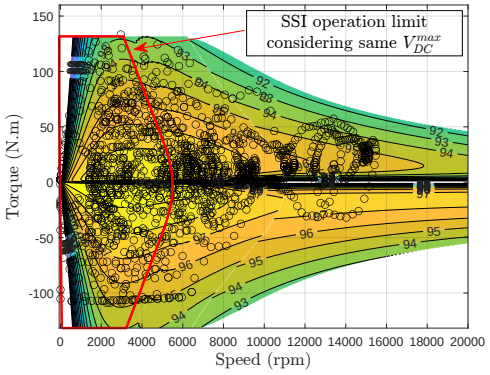
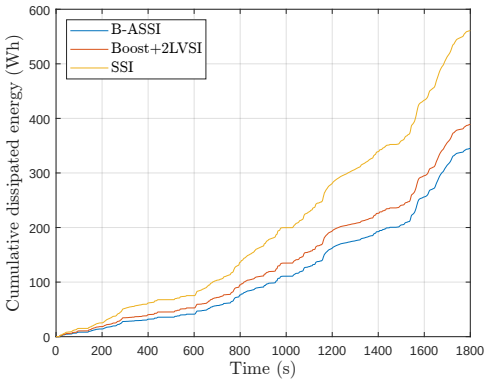


Fig. 12. Efficiency analysis : (a) - definition of working zones in the torque-speed characteristic, (b) - efficiency difference between B-ASSI and two stage Boost+VSI

vehicles Test Procedure (WLTC) drive cycle is elaborated. This is done considering well established longitudinal dynamics of the vehicle [17] and physical parameters of the vehicle. The considered cycle for the analysis is superimposed on the efficiency and presented in the torque-speed characteristic on Fig. 13a. For reference, the limitation of a classical SSI in the torque-speed characteristic can be derived. If the same component are chosen, and thus the maximum DC bus voltage is set to the same value, only the red highlighted area could be obtained with a classical SSI. The Fig. 13b compares the cumulated energy dissipated due to the losses for the considered converters. As elaborated earlier, it presents a similar level of losses dissipated throughout the entire cycle, with the exception of better efficiency for the low loaded points, mostly at the beginning of the drive cycle. For the study of the losses for the SSI, the constraint over the maximum DC bus voltage needs to be relaxed. Thus, a boosting ratio over two time up to six times the input voltage needs to be considered to achieve every point of the cycle as considered here. The SSI undergoes a high over-boosting of the DC bus voltage due to the lack of Degree of Freedom and consequently suffers higher losses. The last graph thus shows that the modification of the SSI based on the principle of the B-ASSI is absolutely necessary to be compatible for traction applications. Finally, it seems that the proposed converter, even if it requires more active



(a)



(b)

Fig. 13. Efficiency analysis : (a) - efficiency of the B-ASSI under considered driving cycle, (b) - cumulated losses comparison under the normalized cycle for several topologies.

switches, presents an equivalent or even better efficiency than the classical two stage solution depending on the considered drive cycle profile.

VII. Conclusion

This paper proposes a depth losses analysis of the previous proposed bidirectional active split source inverter (B-ASSI). The correct operation of the B-ASSI, coupled with its modulation, has been experimentally validated, along with its bidirectional power flow capability and superior efficiency compared to the SSI. The losses analysis for three phase SSI topology and B-ASSI are thus derived in this paper, enabling fast computation and theoretical comparison as well as giving insight for design considerations. Overall, the B-ASSI proves itself to be an interesting single-satge topology, that does not suffer from over-elevation of the DC bus voltage like other single-stage topologies like the SSI or the ZSI. However, the architetcure need to be more thoroughly compared to classical two-stage solutions. The paper tries in a exemple case study to show the potential merit of the B-ASSI over the Boost+VSI in terms of efficiency. Thanks to the new DoF of the B-ASSI, the two convertes presents almostidentical DC bus voltage utilization. However, the Boost+VSI requires fewer semiconductors, lower total active die area and would be more cost effective.

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