

Comparaison des Modèles de Calibrage pour l'Extraction Précise des Performances RF d'un Transistor HBT SiGe en haute fréquence

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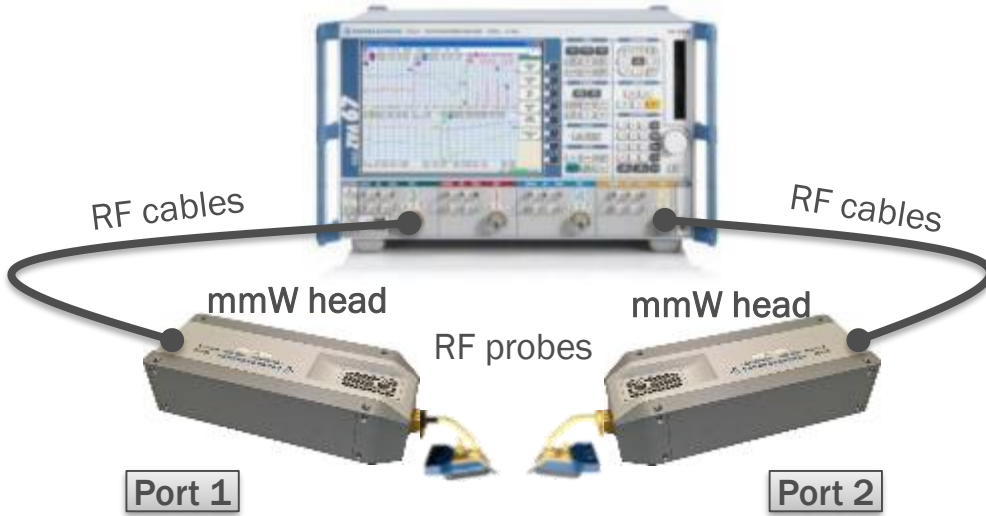
OUTLINE

- Introduction
- 16 errors terms methodology and definition of its standards
- Error terms analysis
- **Results:** SiGe HBT measurement
 - SOLT vs on-wafer TRL and on-wafer 16-T up to 220 GHz
 - Influence of error model up to 330 GHz
- Conclusion

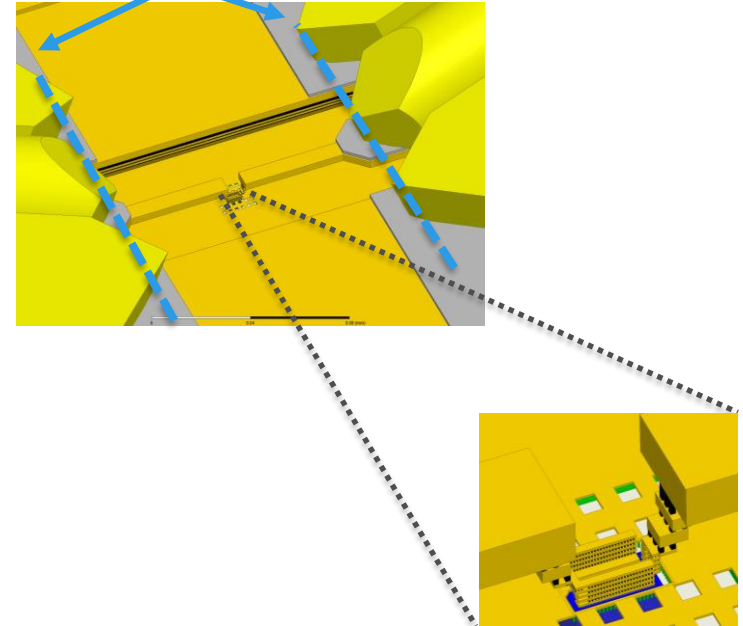
INTRODUCTION

Off-wafer calibration procedure

Vector Network Analyzer (VNA)



Reference plane after calibration



1

Off-wafer calibration on ISS



Impedance Standard Substrate

- "Complete" OPEN (at M1)
- "Complete" SHORT (at M1)

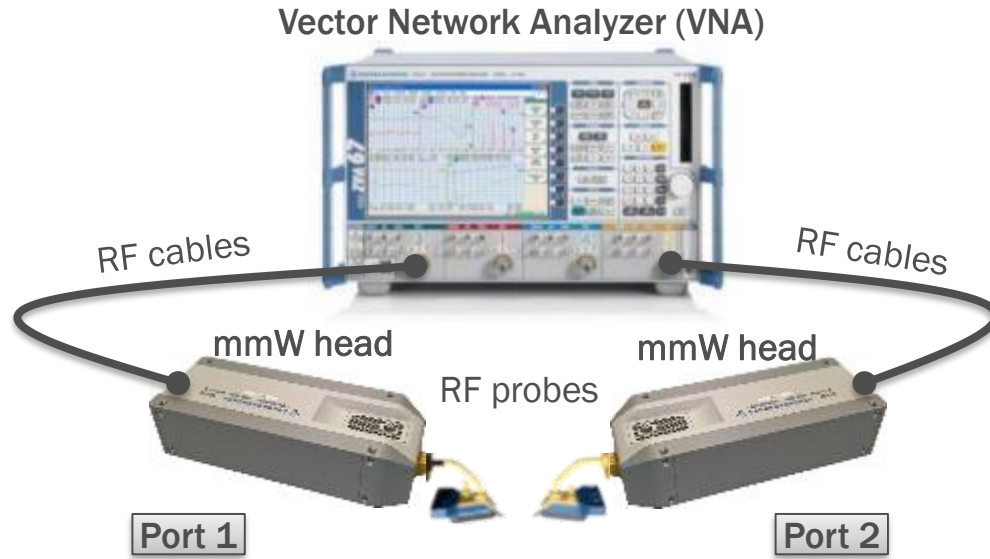
2

On-wafer de-embedding

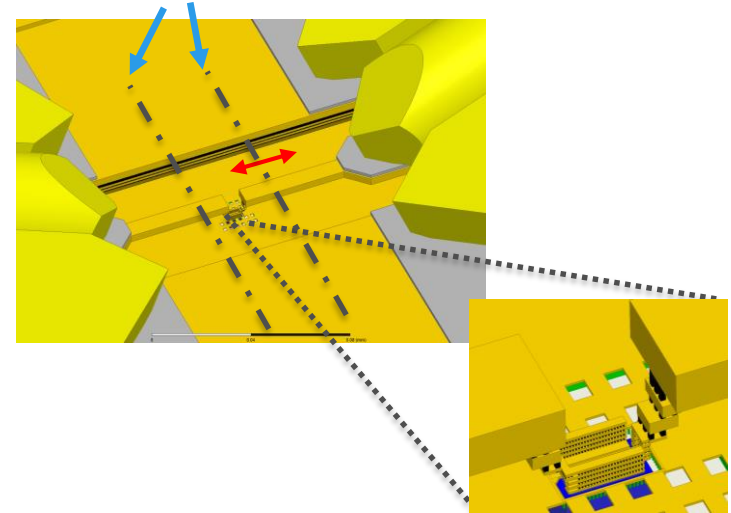
Open-Short de-embedding or PSO / PTSO ...

INTRODUCTION

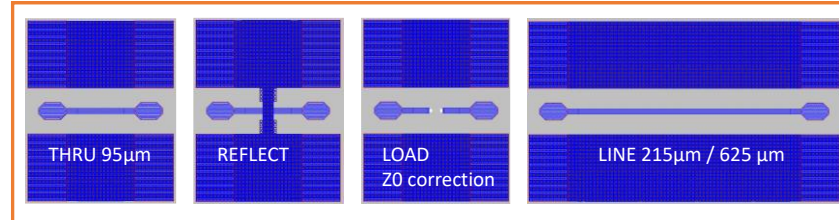
On-wafer calibration procedure



Reference plane after calibration



1 → On-wafer TRL calibration



2 → On-wafer de-embedding

- “Complete” SHORT (at M1)
- “Complete” OPEN (at M1)

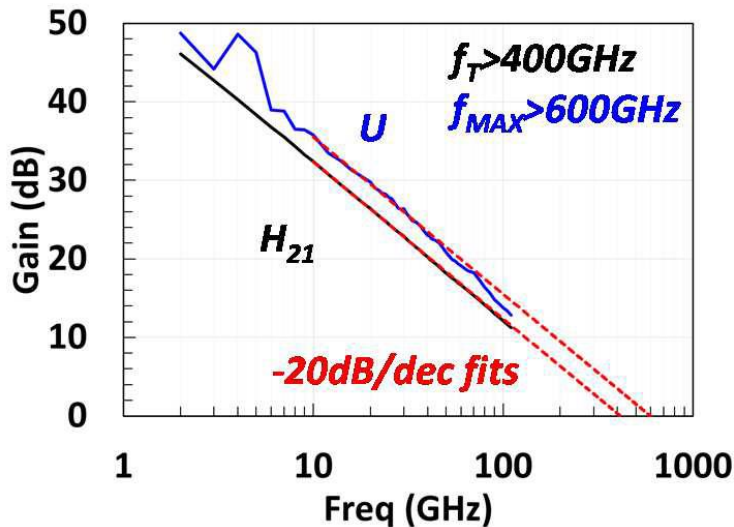
Choose ref. plane & apply S0 or OS de-embedding

Impact of test structure and probes on calibration ?

Impact of calibration/probes on f_{max} measurement

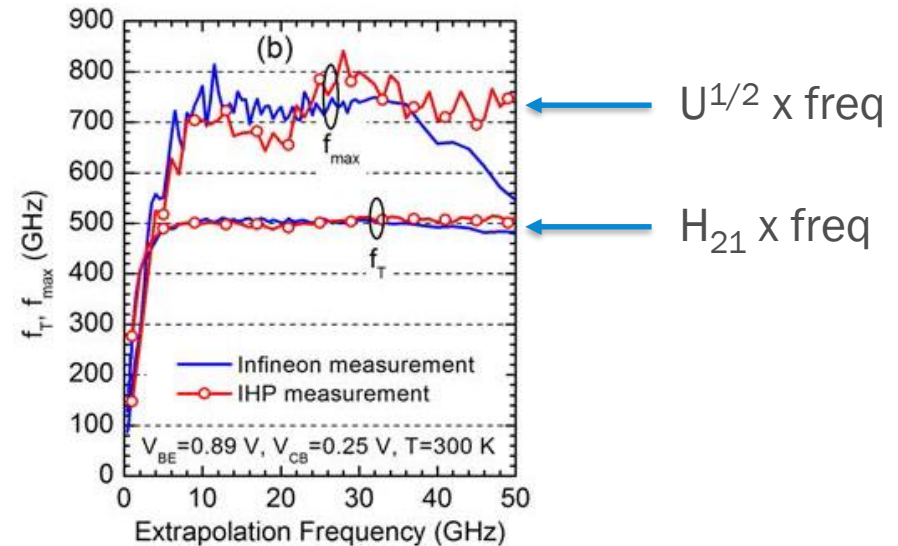


Example N° 1: Global Foundries



Mason's and H_{21} vs frequency for a Si Ge HBT from Global Foundries [5]

Example N° 2: IHP & Infineon



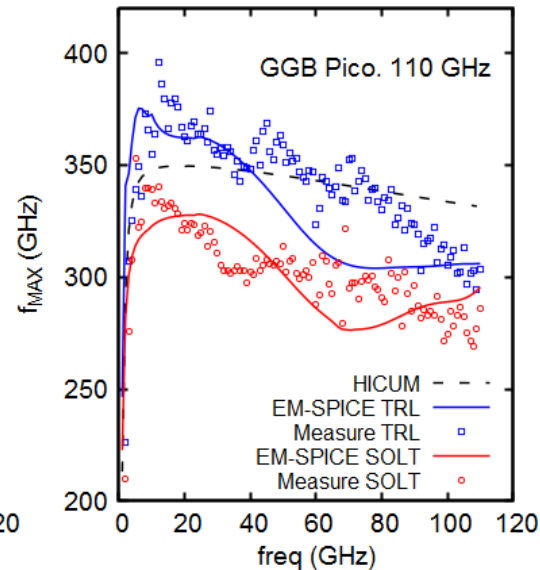
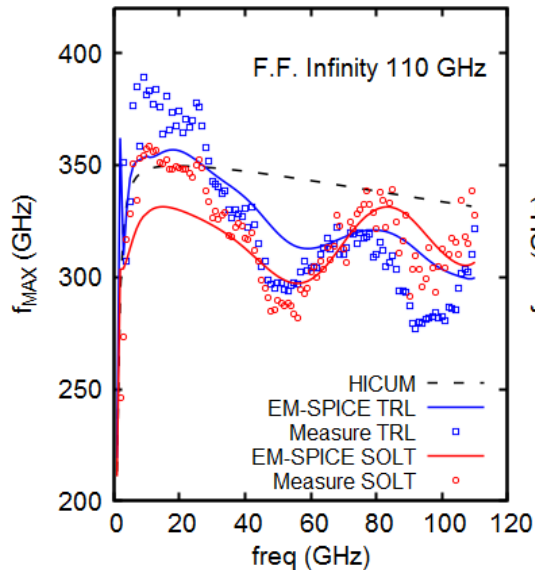
Mason's and H_{21} gain-bandwidth product vs frequency for the same SiGe HBT measured at IHP and Infineon [6]

- ⇒ Measuring FOMs of miniaturized transistors becomes a challenge when their $f_{MAX} \gg 100 \text{ GHz}$
- ⇒ Parasitic from EM probe coupling ~ intrinsic element of the transistor

Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement

- Measuring the same device with two different probes
- Measuring the same device with off-wafer or on-wafer calibration



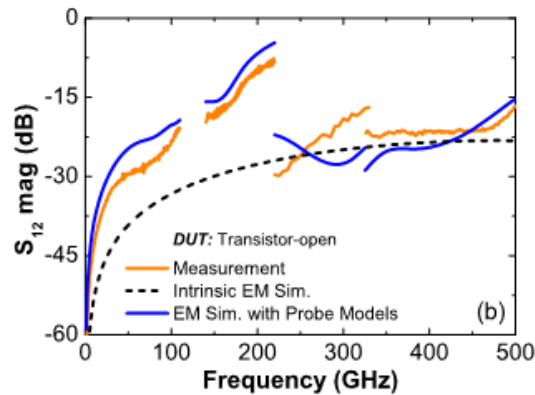
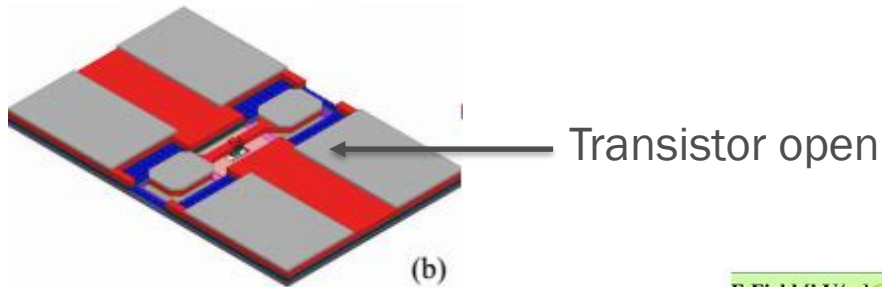
➔ Influence of probes is not removed by calibration

Impact of test structure and probes on calibration ?

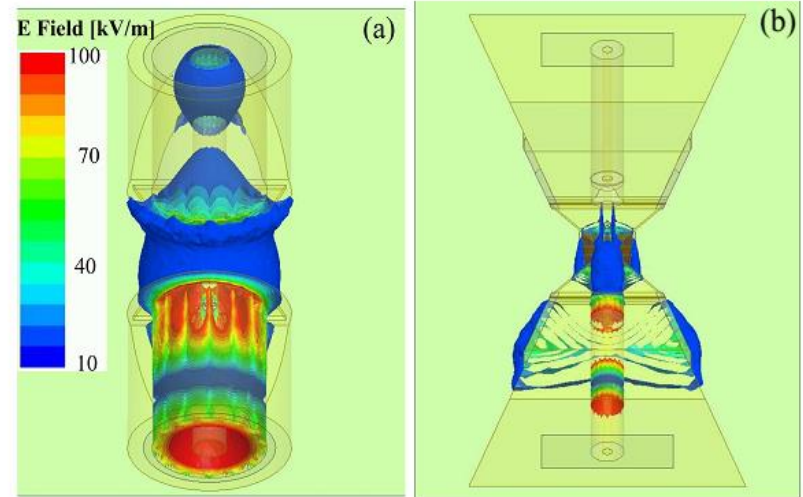
Measurement discontinuities: uncorrected probe couplings ?



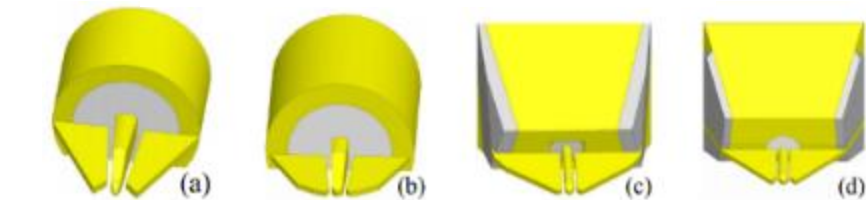
Worst case example : 90 μ m inter-probe distance



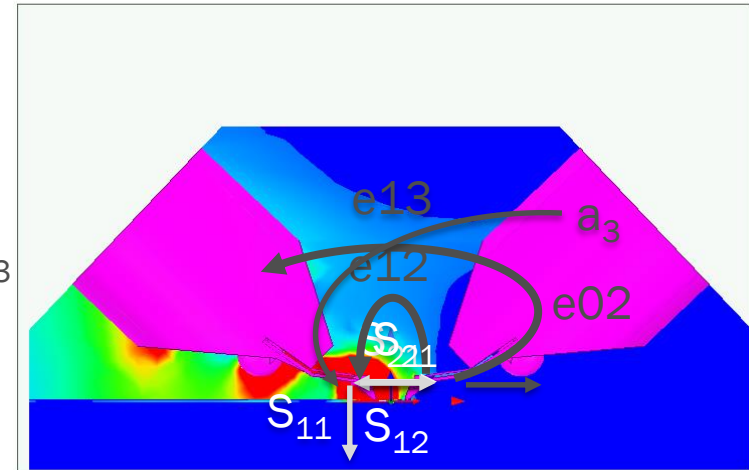
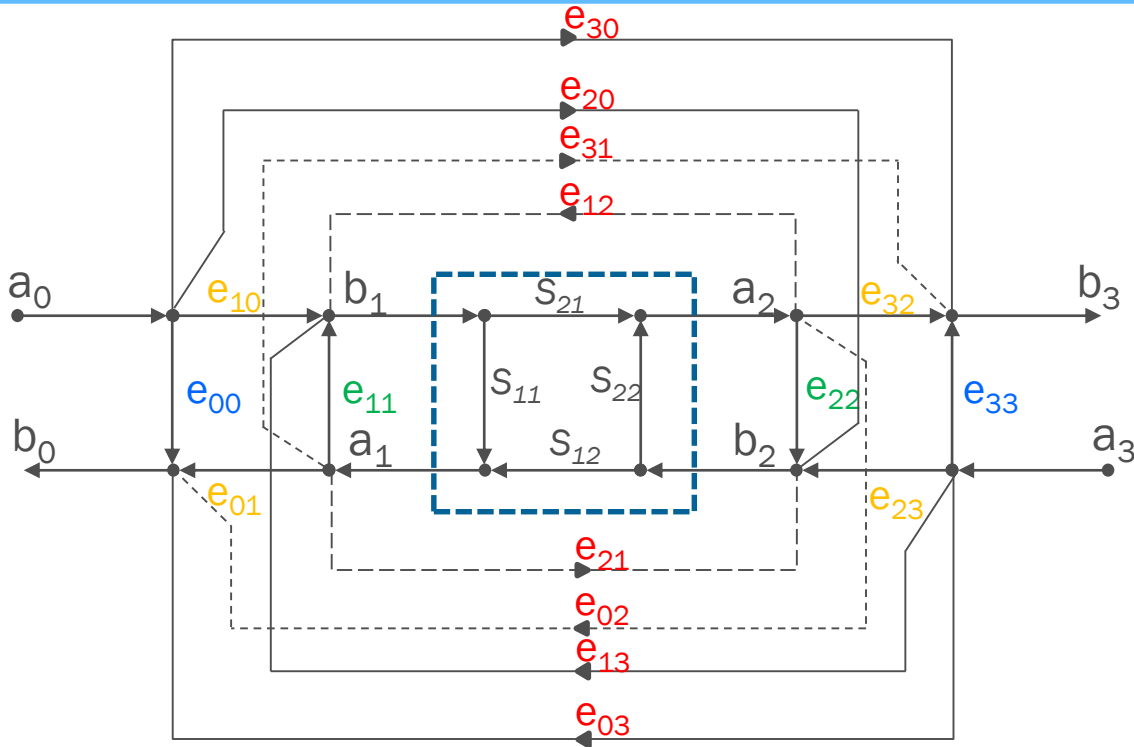
@ 220 GHz



Probes couplings need to be calibrated



16 error terms model



e_{30} and e_{03} models leakage within the VNA

Port Match: e_{11}, e_{22}

Directivity: e_{00}, e_{33}

Frequency Response: $e_{01}, e_{10}, e_{32}, e_{23}$

Leakage: $e_{30}, e_{03}, e_{31}, e_{13}, e_{21}, e_{12}, e_{20}, e_{02}$



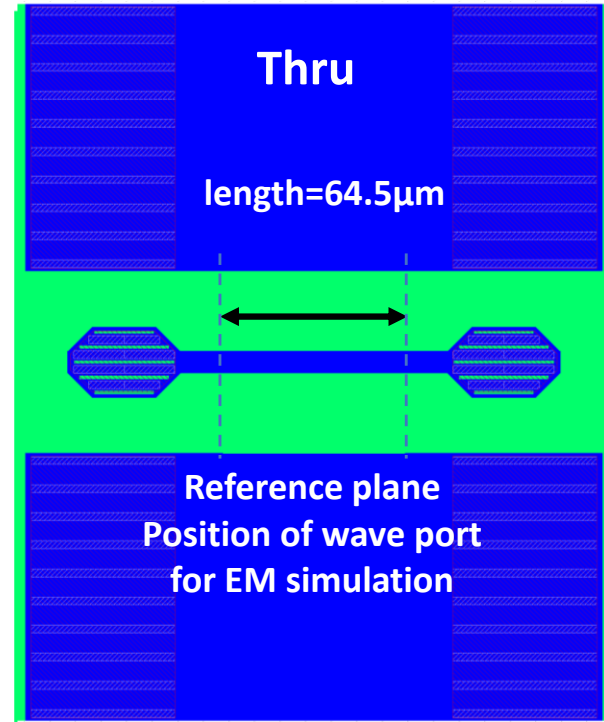
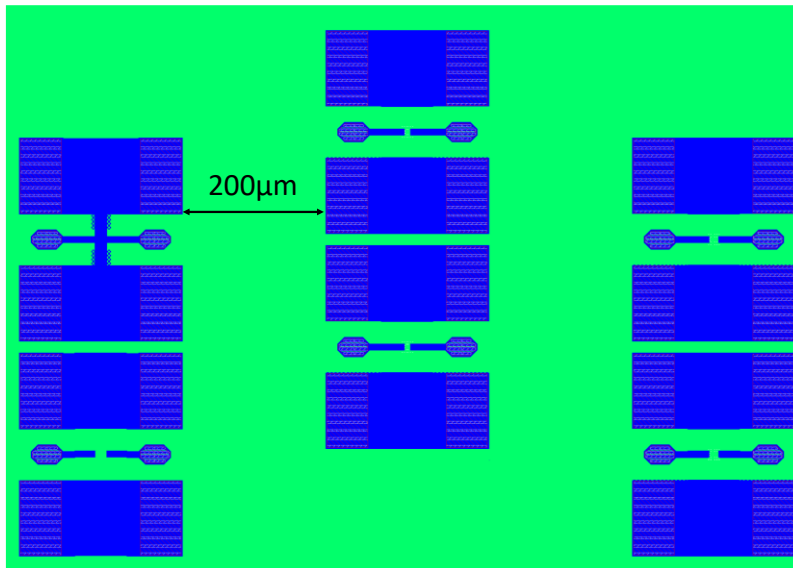
- Error terms find using SVD
- Implementation in ICCAP using Python and PEL

[1] J. V. Butler et al., *IEEE Trans. MTT* 1991, doi: 10.1109/22.106567

Design of test structures for on wafer calibration

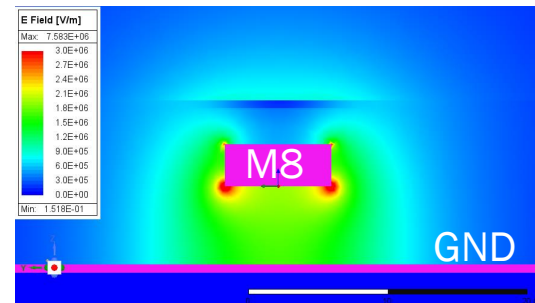
BiCMOS 55nm layout

Floorplan

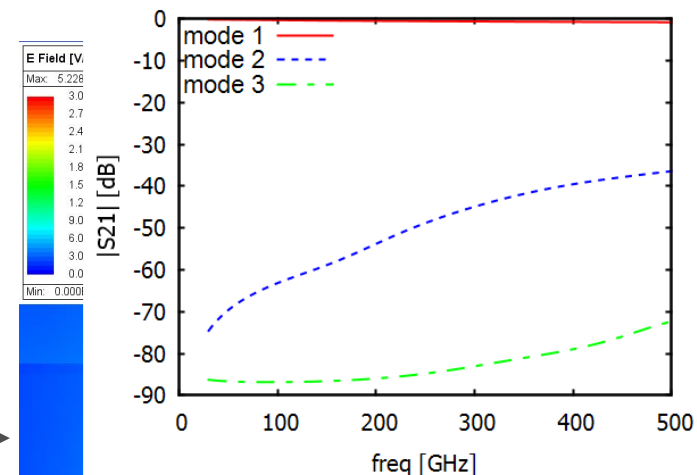
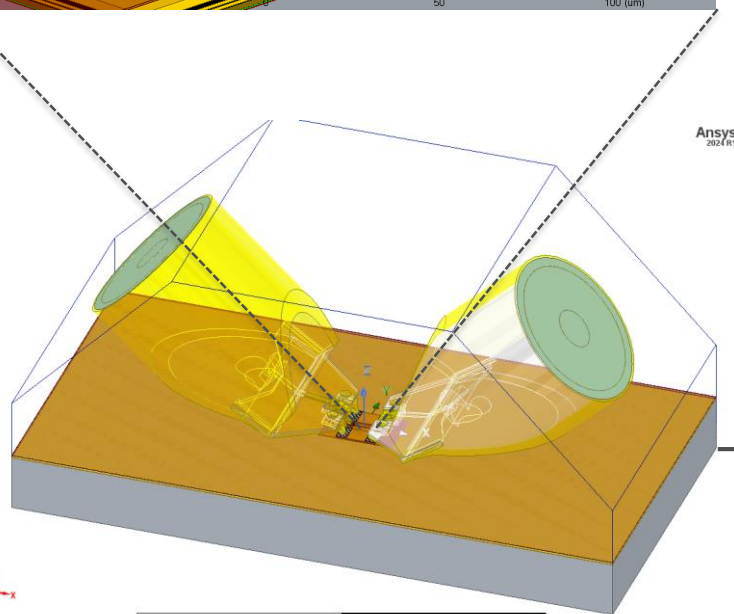
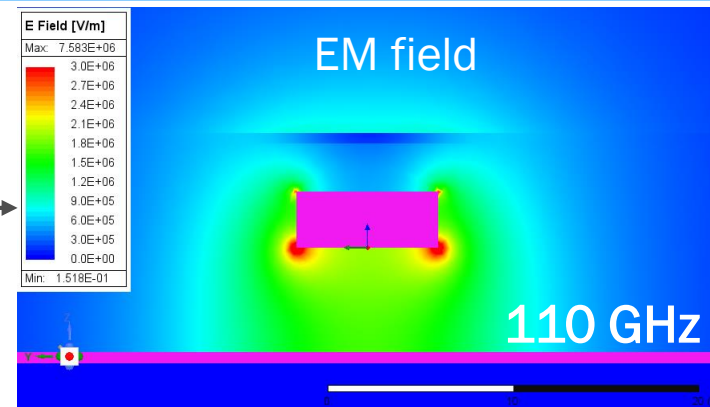
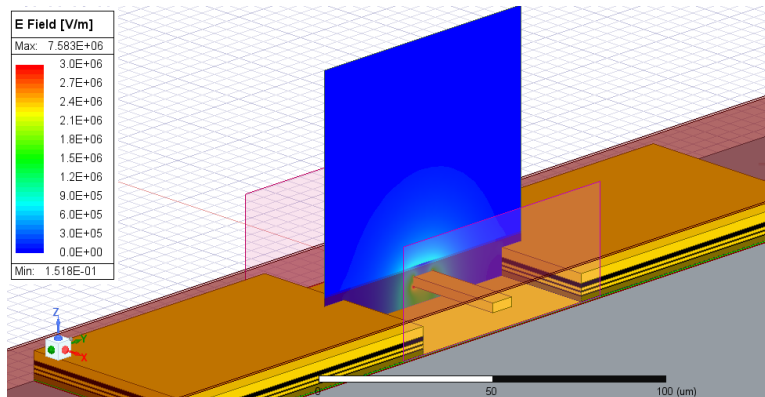


Microstrip line cross-section

- 5 test structures used for 16T calibration:
 - Thru, Short M8, Open M8, Load, Load-Short
- 3 lines available for TRL calibration



Verification of propagation mode establishment for TRL

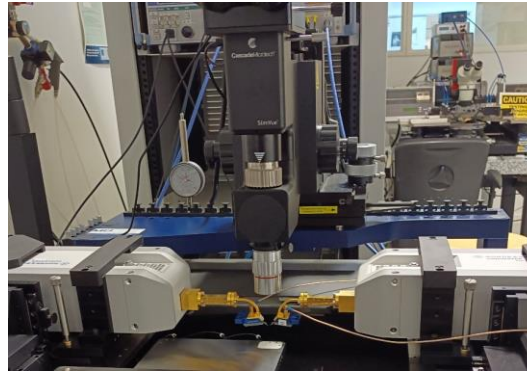


Simulation of the first 3 modes of the microstrip line, Length = 583µm

Definition of standards

Build intrinsic test structure in EM simulator using layout and BEOL definition

Feed EM simulator parameter using DRM

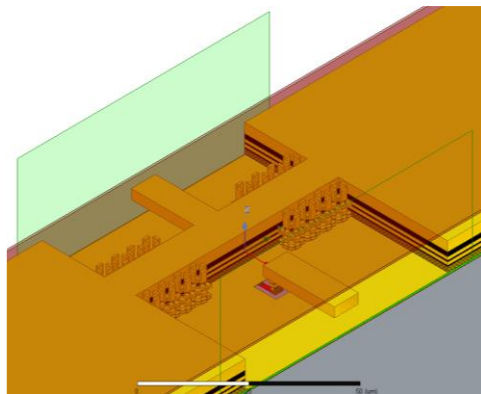


Adjust physical parameters in EM simulator and update EM & 16T cal. if need

1

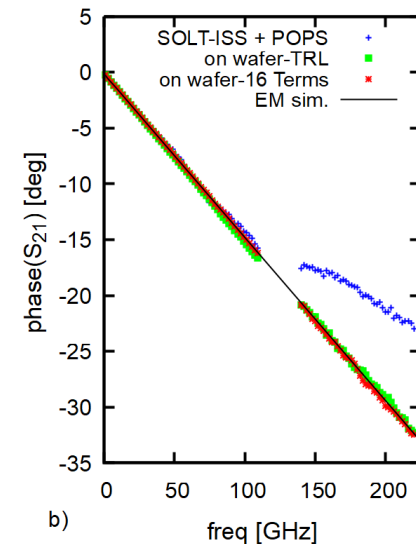
2

3



Perform raw measurements

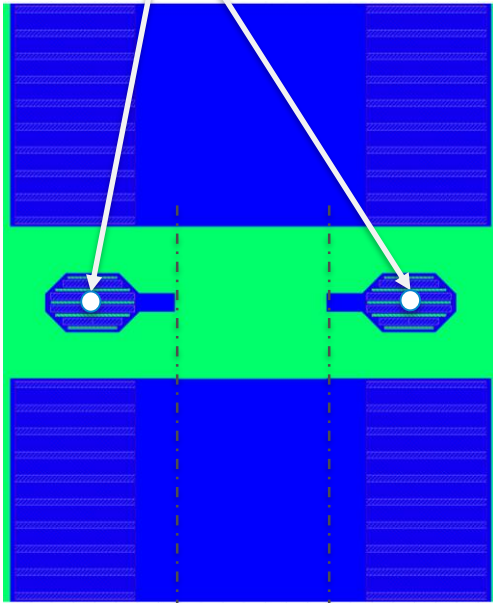
Apply TRL and 16T simultaneously and verify consistency (lines & error terms)



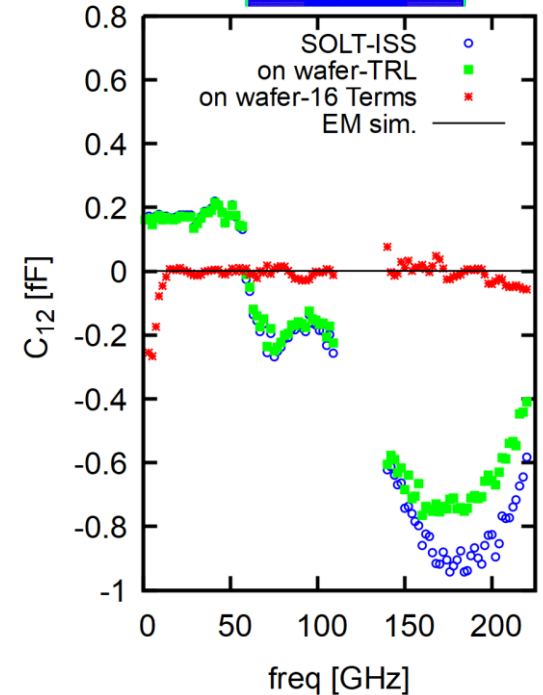
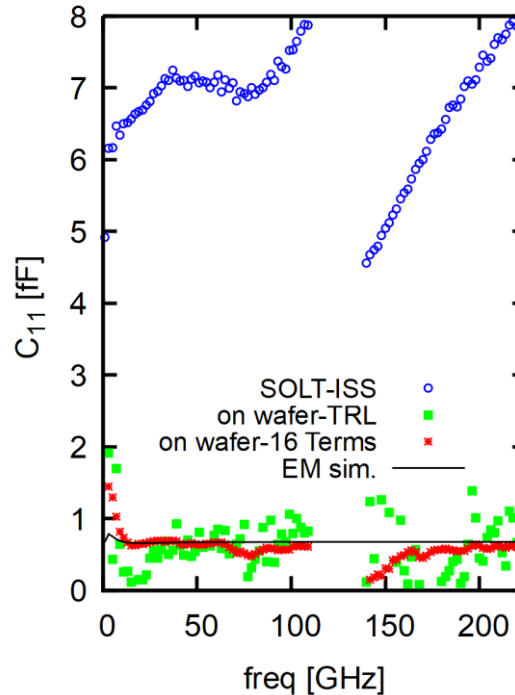
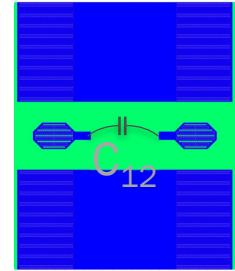
Results: verification (1/3)

Pad-open (no used for calibration)

Reference plane for SOLT



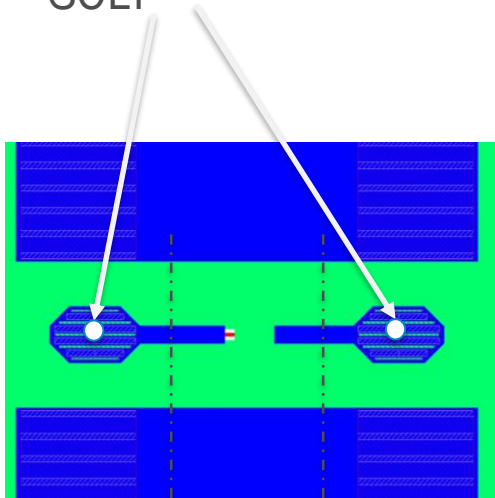
Reference plane for TRL and 16T



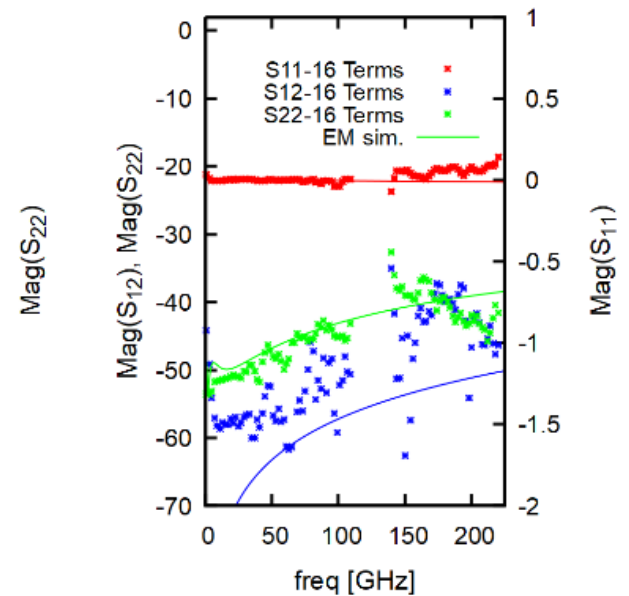
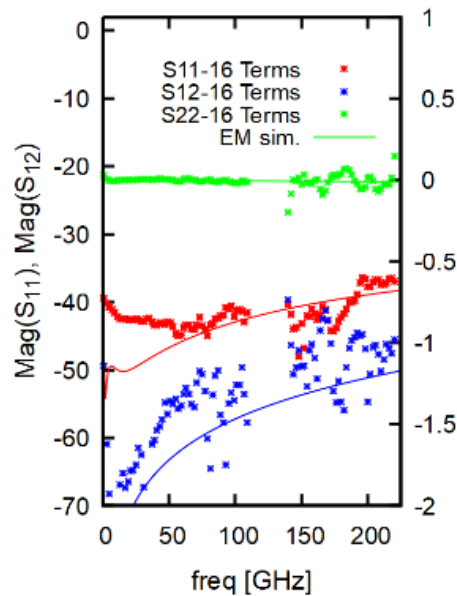
Results: verification (2/3)

Load-open and open-load (no used for calibration)

Reference plane for SOLT



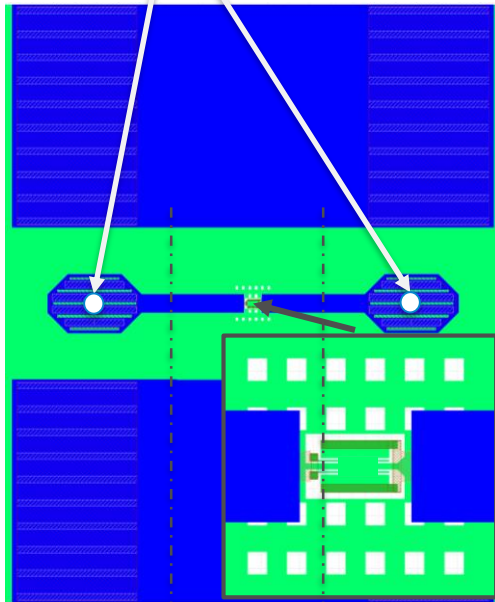
Reference plane for TRL and 16T



Results: verification (3/3)

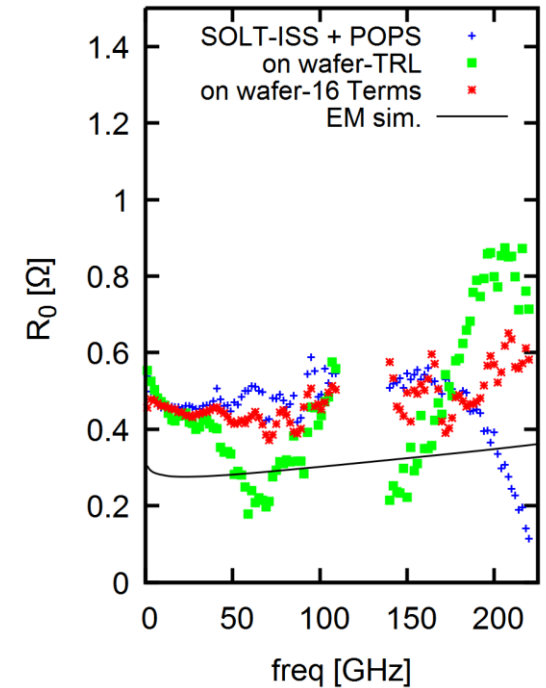
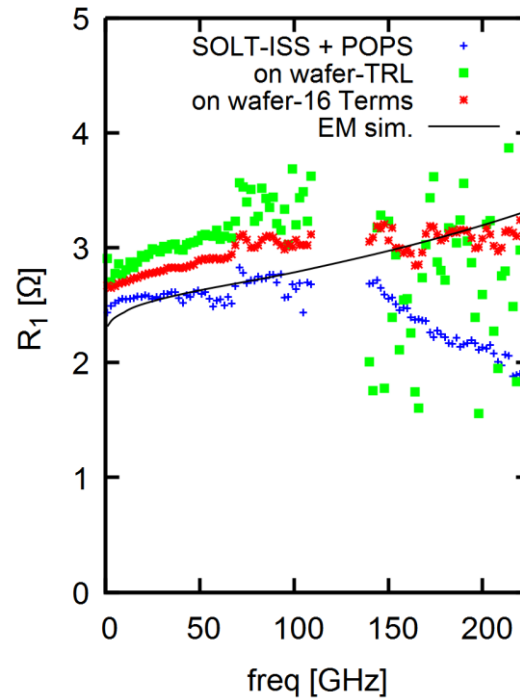
Transistor-short (no used for calibration)

Reference plane for
SOLT



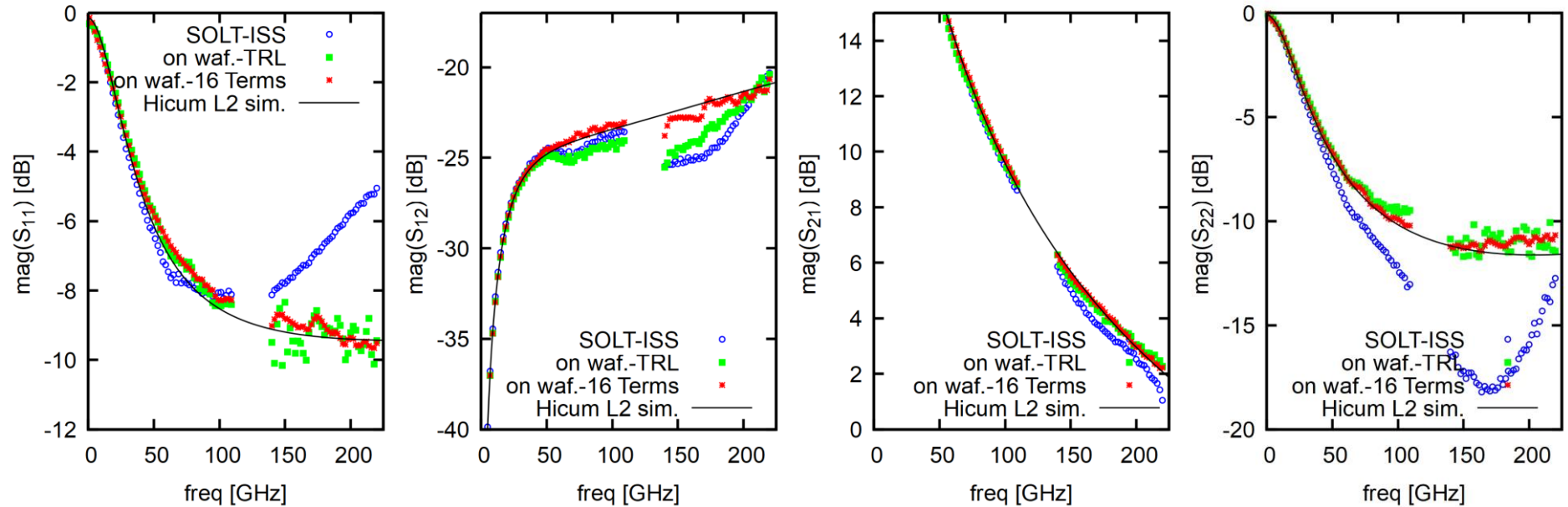
Reference plane for:

- TRL and 16T
- SOLT after pad-open/pad-short de-embedding



Results: transistor S parameters (2/2)

Measurement performed at $V_{BE}=0.9$ V and $V_{CB}=0$ V

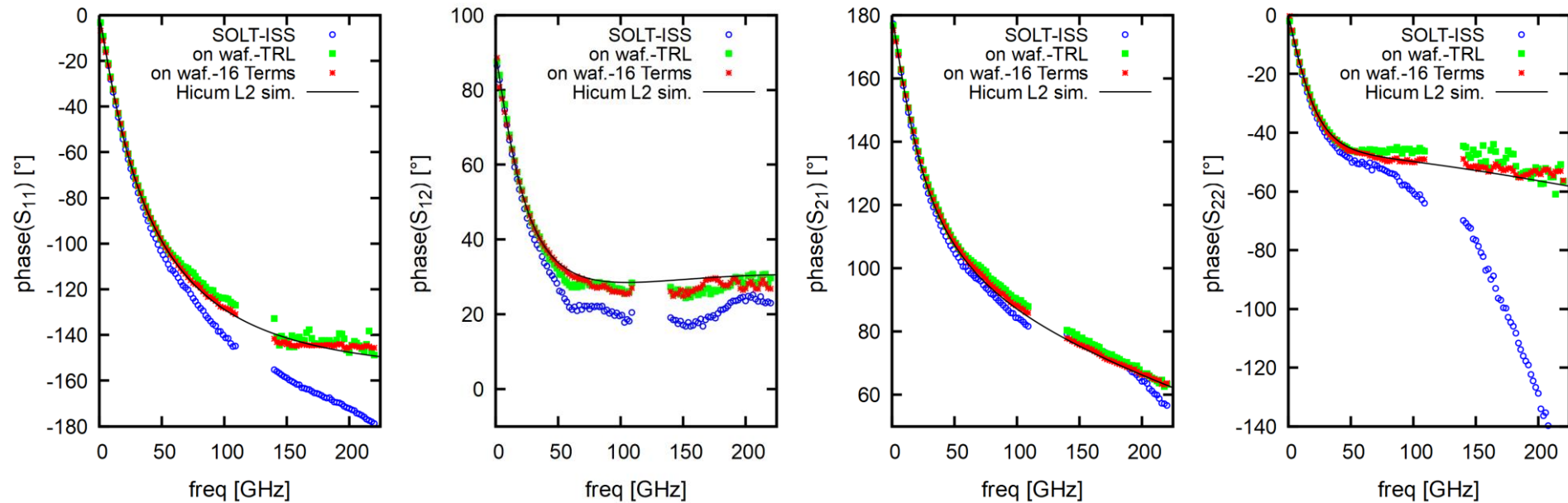


De-embedding is :

- transistor-short/transistor-open for TRL and 16T
- transistor-open/transistor-short for SOLT-ISS

Results: transistor S parameters (2/2)

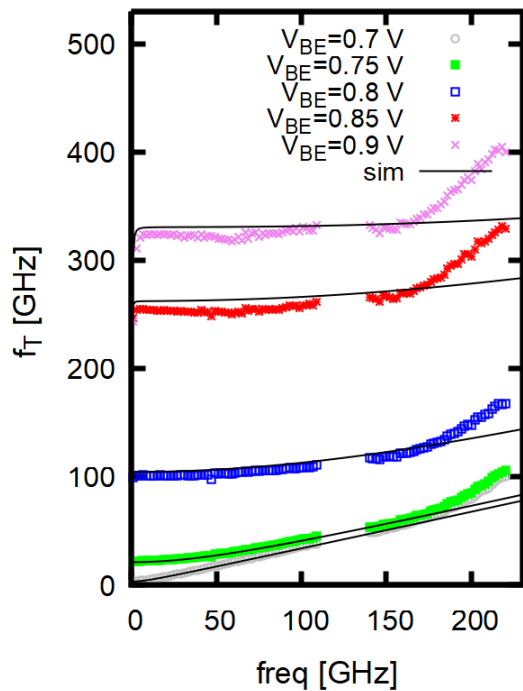
Measurement performed at $V_{BE}=0.9\text{ V}$ and $V_{CB}=0\text{ V}$



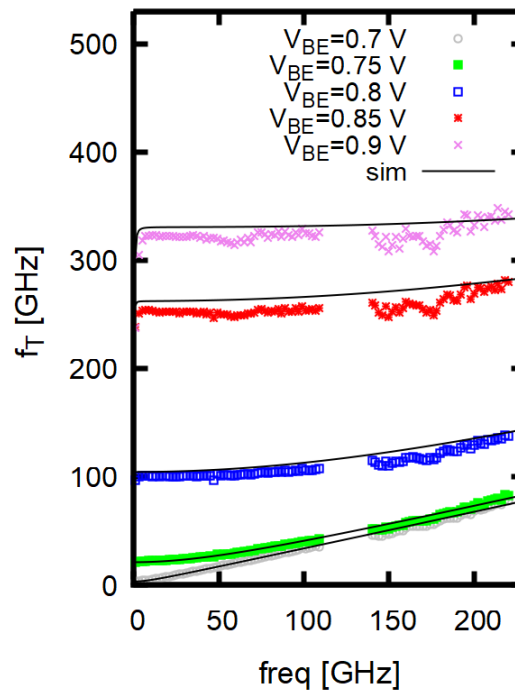
Results: transistor FOM measurement (1/2)

Transit frequency extraction: H21 current gain * frequency

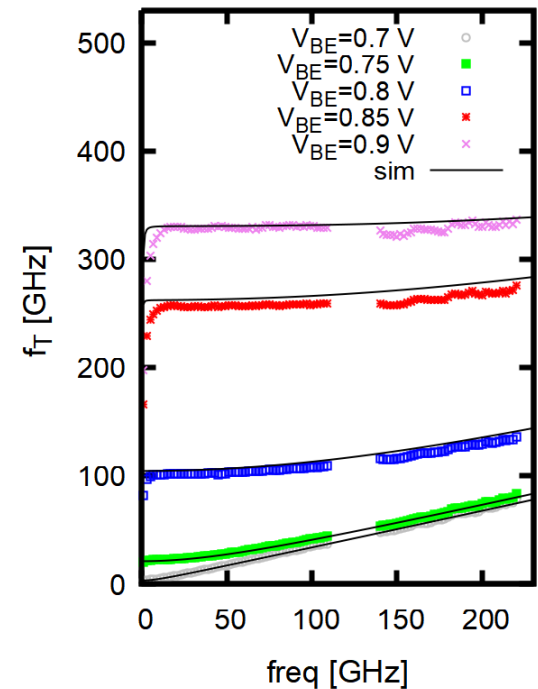
SOLT



On-wafer TRL



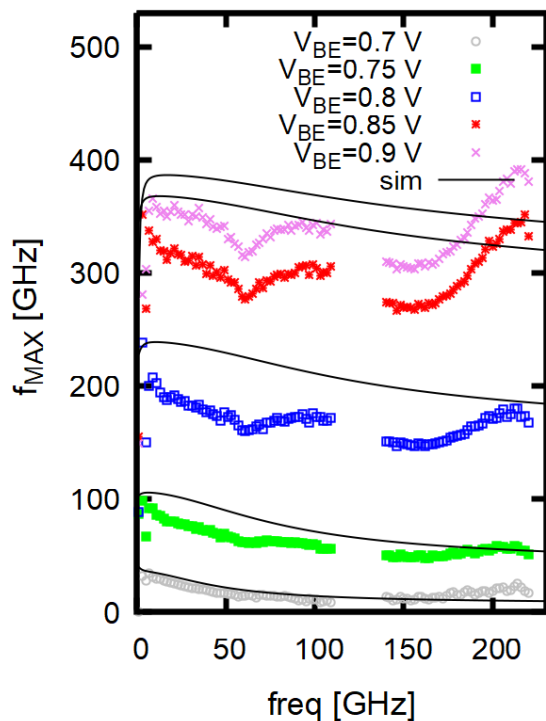
On-wafer 16 error terms



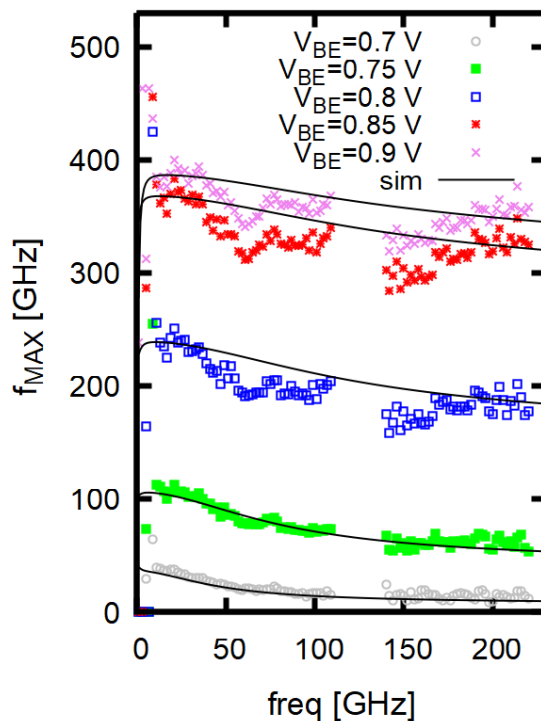
Results: transistor FOM measurement (2/2)

Maximum oscillation frequency extraction: $\text{Power gain}^{1/2} * \text{frequency}$

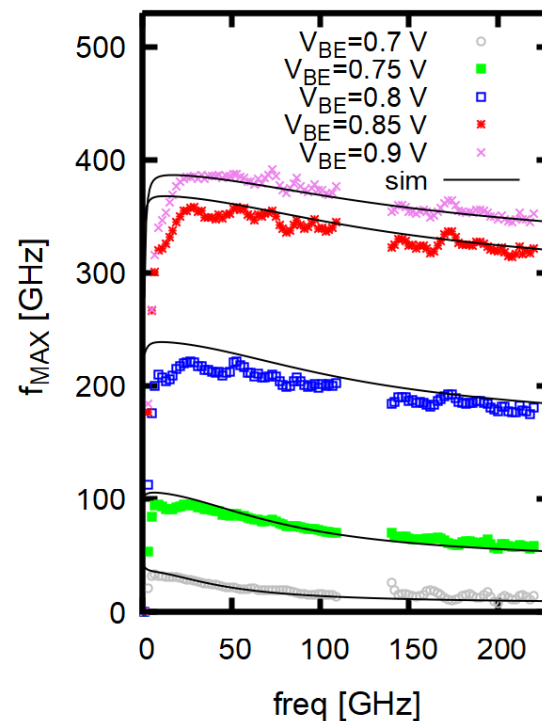
SOLT



On-wafer TRL



On-wafer 16 error terms



Conclusion

- 16 error-terms algorithm has been implemented in ICCAP using SVD (Python & PEL code)
- Specific standards have been designed in BiCMOS from STM
- Definition of reference standards has been done using EM simulation and TRL measurement
- TRL is efficient if crosstalk can be neglected (often not the case for high density Si techno.)
 - Otherwise, the 16 error-terms are recommended
- Outlooks: see the 16T calibration applied on BiCMOS 55X HBT ($f_{MAX} > 500$ GHz) (see it at IEEE [RWW2025](#)) showing almost no-band discontinuity on measurement up to 500 GHz

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- Acknowledgments to RF-Net and NANOCOM platform from IMS

References

- ▶ [1] J. V. Butler, D. K. Rytting, M. F. Iskander, R. D. Pollard, et M. Vanden Bossche, « 16-term error model and calibration procedure for on-wafer network analysis measurements », *IEEE Trans. Microw. Theory Tech.*, vol. 39, n° 12, Art. n° 12, déc. 1991, doi: 10.1109/22.106567.
- ▶ [2] S. Fregonese, « Analysis of high frequency measurement of transistors along with electromagnetic and SPICE co-simulation », *Rev. IEEE Trans Electron Devices*.
- ▶ [3] S. Fregonese, M. De Matos, M. Deng, D. Céli, N. Derrier, et T. Zimmer, « Importance of Probe Choice for Extracting Figures of Merit of Advanced mmW Transistors », *IEEE Trans. Electron Devices*, vol. 68, n° 12, Art. n° 12, déc. 2021, doi: 10.1109/TED.2021.3118671.
- ▶ [4] C. Yadav, « Importance and Requirement of frequency band specific RF probes EM Models in sub-THz and THz Measurements up to 500 GHz », *IEEE Trans. Terahertz Sci. Technol.*.
- ▶ [5] V. Jain et al., "415/610GHz f_T/f_{MAX} SiGe HBTs Integrated in a 45nm PDSOI BiCMOS process," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 11.6.1-11.6.4, doi: 10.1109/IEDM45625.2022.10019417.
- ▶ [6] B. Heinemann et al., « SiGe HBT with f_x/f_{max} of 505 GHz/720 GHz », in *2016 IEEE International Electron Devices Meeting (IEDM)*, déc. 2016, p. 3.1.1-3.1.4. doi: 10.1109/IEDM.2016.7838335.
- ▶ [7] S. Fregonese et al., « Comparison of On-Wafer TRL Calibration to ISS SOLT Calibration With Open-Short De-Embedding up to 500 GHz », *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, n° 1, Art. n° 1, janv. 2019, doi: 10.1109/TTHZ.2018.2884612.
- ▶ [8] L. Galatro et M. Spirito, « Millimeter-Wave On-Wafer TRL Calibration Employing 3-D EM Simulation-Based Characteristic Impedance Extraction », *IEEE Trans. Microw. Theory Tech.*, vol. 65, n° 4, Art. n° 4, avr. 2017, doi: 10.1109/TMTT.2016.2609413.