Sensorless Dual TSEP Implementation for Junction Temperature Measurement in Parallelized SiC Mosfets

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***Abstract*—This article presents a method for detecting temperatures distribution of two Silicon Carbide (SiC) Mosfets parallelized. Two Thermal Sensitive Electrical Parameters (TSEP), which are on state resistance (Rdson) and threshold voltage (Vth), are introduced. The comparison of the temperature interpolated by Vth and the one interpolated by Rdson shows disparity which can lead to individual junction temperature detection. Vth instability and its measurement are discussed for SiC devices. Experiment results show that depending on the instability of the Vth and the sensibility of the two TSEPs at certain temperatures, the combination of different TSEPs could be a solution to extract maximum junction temperature of parallelized devices.**

Keywords— SiC MOSFETs, parallelization, current and thermal imbalance.

I. Introduction

In power electronic, SiC MOSFETs can advantageously replace Si ones, thanks to various intrinsic characteristics, such as higher temperature applications, higher frequency switching and higher voltage operation [1-2]. A major drawback of this material is the difficulty in manufacturing wafers with limited imperfections, which leads to the need of manufacturing smaller dies compared to Si ones to get the same die per wafer yield [1]. Hence, parallelizing (same gate, drain and source connections) dies is mandatory for high current applications. This comes with other problems such as risk of current and thermal imbalance, which both can lead to dysfunctions. During the design phase, as newer power modules start to use 3D architectures, the thermal measurements of dies become very complex with traditional methods (IR camera, thermocouple…). Thus, the use of TSEP becomes mandatory. Nonetheless there is currently no method to detect thermal imbalance of parallelized dies via TSEPs, even though it is an important need [3].

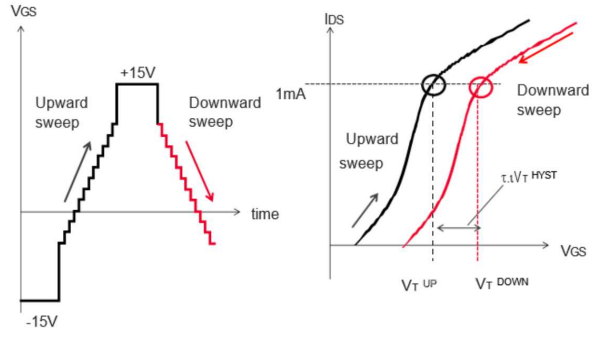

Fig. 1: Vth shift after stress applied to gate (from [5])

Another drawback of using SiC MOSFETs is their Vth shift which is a subject of discussion between industrials and researchers (see Fig. 1). Nevertheless, Vth is a key parameter because its instability plays a part in current imbalance during operation, and because it is an interesting TSEP. To mitigate the impact of Vth shift after stresses, conditioning methods have been developed [4] such as JEDEC guidelines [5] explaining circuits allowing precise measurement of Vth. The conditioning is usually achieved by applying a positive or negative voltage at the gate of the MOSFET while short-circuiting its drain and source, to remove carrier trapping. Measurement is then performed by short-circuiting gate and drain and by forcing a small current (see Fig. 2) through it. The resulting voltage is the Vth, which is known to be sensitive to the temperature variation of the die. In this work, the comparison of the temperature extrapolated by Vth and Rdson is investigated to determine disparity in SiC MOSFETs junction temperature.

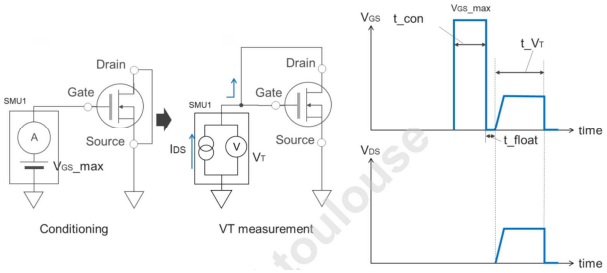

Fig. 2: JEDEC conditioning and Vth measurement method [5]

The SiC MOSFETs studied during tests and simulations were SCT070W120G3-4AG from STMicroelectronics.

II. Methodology

A. Simulations

Numerous TSEPs have been studied to determine which temperature they provide when a temperature imbalance is present between two MOSFETs. The simulations have been conducted with LTSpice software and manufacturer models have been used for MOSFET. In each study, the procedure is as follows: The T°=f(TSEP) is extracted from the model, considering two MOS parallelized with the exact same temperature (see Fig. 3 for an example on the Rdson); then simulations are conducted with thermal imbalance between the two devices. TSEP is calculated and a temperature is interpolated using the previously found equation.

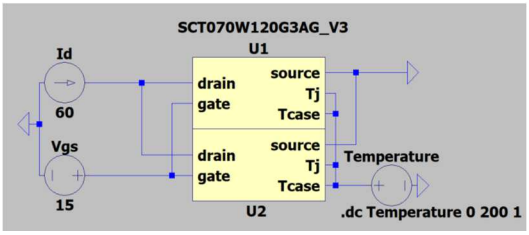

Fig. 3: Example of simulation to extract T°=f(Rdson)

For the same thermal imbalance, the interpolated Tj is compared depending on whether it was obtained with Vth measurement or Rdson measurement. As it can be seen in , the Rdson tends to extrapolate the average junction temperature of the two MOSFETs, whereas the Vth gives a hybrid one between max and average temperature (see Fig. 4).

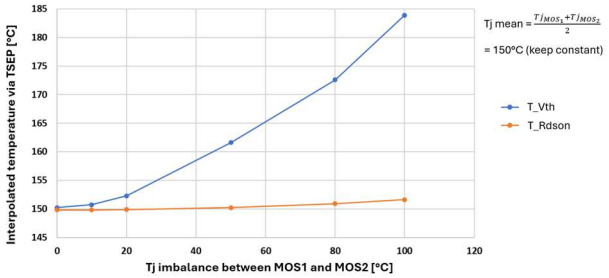

Fig. 4: Comparison of Tj obtained by Rdson and Vth simulation

With discordant junction temperatures obtained from those two TSEPs, it could be possible to extrapolate the temperature imbalance between the two MOSFETs and thus get an estimation of individual junction temperatures, even with totally parallelized MOSFETs where individual measurements are impossible.

B. *Test bench*

The objective of the bench is to perform quick measurements of Rdson and Vth with conditioning before the Vth measurement to detect thermal imbalance. The time between Vth measurement and Rdson one must be as short as possible to be sure to measure the same temperature. The test bench can be separated in two parts: the fluidic and electric ones. Tests have been conducted on the DepTH-LAB platform at Icam Toulouse [6].

a) Fluidic part

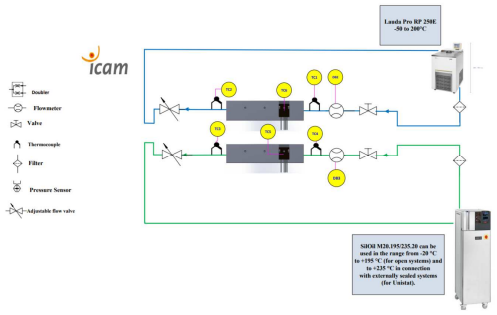

Fig. 5: fluidic part of the bench

The fluidic part can be seen in Fig. 5. Each parallelized MOSFET is thermally linked to one of the cryostats which enable to impose different ambient temperatures and hence different junction temperatures. The exposed pad of the MOSFET is in contact with heat sinks via TIMs. Fluids flow through heat sinks to extract thermal power dissipation and impose the ambient temperatures. Flowrates, inlet and outlet temperatures are controlled. In addition, two thermocouples (T-types) are placed under each MOSFET to measure the temperature as close as possible to the Tcase. The two cryostats used are RP205E from LAUDA (with P20.275.50 oil) and Unistat 510 from HUBER (with M20.195/235.20 oil). Oils used allow the liquid temperature (and so ambient temperature of MOSFETs) to reach 200°C maximum, for high temperature tests.

b) Electric part

As it can be seen in Fig. 6, the electric part of the bench can be separated into three subparts: current sources and switches (green), 4 states driver (red) and configuration changes + measurements (conditioning and Rdson to Vth configuration) (blue).

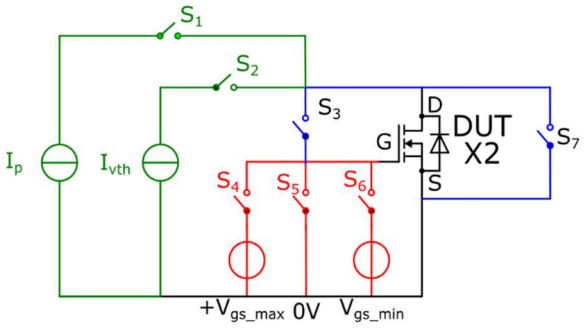

Fig. 6: simplified electric schematic of bench

Each test can be split into the following steps shown in Fig.7.

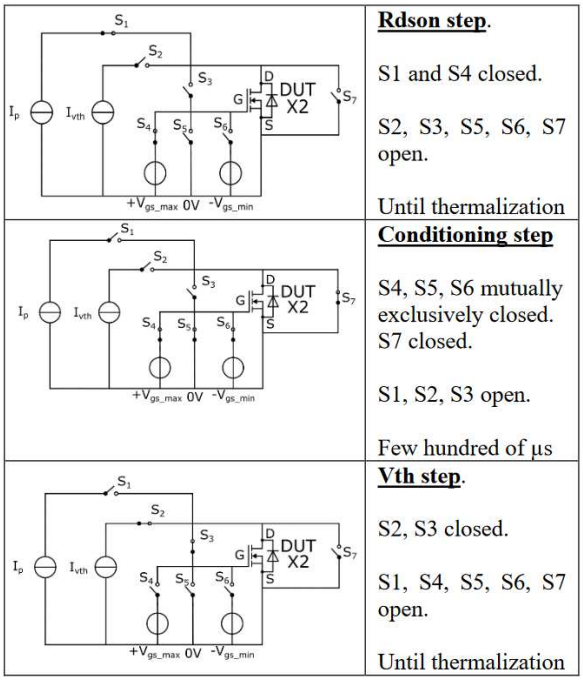

Fig. 7: temporal steps of the electric part of the bench

During the Rdson step, a voltage Vgs_max is applied to the gate (typically 15V). A constant current Ip is injected into the drain (typically 20A). The voltage is measured between drain and source to get the Vds and hence the Rdson. By opening the switch S1, the current is cancelled, and conditioning can begin, with the injection of various voltages during various times thanks to S4, S5 and S6. Switch S7 ensures that drain and source are short-circuited. This step is based on the JEDEC recommendations (see Fig. 2). Then all the switches are opened except switch S2 and S3. S2 allows a small current Ivth (10mA per parallelized MOS, usually 20mA). S3 ensures that drain and gate are short-circuited. The switches presented in schematics are, in fact, composed of two inversed IPTC007N06NM5 in series from INFINEON, which have very low Rdson (0.75 mΩ). They ensure that there is no electrical resistance when closed (true short-circuit, mandatory for S3) and that no current can go through when opened (thanks inversed and in series). Vth is measured via the Vds measurement; thus, the same probe is used to get both Rdson and Vth.

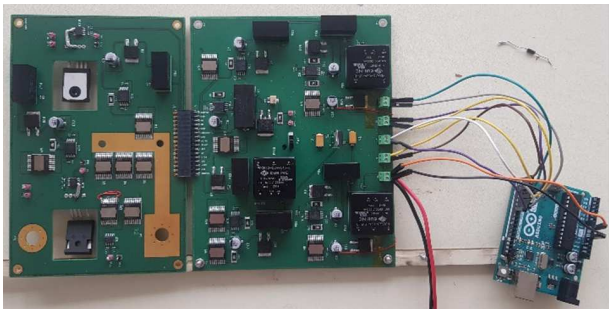

Fig. 8: photography of the electric part of the bench with its Arduino

Commands for all switches are managed by an Arduino Uno microcontroller (see Fig. 8) with direct manipulation of ports to achieve a minimum instruction execution time (time between two switch operations) of 50 ns.

Fig. 9: Oscilloscope and probes used

Measurement acquisition is done with a MSO58N of TEKTRONIX (see Fig. 9). The voltage probe for Vds is a TEKTRONIX TPP0500B and the power current is measured with a TEKTRONIX TCP0030A current probe. The current Ivth is generated by a SMU (Keithley 2612) and the current Ip by a EA-PS 2042-20B.

III. Results

First, all ten SiC MOSFETs had their Vth and Rdson measured individually (see Fig. 10 and Fig. 11). Since MOS 9 and 10 were the ones with the best matching Vth (3.524V and 3.526V), they were the two MOSFETs chosen to be parallelized. It must be noted that it seems to be no correlation between Rdson value and Vth value.

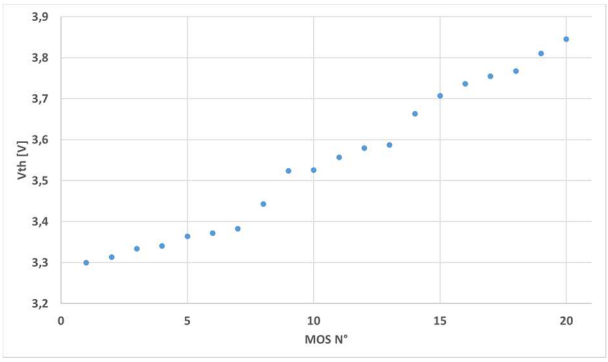

Fig. 10: Dispersion of Vth of 10 SCT070W120 (Vgs=Vds, Id=10mA) from the lowest to the higher value

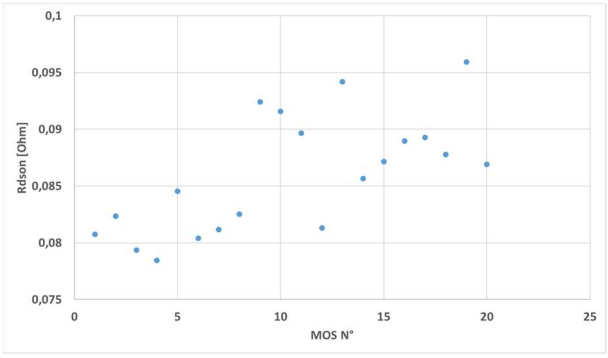

Fig. 11: Dispersion of Rdson of 10 SCT070W120 (Vgs=15V, Id=19A). Same order than Fig. 10

Once parallelized, tests were performed. The first objective was to demonstrate the feasibility of temperature imbalance detection. It was decided to perform long gate saturation to suppress traps and Vth instability before each measurement (1 second).

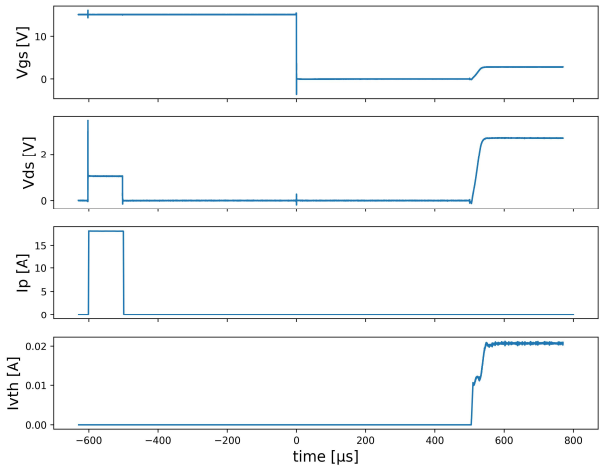

Fig. 12: Typical scenario for Rdson/Vth Tj comparison

Fig. 12 describes the scenario used to measure Rdson and Vth successively, after a one second conditioning (+15V on the gate, 0V Vds). The one millisecond between the Rdson measurement and the Vth one ensures that the Vth measured corresponds to the temperature imposed by the heating plate and not the self-heating during the Rdson phase. It means that for those tests, the junction temperature of each MOSFET is equal to the temperature of the cryostat.

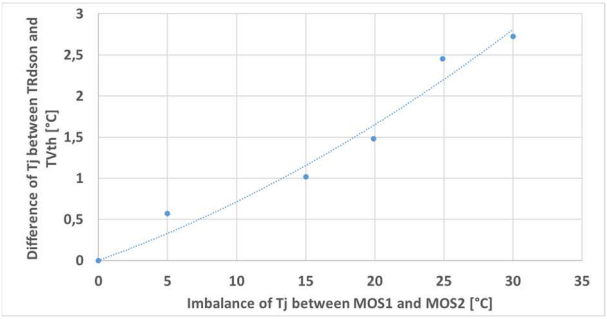

Fig. 13: Relationship between Imbalance of Tj measured with Rdson and Vth and imbalance between MOSFET1 and MOSFET2

The two MOSFETs were put to 100°C each. A test was performed and then the temperature of one MOSFET was increased to create a thermal imbalance. Measurements are performed and then thermal imbalance is increased again. Those tests are shown in Fig. 13 for SCT070W120G3-4AG. It can clearly be seen that there is a correlation between temperature imbalance between the two MOSFETs and the difference of temperature interpolated with Rdson and Vth.

Thermal Measurements			
T1 [°C]	T2 [°C]	Taverage [°C]	Difference (T2-T1) [C°]
121,70	121,40	121,55	0,30
121,70	128,20	124,95	6,50
121,80	140,10	130,95	18,30
121,80	148,00	134,90	26,20

Dual TSEP temperatures Estimations			
Difference (T1-T2)	Taverage [°C]	T1 [°C]	T2 [°C]
0,00	121,55	121,55	121,55
2,46	125,13	123,90	126,36
13,16	131,72	125,14	138,30
17,61	136,27	127,47	145,08

Electric measures		TSEP etimations		
Rdson [Ohm]	Vth [V]	Trdson [°C]	Tvth [°C]	DeltaT [°C]
0,055	2,792	121,55	121,55	0,00
0,056	2,771	125,13	125,29	0,16
0,058	2,728	131,72	132,67	0,94
0,059	2,699	136,27	137,61	1,33

Fig. 14: First SiC Results

With this correlation, new tests were performed (Fig. 14). This time, T1, T2, Vth and Rdson were measured. Vth and Rdson permitted a TRdson and TVth estimation, and the difference between these two values, using the equation given by Fig. 13, makes it possible to get an idea of the imbalance of temperature between the two MOSFETs. As the temperature interpolated by Rdson seems to be near of the average temperature of the two MOSFETs (see Fig. 4), it was then possible to get an evaluation of the individual temperature of the two MOSFETs, even if totally parallelized.

IV. Discussion

SiC results presented are the very first of an ongoing test campaign and should be regarded as a work in progress. Currently, only offline measurements have been conducted, without accounting for self-heating. Need of conditioning before measurement has not been studied.

Nonetheless, those first results are promising: as seen in Fig. 14, it is possible to detect temperature imbalance in simple cases. It must be noted that even if the imbalance is underestimated, it is much more precise than a single measurement of Rdson or Vth. New tests must be carried out at different ambient temperatures to determine if the results are or not reproductible. More importantly, tests with junction temperature increased by self-heating will be achieved as it is the goal of any TSEP.

V. Conclusion

A non-intrusive test has been developed to acquire the individual temperature of SiC MOSFETs in the case of total parallelization, using the Vth and Rdson TSEPs. Simulations conducted with LTSpice manufacturer models show good correlation with test results. First results on two SiC MOSFETs of STMicroelectronics are promising, and new tests are planned.

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