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Low-frequency Noise Performance of pMOS SOI Transistors for Analog Applications

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Abstract—This work assesses the low frequency noise level behavior for mesa isolated silicon-on-insulator (SOI) pMOS transistors dedicated to analog applications. Noise scaling with gate design, including gate length and gate width, is firstly studied. It demonstrates a nominal noise scaling with gate dimensions, even at small surfaces. Technological variants are then introduced, with forming gas anneal and source/drain engineering influence. On this technology our results demonstrate that forming gas anneal is efficient to reduce low frequency noise. The pMOS SOI transistor noise performance is finally compared to literature, illustrating promising noise figure of these devices isolated by mesa process.

Index Terms—SOI; low frequency noise; scaling; forming gas anneal

I. INTRODUCTION

Low frequency noise is one of the crucial parameter for analog electronic circuit performance. In the case of imager for instance noise level influences directly the signal-to-noise ratio, and is one of the limitation of these kind of devices [1]. Its measurement is therefore necessary to assess the technology performance. This paper reports low frequency noise (LFN) measurement analysis performed on mesa-isolated undoped SOI pMOS transistors, developed for 2.5V applications [2]–[4]. As reported in [2], mesa-isolation (showed by TEM image of Fig. 1) has a direct influence on transistor static characteristics and its influence on noise level need to be assess. In this context LFN results are presented for devices with variation of gate design (width W and length L) and technological processes (forming gas anneal and source/drain engineering).

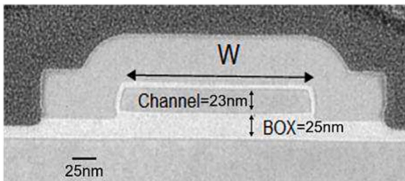


Fig. 1: TEM cross section of the SOI device under study

II. THEORETICAL BACKGROUND, DEVICES UNDER TEST AND EXPERIMENTAL PROTOCOL

The dominant source of noise in MOSFET transistor is traditionally flicker noise: the noise Power Spectral Density

(PSD) of drain current SI_d exhibits a $f^{-\alpha}$ dependency, with $0.7 < \alpha < 1.3$ [5]. Flicker noise in SOI transistors can be modeled thanks to the so-called unified model of flicker noise, which assumes a number of carriers fluctuation correlated with a mobility fluctuation, both due to trapping/de-trapping in slow oxide defects [6]. According to this model, the normalized drain current noise PSD is defined by the following equation:

$$\frac{SI_d}{I_d^2} = \frac{q^2 \lambda_t k_b T N_t}{W L f C_{ox}^2} \left(\frac{g_m}{I_d} \right)^2 (1 \pm \alpha_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m})^2 \quad (1)$$

In this equation, q is the Coulomb charge ($q = 1.6 \cdot 10^{-19} C$), k_b the Boltzmann constant ($k_b = 1.38 \cdot 10^{-23} J \cdot K^{-1}$), λ_t the tunneling constant in dielectric ($\sim 0.1 \text{ nm}$ for SiO_2), α_{sc} the remote Coulomb scattering coefficient, μ_{eff} the effective mobility, C_{ox} the gate oxide capacitance, f the frequency. g_m is the transconductance ($g_m = dI_d/dV_g$). W and L are respectively the gate width and the length. N_t is the oxide trap density in the volume of the oxide close to the interface, expressed in $\text{cm}^{-3} \cdot \text{eV}^{-1}$. The N_t parameter is used to qualify the technology in regards with its noise level, and ranges between $1.10^{15} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ and $1.10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ [7]. The measured SOI transistors are pMOS-type transistors whose characteristics fulfill requirements for imager application ($V_{dd} = 2.5V$) [2]–[4]: SiO_2 -polysilicon gate, 5 nm SiO_2 gate oxide thickness t_{ox} made by Rapid Thermal Oxidation (RTO), 23nm silicon-on-insulator film thickness t_{si} , 25nm buried oxide thickness t_{box} . They have an N-type Ground plane highly doped in-situ (Phosphorus, $N_d = 2 \cdot 10^{20} \text{ cm}^{-3}$). SOI film remains undoped. Various gate width and length are designed. Technological variants include devices with and without forming gas anneal, presence of Low Doped Drain (LDD) zone and presence of silicidation on source/drain zone. Low frequency noise is measured directly on wafer thanks to a programmable bias low noise amplifier connected to a Dynamic Signal Analyzer Keysight 35670A. With this experimental set-up minimal measurable PSD is $S \sim 2 \cdot 10^{-29} \text{ A}^2 \cdot \text{Hz}^{-1}$. For each device, the low frequency noise is measured from weak to strong inversion. For each polarization point three PSD are systematically measured: the total PSD is an average PSD of the three PSD measured. Transistors operate in ohmic regime ($V_d = -50 \text{ mV}$) and thermal regulation is set at 30°C . For each design and technological variant presented in this work, five devices are measured in order to take into consideration to some extent the dispersion of the noise characteristics.

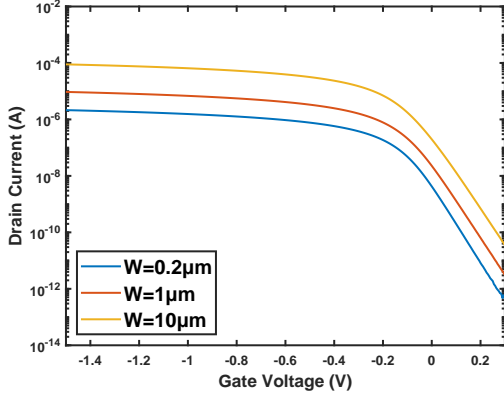


Fig. 2: $I_d(V_g)$ characteristics in semilog scale for gate width varying from $W=0.2\mu\text{m}$ to $W=10\mu\text{m}$.

III. NOISE SCALING WITH GATE DESIGN

The devices presented in this section have received a forming gas anneal, and have a LDD and silicidation zone.

A. Scaling with gate width

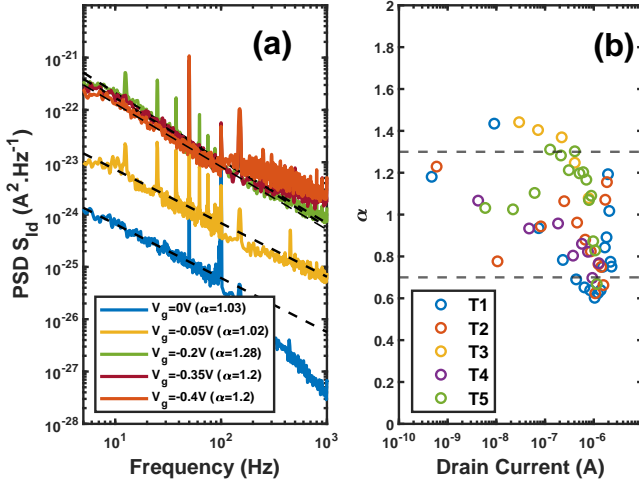


Fig. 3: Measurements realized on small surface transistor ($W/L=0.2/0.4$). (a): PSD as a function of frequency for several bias (solid line). These characteristics are fitted with $f^{-\alpha}$ curves (dotted line). (b): extraction of α coefficient on 5 (T1 to T5) transistors, as a function of drain current.

Noise evolution with gate width W is firstly assessed. Devices with W varying from $10\mu\text{m}$ to $0.2\mu\text{m}$ are measured. Gate length in this part remains constant, such that $L=0.4\mu\text{m}$. Fig. 2 firstly represents $I_d(V_g)$ in semilog scale of these devices, showing that current increases in weak and strong inversion as gate width increase. As surface of MOS transistors is scaled down, excess noise and apparition of RTN (Random Telegraph Noise) is likely to occur. RTN noise leads in particular to apparition of Lorentzian type PSD spectrum, with a $f^{-\alpha}$ dependency with α comprised between 1.5 and 2. Fig. 3.(a) represents example of PSD evolution as a function of

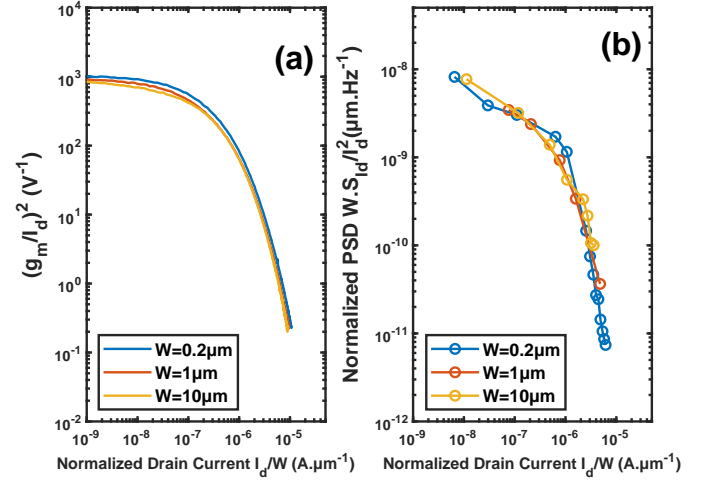


Fig. 4: (a): $(g_m/I_d)^2$ evolution as a function of I_d normalized by W in log-log scale for gate width varying from $W=0.2\mu\text{m}$ to $W=10\mu\text{m}$. (b): SI_d/I_d^2 normalized by W as a function of I_d (normalized by W) in log-log scale for gate width varying from $W=0.2\mu\text{m}$ to $W=10\mu\text{m}$. Normalized PSD is extracted at $f = 10\text{Hz}$.

frequency for various biases, on a $W=0.2\mu\text{m}$ device. Fig. 3.(b) represents coefficient α evolution as a function of drain current for the five $W=0.2\mu\text{m}$ devices measured. α is extracted at low frequency between 5Hz and 40Hz, in order to be localized under the low noise amplifier cutoff frequency. Measured PSD (Fig. 3.(a)) demonstrates the flicker noise presence with an extracted factor α (Fig. 3.(b)) ranging between 0.7 and 1.3, as expected from literature. Based on these results on five devices, there is no clear evidence of spectral deformation induced by RTN.

Noise scaling with width is now studied. Fig. 4.(b) represents PSD extracted at $f = 10\text{Hz}$ normalized by drain current and width ($SI_d/I_d^2 \cdot W$) for the various width studied, with respect to drain current normalized by width (I_d/W). Fig. 4.(a) represents evolution of $(g_m/I_d)^2$ with respect to drain current normalized by width (I_d/W). SI_d/I_d^2 is width dependent, as the surface of transistor varies: the more the gate surface is important, the lower is the noise. It is perceptible on the W normalized SI_d/I_d^2 where equal characteristics whatever the width are obtained. SI_d/I_d^2 evolution whatever the width is moreover correlated with the $(g_m/I_d)^2$ ratio presented in Fig. 4.(a). This correlation is anticipated by the unified model of flicker noise introduced in part II. This correlation allows the extraction of the N_t parameter. Fig. 5.(a) represents an example of N_t parameter extraction on a $W=0.2\mu\text{m}$ device. N_t is extracted thanks to a polynomial fit related to the unified model of flicker noise introduced in part II. The methodology is applied on the measured devices, and Fig. 5.(b) represents the average N_t with its standard deviation extracted on the devices according to the width. Scaling of SI_d/I_d^2 presented Fig. 4.(b) is nominal in regards with evolution predicted by the theoretical model: N_t parameter extracted is similar between various width devices, with a value in average $N_t \sim 1.6 \cdot 10^{16} \text{cm}^{-3} \cdot \text{eV}^{-1}$. These results show that small

surfaces devices based on the SOI technology introduced in part II do not exhibit excess noise, by comparison with larger surfaces. Based on these results, the mesa isolation does not influence low frequency noise, which is consistent with the undoped SOI film studied in this work [2]. the N_t parameter values are among the best values reported in state of the art whatever the width, as will be introduced afterwards in Part V. It is worth to notice finally that dispersion on the N_t parameter seems to increase as width decrease. This increase of dispersion in small surface devices was measured on $I_d(V_g)$ characteristics as well.

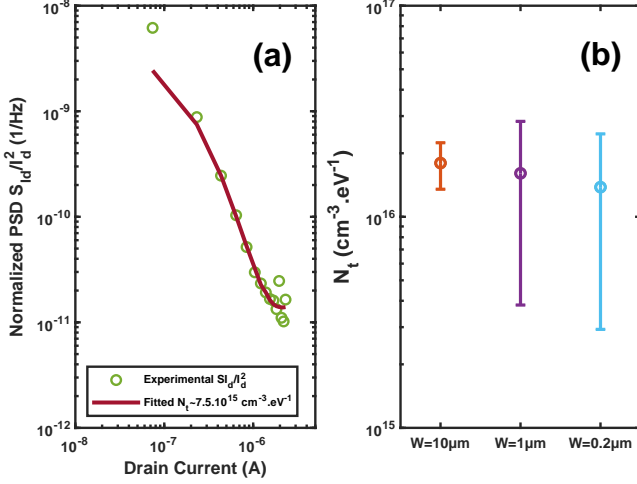


Fig. 5: (a): example of extraction of the N_t parameter. Experimental data (circles) are polynomial fitted according to the unified flicker noise model (solid line). (b): Average N_t parameter extracted on various width devices.

B. Evolution with gate length

Devices with $L=10\mu\text{m}$ and $L=1\mu\text{m}$ gate length were measured and compared to $L=0.4\mu\text{m}$ devices. Same width devices are considered ($W=0.2\mu\text{m}$). Fig. 6 represents α coefficient extracted according to the same methodology than in part III.A on $L=1\mu\text{m}$ device. Logically, given the results of part III.A, α coefficient extracted ranges between 0.7 and 1.3 denoting presence of flicker noise. Fig. 7.(a) gives an example of N_t parameter extraction on $L=1\mu\text{m}$, showing once again a good correlation between unified model of flicker noise and experimental data. Fig. 7.(b) compares average N_t parameter of $L=1\mu\text{m}$ and $L=10\mu\text{m}$ devices to $L=0.4\mu\text{m}$ devices. Average N_t extracted on $L=1\mu\text{m}$ and $L=10\mu\text{m}$ devices stand in the same range than on $L=0.4\mu\text{m}$ devices: decreasing the gate length has no significant influence on the low frequency noise general level. This result is moreover consistent with [2], that indicates that static characteristics of transistors studied in this work are not affected with short channel effect at $L=0.4\mu\text{m}$.

IV. INFLUENCE OF TECHNOLOGICAL VARIANTS STEPS ON NOISE

A. Forming gas anneal influence

Devices without forming gas anneal (FGA) was included in the technological batch. The effect of FGA on noise is uncer-

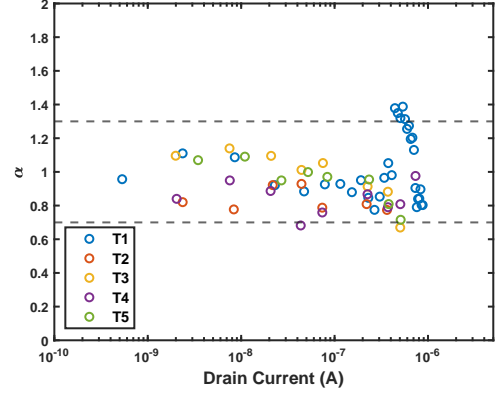


Fig. 6: extraction of α coefficient on five $L=1\mu\text{m}$ transistors (T1 to T5) as a function of drain current. Width is constant ($W=0.2\mu\text{m}$).

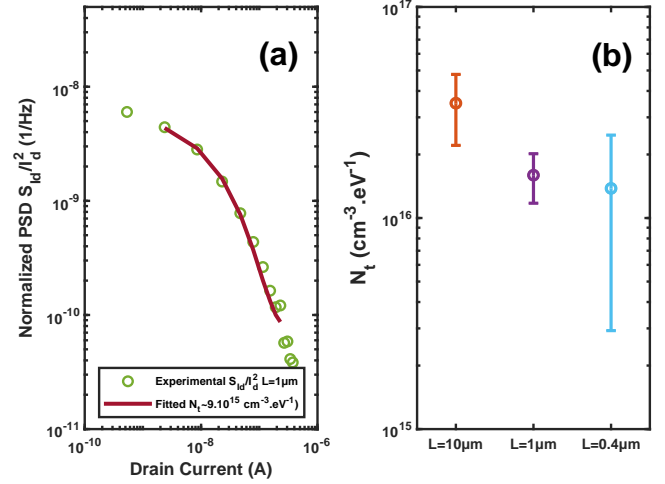


Fig. 7: (a): example of extraction of N_t parameter. Experimental data (circles) are polynomial fitted according to the unified flicker noise model (solid line). (b): Average N_t parameter extracted on various length devices.

tain on advanced MOS technology, as gate stack complexity increases: its influence needs therefore to be assess. The low frequency noise with and without FGA was measured on five small surface ($W/L=0.2/0.4$) devices. Fig. 8.(a) represents an example of the comparison of two devices with and without FGA in terms of input-referred noise SV_g ($SV_g = SI_d/g_m^2$). SV_g is extracted at $f = 10\text{Hz}$. A clear decrease of noise is measured on FGA device in weak and strong inversion. This decrease is confirmed in Fig. 8.(b) with the extraction of the average N_t parameter on devices without FGA: an average factor 6 is perceptible between with and without FGA devices, favoring FGA devices. This difference is higher than the dispersion range calculated on these devices. These results confirm the FGA anneal is still operational on the SOI transistor technology studied in this work.

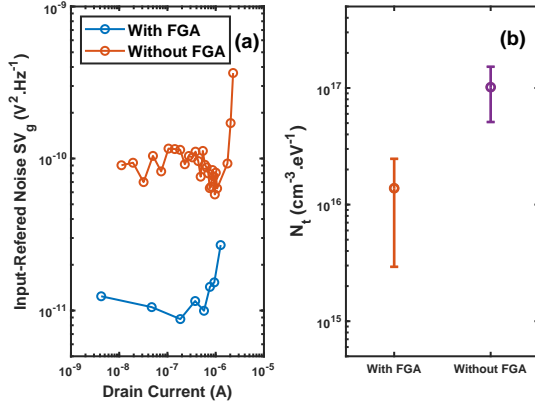


Fig. 8: (a): input referred noise SV_g (SI_d/g_m^2) extracted at $f = 10Hz$ as a function of drain current of devices with and without forming gas anneal. (b): Average N_t parameter extracted on devices with and without forming gas anneal.

B. Source/drain engineering influence on noise

Devices without drain and source silicidation (Fig 9.(b)) and without Low Doped Drain (LDD) (Fig 9.(c)) zone were included in the technological batch. These two variants received a FGA. Fig. 9.(d) reports extracted N_t on devices of these two variants, compared to the reference with LDD and with silicidation zone (Fig 9.(a)). No clear influence of these two source/drain engineering variants are perceptible on the general level of noise: N_t parameter extracted ranges between of $2 - 3 \cdot 10^{16} cm^{-3} \cdot eV^{-1}$, which stand in the reference with LDD and with silicidation zone dispersion range.

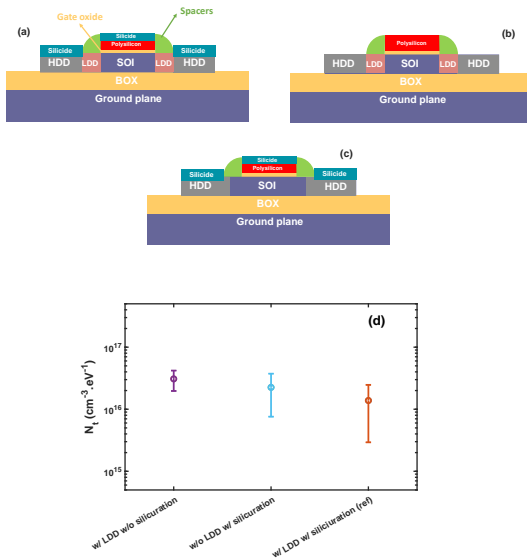


Fig. 9: (a),(b),(c): schematic representation of the SOI transistor respectively with LDD and silicidation zone (a), without silicidation zone (b) and without LDD zone (c). (d): Average N_t extracted on devices without silicidation zone and without LDD.

V. COMPARISON WITH LITERATURE

Extracted values of N_t parameter are finally compared in Fig. 10 with references in literature, with respect to the Equivalent Oxide Thickness (EOT). The latter are values obtained on pMOS bulk [7], 22nm FDSOI [8] and PDSOI [9]. The SOI technology presented in this paper stands among the best values reported in the state of the art, despite mesa technology isolation, small surface transistor measured, and thin SOI film (by comparison with PDSOI).

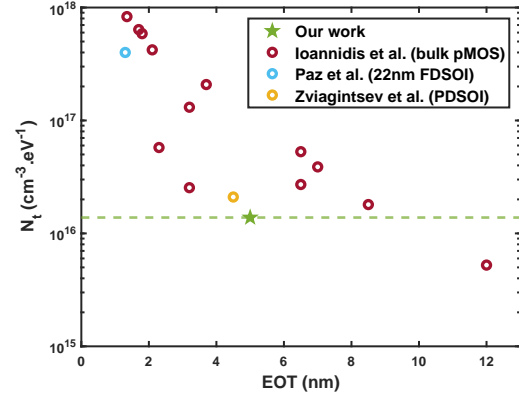


Fig. 10: Comparison of our work against N_t parameter extracted from literature. Results are presented with respect to the EOT thickness.

VI. CONCLUSION

This paper presented low frequency noise measurement on pMOS SOI transistor. Measurements demonstrated a promising noise level of these devices, including a correct scaling between large and small gate surfaces. Values of noise are among the best values reported in state of the art, despite mesa SOI technology. Mesa isolated pMOS SOI transistors are therefore promising devices for low noise applications.

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