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1200V fully vertical GaN-on-Silicon P-i-N diodes with avalanche capability and high on-state current above 10 A

Youssef Hamdaoui, Sondre Michlerson, Adrien Bidaud, Katir Ziouche, and Farid Medjdoub

Abstract— We report on fully vertical GaN-on-Silicon P-i-N diodes delivering above 1200 V soft breakdown voltage. Temperature dependence measurements indicate avalanche breakdown capability reflecting the high-quality processing and epitaxy growth. On-state characteristics of the fabricated vertical P-i-N diodes reveal on-resistances ranging from 0.48 mΩ.cm² for small anode to 1.7 mΩ.cm² for large anode diameters (i.e. 1 mm). The on-state resistance increase is attributed to the thermal dissipation issues. Nevertheless, the large devices exhibit high on-state current close to 12 A owing to an optimized process including a deep mesa etch as edge terminations and thick Cu layer for heat sink on the backside enabled by a polyimide passivation that strengthens the mechanical robustness of the membranes. To the best of our knowledge, this represents the first demonstration of fully vertical 1200 V GaN-based devices grown on silicon substrates with high current operation above 10 A, corresponding to a Baliga figure of merit of 3 GW/cm².

Index Terms— GaN-on-Silicon, fully vertical, 1200 V breakdown, high current, power diodes, Local substrate removal, avalanche, High breakdown voltage, low Ron.

I. INTRODUCTION

THE high demand for superior performance and reliable power electronic devices at low-cost fabrication requires the development of new technologies. Gallium nitride (GaN) based lateral High Electron Mobility Transistors (HEMT) offer promising physical properties such as a high critical electric field, high mobility, and a large bandgap. Additionally, the cost of GaN device fabrication can be reduced by employing silicon as a substrate. However, the use of GaN lateral devices in high volume applications beyond 600 V operation is still limited due

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to remaining reliability issues, especially when using large device area. Indeed, the blocking capability of lateral GaN devices suffers from destructive breakdown affecting the circuit level reliability. Consequently, lateral GaN-based devices require oversized dimensions to both deliver high current and to withstand the blocking voltage with a proper margin (typically 50% to 100% below the destructive breakdown voltage). In addition, the complexity of the epitaxy and the 2DEG proximity from the surface make the devices more sensitive to electron trapping issues [1]-[3]. Therefore, the development of vertical GaN devices for medium and high voltage operation is necessary to unlock the potential of this material. Recently, vertical GaN-based power devices grown on GaN bulk substrates have shown excellent performance, including low on-state resistance (Ron), and high non-destructive breakdown voltage (BV) [4], [5]. However, GaN substrates are still expensive and not yet commercially viable to produce low-cost power devices [6]. On the other hand, high performances have been recently demonstrated on silicon substrate, using P-i-N or Schottky design, which would be an attractive choice from performance / cost balance point of view [7]-[19].

The most common design in literature to fabricate GaN-on-Silicon vertical devices is the pseudo vertical structure (PVS). In this case, the bottom contact layer is accessed from the frontside by deep etching. However, current transport in PVS do not strictly follow the vertical direction as an additional lateral path is created at the bottom N+ layer. This results in a crowding effect that significantly affects the on-state resistance when using large anode area (mm scale), required to generate high current. In turn, thermal issues are enhanced in large PVS devices, preventing high current spreading. That is why the development of fully vertical devices (FVD) is essential. This can be achieved by means of local substrate and buffer removal through the backside to access the bottom N+ layer (Fig. 1) while preserving the material quality [20]-[22]. However, the substrate removal makes the resulting membranes fragile. This, in turn, prevents the implementation of a proper heat sink such as thick copper electroplating in order to reduce the thermal dissipation and deliver high current. In addition, backside ohmic contacts to N-face GaN are challenging as the crystal polarity of the GaN surface affects the Schottky barrier height and is prone to a high oxidation rate [23]-[25].

In this paper, we demonstrate state-of-the-art fully vertical P-i-N diode with low Ron (0.48-1.7 m Ω .cm²) and high breakdown voltage (1230 V). The fabricated diodes show a signature of avalanche breakdown and deliver close to 12 A on-state current. This was achieved by using an optimized fabrication process including polyimide passivation, a thick Cu electroplating (300 μ m) and HCl wet treatment enabling low contact resistance non-alloyed N face ohmic contact backside.

II. DEVICE STRUCTURE AND FABRICATION

A 2 \times 6" GaN-on-Si wafer was grown by Metalorganic Chemical Vapor Deposition (MOCVD). The GaN-based P-i-N epitaxial structure for the first wafers contains: a 1.5 μ m thick buffer layer, a 500 nm Si-doped (5×10^{18} cm⁻³) N⁺-layer, a thick 7.4 μ m drift-layer slightly Si-doped (of 3×10^{16} cm⁻³, corresponding to a net ionized doping of 9×10^{15} cm⁻³ as extracted by means of electrochemical capacitance-voltage (ECV), and a 700 nm thick Mg-doped (5×10^{19} cm⁻³, corresponding to 3×10^{17} cm⁻³ active doping) P-layer. More details about the growth can be found in [26]. The second wafer has identical epitaxial parameters except for the drift region thickness, which was reduced to 4.5 μ m. This wafer has an avalanche capability with 800 V breakdown voltage which were demonstrated using a pseudo vertical design [19]. It serves for the optimization of bevelled mesa depth as edge termination. The threading dislocation density within the two heterostructures is estimated to 5×10^8 cm⁻² as assessed by weak beam darkfield TEM with an FEI Titan 80–300 microscope operating at 300 keV. The electron mobility within the drift region was measured by means of Hall effect measurements and found to be ~ 756 cm²/Vs. The fully vertical P-i-N diodes were fabricated starting from the frontside. A plasma-enhanced chemical vapor deposition (PECVD) SiO₂ film was used as a mask, which was opened with a SF₆-based plasma reactive ion etching (RIE) to define a deep mesa variation used as edge termination to spread the electric field at the junction's periphery and reduce the leakage current. A deep bevelled mesa was then created using an optimized Cl₂-based inductively coupled plasma (ICP) recipe (Fig. 1.b). The choice of a bevelled mesa profile was found to be effective in the reduction of leakage current, breakdown voltage uniformity and avalanche capability [4], [27], [28]. This was followed by a Ni (20nm)/Au (200 nm) metal stack deposited on the P-layer using evaporation. The contacts were annealed at 500°C in a mixed environment (N₂+O₂) in order to form ohmic contacts to the P-layer. An additional Ti (100 nm)/Au (1 μ m) pads were deposited using evaporation. A critical challenge of fully vertical GaN-on-silicon device fabrication approach is the robustness of the resulting membranes subsequent to the silicon and buffer layers backside removal. Within this framework, polyimide encapsulation can be used both as a passivation layer protecting against peak electric field but also to fill in the deep mesa trenches and thus strengthen the membranes. The polyimide filling process involved a three-steps spin coating approach to overcome the challenge related to the deep mesa. An initial low-speed ramp ensured the trench filling (especially of the corners), then a medium-speed ramp improved uniformity, and finally a high-speed ramp enables reaching the desired thickness. A post-baking step with varied proximity settings

was also introduced to enhance the coverage. After the deposition of thick polyimide (Fig. 1.b), a thick layer SiO₂ was used to protect the frontside. The silicon substrate was thinned down from 1 mm to 300 μ m and locally etched using deep reactive ion etching (DRIE), followed by the buffer layer etching using ICP.

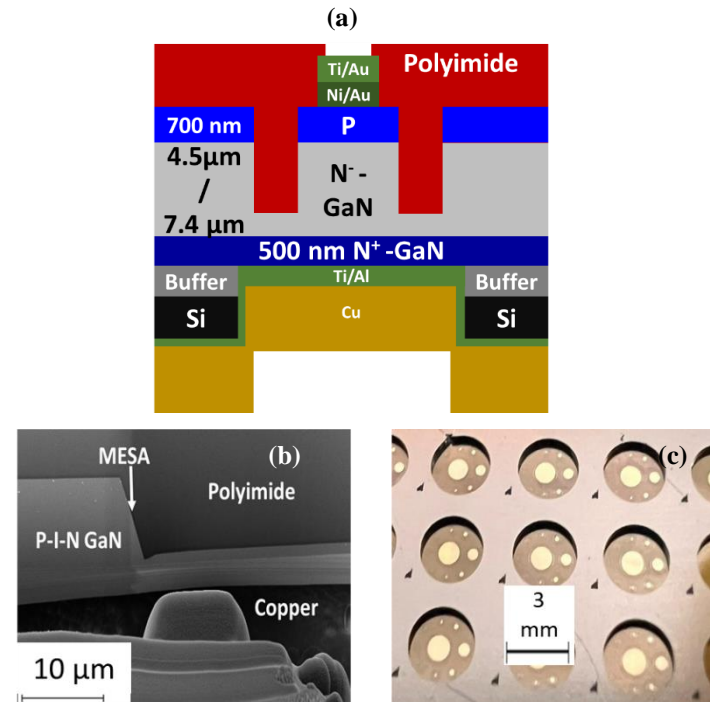


Fig. 1. (a) Schematic cross section of the fully vertical PIN diodes. (b) Focused ion beam cross section image of the vertical diodes. (c) optical image of the backside after silicon and buffer removal where the frontside circular diodes appear by transparency.

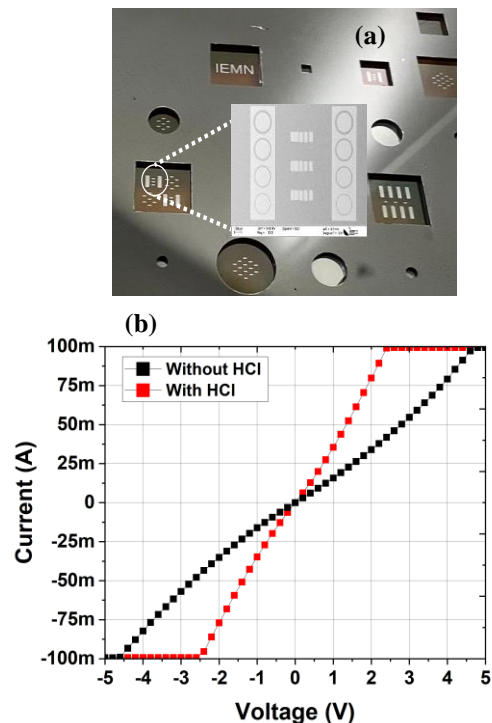


Fig. 2. (a) Image of TLMs inside the membranes. (b) TLM measurements with and without HCl wet treatment.

Fig. 1.c shows a backside view of the fabricated devices where the circular diodes on the frontside are visible through the membranes. We used large circular membrane with 3 mm diameter. To assess and optimize the backside ohmic contacts to N-face GaN, Ti/Al (25/100 nm) TLMs were patterned using direct laser writing lithography since standard photolithography is not applicable on non-planar surfaces (Fig. 2.a). Initial TLM measurements showed a poor ohmic contact quality with high contact resistances ($>10^{-4} \Omega \cdot \text{cm}^2$). To enhance the ohmic contact, an HCl wet treatment was developed and found to be effective in reducing the contact resistance ($9 \times 10^{-6} \Omega \cdot \text{cm}^2$), as seen in Fig 2.b. More details about this pretreatment can be found in reference [29]. Finally, the fully vertical device processing ended with the deposition of Ti(25nm)/Al(100nm) and Cu (300 μm) using evaporation and electroplating, respectively (see Fig. 1). It is important to note that the highly strained thick Cu deposition is enabled by the polyimide protection on the frontside that strengthens the mechanical robustness of the membranes, otherwise resulting in cracked and damaged devices.

III. RESULTS AND DISCUSSION

Fully vertical P-i-N diodes using 4.5 μm drift region thickness were fabricated using a deep mesa variation to assess the impact of this parameter both on leakage current, and breakdown voltage (soft or hard). Silvaco TCAD simulations were conducted to gain further insight into the electrical behavior of the fabricated devices across different mesa depths, ranging from 0.7 μm to 5.2 μm . Figure 3.a shows the off-state characteristics of the fully vertical design with varying mesa etching depths, while these measurements are compared to the TCAD simulation results in Figure 3.b. Both experimental data and simulations reveal a significant reduction in leakage current as the mesa depth increases up to 2.5 μm (see Figure 3.b). The blocking voltage at 10 μA is significantly reduced as current flow is inhibited for deeper mesa depths. For mesa depths below 2.5 μm , residual leakage along the sidewall creates a pathway, leading to higher leakage currents. Specifically, at 10 μA leakage current, TCAD simulations indicate that the peak electric field within the P-i-N diodes is concentrated between the P and N- layers, further contributing to sidewall leakage when the mesa depth is shallower (Figure 4). As a result, lower breakdown voltages are observed for shallow mesa depths. Conversely, with a deeper mesa ($> 60\%$ of the drift + P region thickness), the breakdown voltage is improved, reaching 760 V in this case, demonstrating the advantages of a deeply beveled mesa. Furthermore, it is worth noting that the 4.5 μm diode with deeper mesa etching exhibited non-destructive soft breakdown behavior, suggesting avalanche capability.

Figure 4 illustrates the electric field distribution at 800 V for mesa depths of 1 μm , 2 μm , and 4.5 μm . For the 1 μm mesa, the electric field peaks at more than 3 MV/cm, causing premature breakdown, while this peak is entirely eliminated with the 4.5 μm mesa.

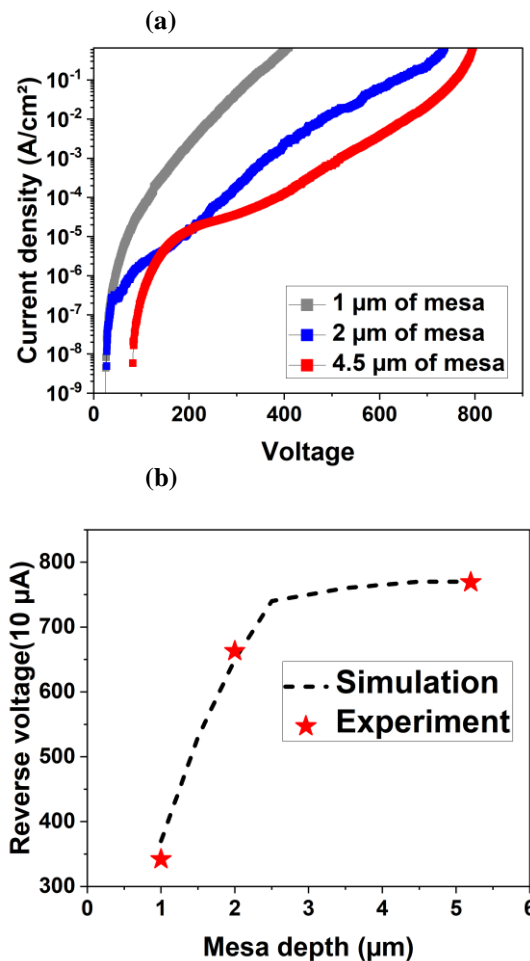


Fig. 3. (a) off-state characteristics of the fully vertical 4.5 μm P-i-N diodes using various mesa etching depth. (b) Experimental and simulated reverse voltage at 10 μA leakage current

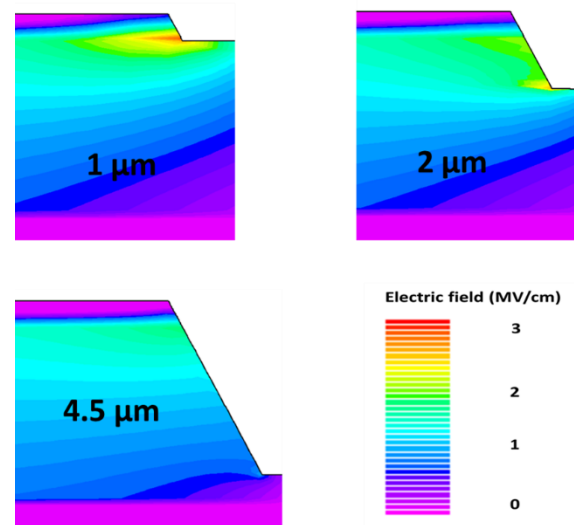


Fig. 4. Electric field distribution at 800 V of the fully vertical 4.5 μm P-i-N diodes using various mesa etching depth.

During the fabrication process of the fully vertical GaN on Silicon P-i-N diodes with 7.4 μm drift region, the deep mesa edge termination ratio (60 % of the total drift and P layer thickness) has been fixed to 7.3 μm . Fig. 5.a presents the reverse characteristics of fully vertical 7.4 μm drift layer thickness P-i-N diodes with various anode size (from 50 μm to 1000 μm). We can observe a uniform breakdown voltage > 1200 V. The increase of diode diameter affects neither the leakage current nor the breakdown voltage. This reflects the high growth and processing quality as larger area potentially involves more defects through the heterostructure or the mesa sidewalls.

Fig. 5.b plots typical reverse characteristics of the fully vertical GaN on Silicon P-i-N diodes (with 7.4 μm drift region) at various temperatures for small diodes size ($d < 100$ μm). At room temperature, a high breakdown voltage of 1230 V and low leakage current are observed. The P-i-N diode breakdown voltage translates to a high critical electrical field at the junction > 2.2 MV/cm, calculated using the described equation in ref [30]. This translates to an average electric field across the drift layer of 1.66 MV/cm. No additional leakage path was induced by the device processing owing to the optimized deep mesa etching [5]. Moreover, the P-i-N diode exhibits a soft breakdown, hinting at the avalanche capability. It can be pointed out that this is an essential feature for the industrialization of these new types of devices. The avalanche breakdown provides indeed a safe leakage current path that protects the devices from irreversible damages. In this case, the leakage current is induced by the impact ionization of the accumulated carriers when exceeding a specific energy. Increasing the temperature causes a delay in the onset of impact ionization due to phonon scattering. Therefore, a higher reverse bias is needed at higher temperatures to achieve the same energy level. In other words, when the temperature increases, the soft breakdown voltage increases as seen in Fig. 3.b showing the temperature dependence of BV, which were measured on the exact same device for each temperature, confirming the signature of the avalanche capability slightly above 1200 V. the temperature coefficient of avalanche breakdown was estimated to be 2×10^{-4} K $^{-1}$. It is important to mention that the avalanche signature was observed uniformly on the small diodes (diameter ≤ 100 μm). Concerning the large diodes, even though a soft breakdown was observed, the breakdown voltage does not increase with the temperature and shows hard breakdown. The absence of soft breakdown for large diodes is attributed to the larger amount of defects that may contribute to increase the leakage current, especially at high temperature preventing the avalanche phenomenon. This suggests that defect-assisted tunneling or trap-assisted recombination may dominate the leakage current in these devices.

Fig. 6 shows the forward characteristics and $R_{\text{ON,sp}}$ of representative fully-vertical circular P-i-N diodes with various anode diameters. For small diodes (≤ 200 μm), CW DC measurements were performed while large 1 mm diodes were measured in pulsed mode with a duty cycle of 0.5% and a pulsed width of 1 ms. A similar threshold (V_{th}) of +5V was observed across all diodes by linear extrapolation. An excellent

on-state current scaling capability of the fully vertical diodes is observed with a total current ranging from 100 mA to 11.6 A at a voltage of 8.5V.

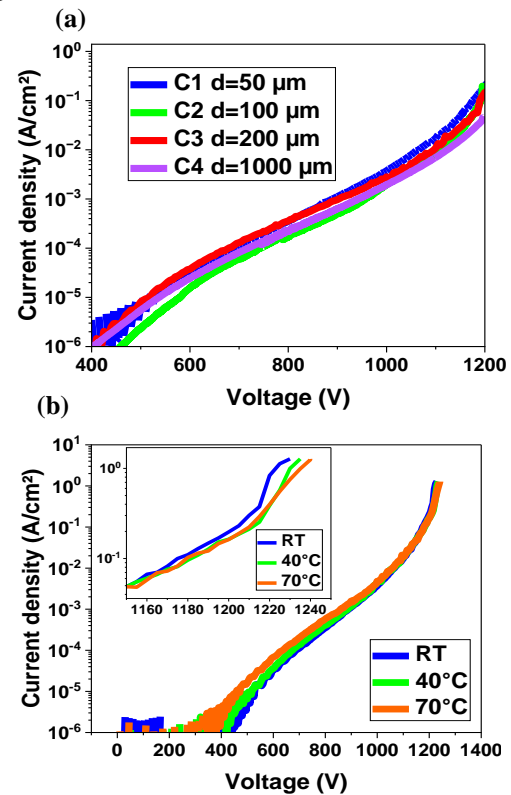


Fig. 5. (a) Reverse characteristics of fully vertical PiN diodes with various anode size (b) Typical reverse characteristics of fully vertical P-i-N diodes at various temperatures for small diodes size ($d < 100$ μm).

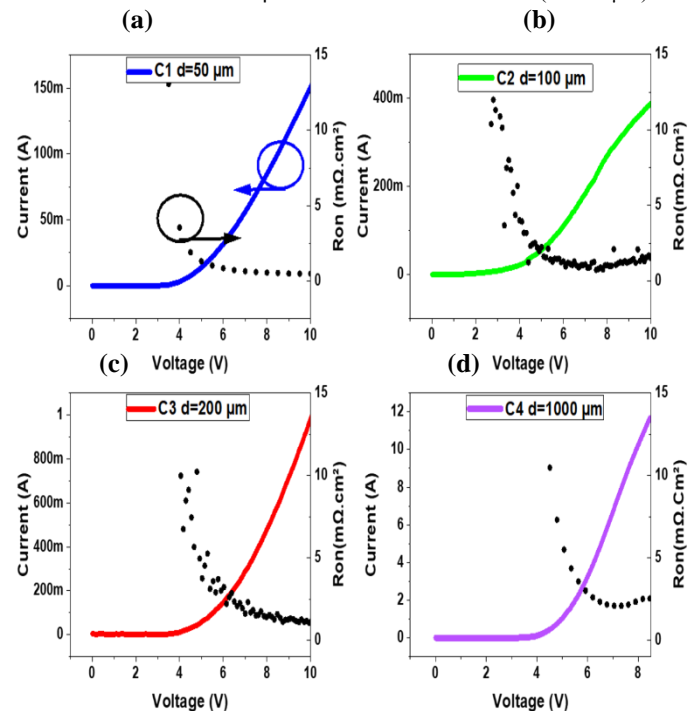


Fig. 6. Forward characteristics of fully vertical P-i-N diodes with various anode sizes (a) C1($d=50$ μm), (b) C2($d=100$ μm), (c) C3($d=200$ μm) and (d) C4 ($d=1000$ μm)

Fig. 7.a shows the $R_{\text{on,sp}}$ and related current density of different anode areas extracted from the I(V) measurements,

which were normalized using the anode area. For a small anode size (diameter = 50 μm), the $R_{on,sp}$ is about 0.48 $\text{m}\Omega\cdot\text{cm}^2$. For larger diode size, a relatively slight degradation of $R_{on,sp}$ and current density was observed. Indeed, the R_{on} increases only by a factor of 3 as compared to the small 50 μm diodes while the anode area is increased by 400%. Since the measurements are performed in pulse mode, the R_{on} degradation is attributed to the thermal dissipation that can be further improved by optimizing the Copper heat sink deposition at the n+ GaN bottom layer interface and the use of proper packaging. Nevertheless, the diodes deliver an unprecedented high on-state current with more than 11.5 A for a 1 mm anode diameter (see Fig. 7.b). This is ascribed to both the optimization of backside N-face ohmic contacts and the implementation of thick copper electroplating replacing the Si substrate as a heat sink. To the best of our knowledge, this is the first demonstration of high current operation (above 10 A) for vertical GaN-based devices on silicon substrates.

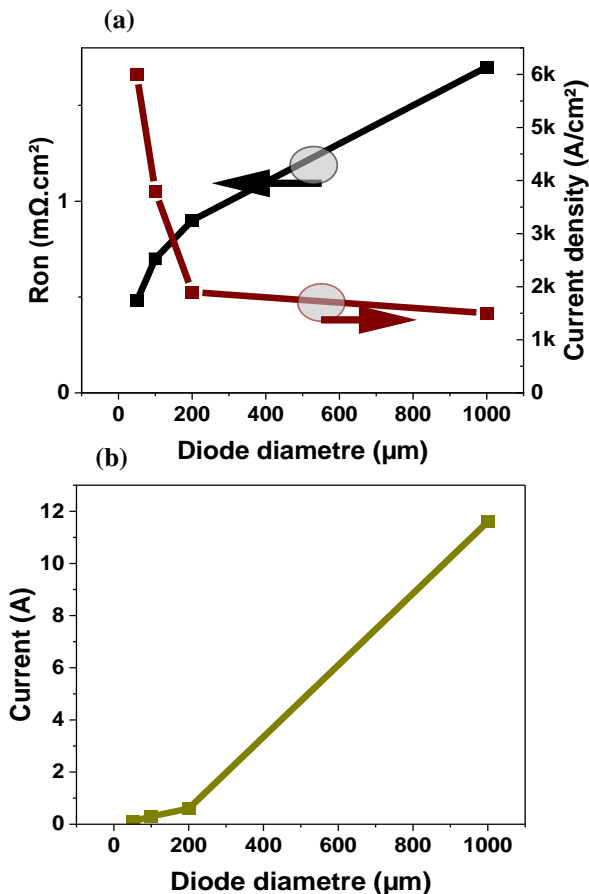


Fig. 7. (a) The extracted R_{on} , on-state current density and (b) Forward current measurement versus diode anode diameter at 8.5 V

Fig. 8 benchmarks the fabricated diodes (up to 100 μm anode size) with reported pseudo and fully vertical GaN-on-foreign substrate from the literature using Baliga figure of merit (BFOM) [7]-[9], [12], [17]-[19], [21], [22], [31]-[39]. The high BFOM of 3.17 GW/cm^2 is superior to the reported vertical GaN P-i-N diodes on foreign substrates. It should be specified that the main drawback for the pseudo vertical architecture is the R_{on} degradation when increasing the anode size due to the current crowding effect. That is why the reported pseudo vertical diodes typically employ small anode sizes to extract the

R_{on} , which results in limited on-state current. To the best of our knowledge, this is the first demonstration of high on-state current > 10 A in fully vertical GaN on Silicon P-i-N diodes offering potentially avalanche soft breakdown up to 1200 V as characterized on small diodes.

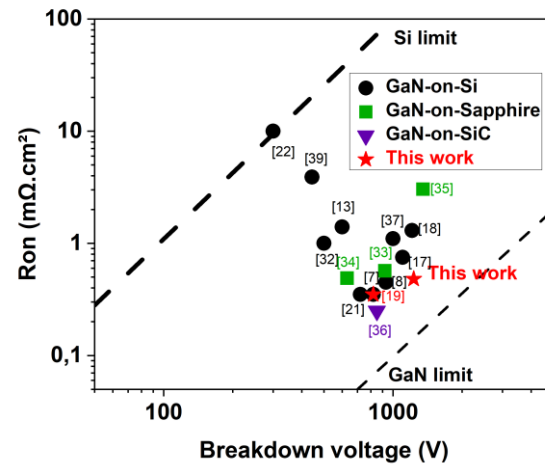


Fig. 8. Benchmark of fully and pseudo-vertical small GaN-on-foreign substrate diodes.

IV. CONCLUSION

This paper demonstrates high quality fully vertical GaN-on-Silicon P-i-N diodes with state-of-the-art BFOM performances (> 3.17 GW/cm^2), achieving 1200 V blocking voltage with avalanche signature, unprecedented on-state current (> 10 A) and low R_{on} . The high performance on large anode sizes results from the high material quality, the polyimide passivation strengthening the membranes and thus enabling both the use of deep mesa etching as edge termination and the implementation of a thick Cu layer as heat sink; as well as an HCl treatment allowing to significantly reduce the backside N face ohmic contact resistances.

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