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Nuraddeen Ado Muhammad

nuraddeen.ado.muhammad@univ-poitiers.fr

Université de Poitiers, Univ. Limoges, CNRS, XLIM

David Cordeau

Université de Poitiers, Univ. Limoges, CNRS, XLIM

Jean-Marie Paillot

Université de Poitiers, Univ. Limoges, CNRS, XLIM

Research Article

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Posted Date: March 18th, 2024

DOI: https://doi.org/10.21203/rs.3.rs-4102730/v1

Additional Declarations: No competing interests reported.

Analysis and design of an innovative 19.5 GHz active phase shifter architecture, implemented in a 0.13 µm BiCMOS SiGe:C process, for beamforming in 5G applications

Nuraddeen Ado Muhammad [1*], David Cordeau [1], Jean-Marie Paillot.[1]
[1] Université de Poitiers, Univ. Limoges, CNRS, XLIM, Angoulême, France

* Corresponding author: Nuraddeen Ado Muhammad (*nuraddeen.ado.muhammad@univ-poitiers.fr*).

Université de Poitiers, CNRS, XLIM, 16000, Angoulême, France

https://orcid.org/my-orcid?orcid=0000-0002-4585-3651

ABSTRACT

This paper presents the design and implementation of a 19.5 GHz active phase shifter for beamforming. The proposed circuit is based on an original architecture using an injection-locked voltage-controlled oscillator (ILVCO) associated with a polyphase filter followed by a phase selection circuit and its sign. From a 1.3 V supply voltage, the proposed circuit was designed to obtain a phase shift range of 360°. This phase shifter is synthesized using the phase selection circuit (PS) for coarse adjustment in the steps of 90° and the injection-locked VCO for a fine-tuning adjustment between ±45°. The circuit consumed a total current of 20.47 mA with a chip size of 1.51 mm^2 including the pads and it is integrated in a BiCMOS SiGe:C 0.13 µm process.

Keywords: Active Phase Shifter, 5G, Injection locked VCO, Phase and Sign Selector, Polyphase filter, Beamforming.

1. Introduction

The 5th Generation cellular system has been standardised and deployed around earlier 2020s [1]. Numerous competencies include, guaranteed low latency, mass connectivity, and ultra-reliability are currently being normalised [2]. Massive machine type communications (mMTC), enhanced mobile broadband (eMBB), and ultra-reliable and low latency communications (uRLLC) are the three major 5G communication possibilities according to 5G NR by 3GPP [3]. The major advantages over 4th Generation wireless communication systems includes, 1 million devices/km^2 connection density, 1 ms end-to-end latency, 20 Gbps peak data rate, 10 Mbps/m^2 area traffic capacity, 0.1 Gbps user-experienced data rate, support for 500 km/h mobility, and 3 times spectrum efficiency. To accomplish the goal of 5G, several key technologies have been proposed, including massive multiple-input multiple-output (MIMO), millimeter wave (mmWave), and ultra-dense network (UDN). As shown in Fig. 1, the three primary bands for 5G spectrum allocation are low, high, and very high. The spectrum at lower frequencies, particularly at 700 MHz allows for wide-area 5G coverage and deep indoor penetration. The spectrum at high frequencies with comparatively large bandwidths below 6 GHz (at 3.4 GHz to 3.8 GHz) offers the required capacity to support many connected devices and guarantee high speed for devices that are connected at the same time. The most optimal balance between capability and coverage is provided by this spectrum. The spectrum above 24 GHz (mmWave) offers extremely high capacity, extremely low latency and ultra-high throughput (for example, 5G NR band n258 which is in the range of 24.25 GHz to 27.5 GHz) with very wide bandwidths [4].

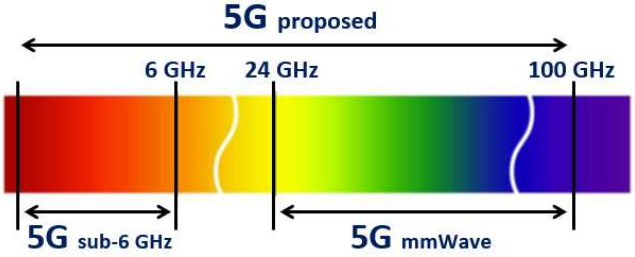

Fig. 1 The 5G Spectrum

The millimeter wave frequenciy band is characterized by an accessible bandwidth that can promote high-speed wireless system for the future radio communications systems, including (5th Generation) cellular systems and beyond. The frequencies of operation at millimeter wave generally require larger antenna aperture to improve the channel budget. These antennas are usually in the form of phased arrays, allowing beamforming to be performed. Beamforming of a phased array is achieved by applying phase-shifted RF signals to each element of the array to steer the beam in the desired direction while providing zeros in the directions of the interfering signals. [5]. Thus, RF phase shifters are in high demand because they are widely used in applications such as phased antenna arrays, smart antennas, and MIMO systems. They are therefore key functions in phased array antenna systems that provide flexible beam steering by allowing altering the phase of each antenna element. As presented in the literature, there are different types of phase shifters which are classified as active or passive, with either analog or digital set-up. Examples of these phase shifters currently in use are line-load, reflection-type, vector-sum and line-switch [6]–[9]. Active phase shifters (APS) provide a very high degree of integration, smaller amplitude variations and no insertion losses but they need high power consumption in comparison to the passive phase shifters (PPS).

In this context, in order to address and suggest some possible solutions to the challenges associated with active phase shifters that includes linearity, phase error, complexity and resolution, some existing active phase shifters for beamforming of an antenna array are reviewed. To obtain a phase shift that is linear over a range of ± 45° and that can cover the entire 360° phase plane, an original architecture based on an injection-locked oscillator associated to an IQ modulator is proposed by [5]. This phase shifter covers a 360° phase plane by steps of 90° for each combination of the digital command I and Q but at the expense of a highe power consumption . Also, [10] presents a design of a broadband Vector Modulator (VM) with coupler-based phase generation. The proposed phase shifter's fundamental working premise is the superimposition of two weighted signals with a phase difference of ±90°. It contributes to a gain, and it is implemented as a traditional cascode with reactive matching but this phase shifter circuit suffers from complexity. The work presented by [11], [12] and [13] presents high resolution and linearity performances but at the expense of complexity, power consumption and die area. Among the prevalent APSs techniques, injection-locked oscillators arrays (ILOAs) are among the most frequently used techniques. In this approach, an external injection signal locked the oscillators which can be controlled independently by altering their free-running frequencies. Between the oscillators' outputs and the injected signal, a phase difference is created. Unfortunately, the obtained phase shift versus the difference between the frequency of the injection signal and the free-running frequency is non-linear and constitute a significant disadvantage of an injection-locked oscillator [5]. Thankfully, the phase shift is roughly linear in the range ±45°.

In this contest, in order to minimise some of the drawbacks associated with these phase shifters, this paper aims at showing the feasibility of designing an original and efficient architecture of an active phase shifter at 19.5 GHz that can meet the constraints imposed by the new 5G standard. The design of a novel architecture of an active phase shifter is based on an injection-locked oscillator followed by a polyphase filter in association with phase and sign selectors. The phase shifter is going to perform a linear, fine tuning phase shift in a range of ± 45° by tuning the control voltage of an ILVCO and to equally cover the entire 360° phase plane with the help of control signals S_0 and S_2 of a phase selector and its sign for coarse tuning. This active phase shifter will be placed in the LO path of a phased antenna array for beamforming. It has been designed and implemented in a BiCMOS SiGe:C 0.13 µm process.

The paper is organized as follows. In section 2, the architecture of 5G phased array receiver and frequency plan is presented. Section 3 detailed the proposed active phase shifter circuit followed by the main building blocks design. The implementation and the post-layout simulation results are presented in section 4. Finally, the paper is concluded in section 5.

2. 26 GHz Phased array receiver architecture

The three primary bands for 5G spectrum allocation are low frequency (700 MHz), high frequency (below 6 GHz (at 3.4 GHz - 3.8 GHz)), and very high frequencies above 24 GHz (24.25 GHz - 27.5 GHz, referred to as "26 GHz" and known as the 5G NR band n258) [4]. Hence, the block-diagram schematic of a 26 GHz phased-array receiver using an LO phase shifting technique could be the one presented in Fig. 2.

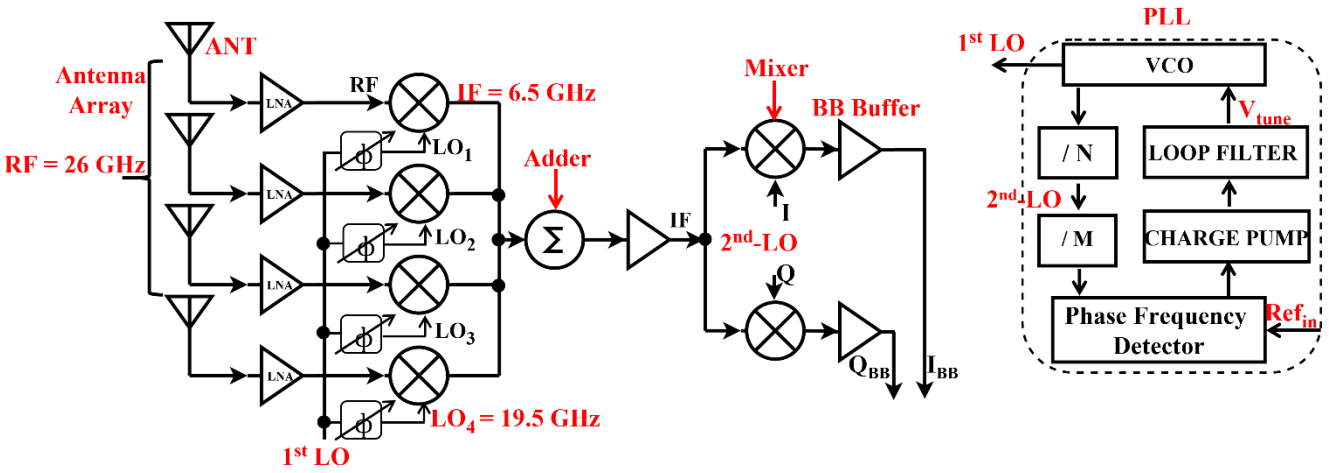

Fig. 2 Architecture of a 5G Phased array receiver

As can be observed on Fig. 2 , the phased-array receiver consisting of four paths uses a two-step down-conversion architecture with an intermediate frequency (IF) of 6.5 GHz for two main reasons. First, a heterodyne-type receiver delivers greater selectivity and gain control at numerous stages than a single down-conversion system such as homodyne [14]. Secondly, by using a proper frequency planning, both LO frequencies can be generated in a single synthesizer loop using a dedicated frequency divider (/N), as illustrated in the right part of Fig. 2. Indeed, let us consider the following frequency plan:

The RF frequency is given by:

$$F_{RF} - F_{LO} = F_{IF} \tag{1}$$

To obtain a direct baseband down conversion then:

$$F_{RF} = F_{IF} + F_{LO} \tag{2}$$

These two LO frequencies have to be synchronous, in these conditions, the signal at F_{LO2} is provided by the same PLL with a multiplication ratio *N* then:

$$F_{LO2} = \frac{F_{LO1}}{N} \tag{3}$$

Hence:

$$F_{LO1} = \left(\frac{F_{RF}}{1 + \frac{1}{N}} \right) \tag{4}$$

If N = 3, then $F_{LO1} = \frac{26\ GHz}{1.33}$ = 19.5 GHz (i,e working frequency of the proposed active phase shifter) and:

$$F_{IF} = F_{RF} - F_{LO1} \quad (5)$$

$$= 6.5\ GHz \quad (6)$$

Therefore, the image frequency is 19.5 – 6.5 = 13 GHz which can be naturally rejected by the antenna and the LNA.

3. Proposed active phase shifter design

Fig. 3 shows the architecture of a 5G NR Band n258 phased array receiver with the proposed active phase shifter implemented in the LO path as well as its constituting blocks.

As can be seen on this figure, the proposed active phase shifter uses an injection-locked VCO associated with a polyphase filter and a phase selection circuit and its sign in order to cover a continuous phase shift range of 360°. At first, the RF balun splits the injected input signal into two differential signals. Thus, the injection-locked VCO will allow to vary the phase shift in a linear form between -45° and +45°. On the other hand, to allow a step adjustment of the phase shift, an I/Q signal is generated from a polyphase filter and we select the desired quadrant thanks to the phase selection circuit and its sign.

Thus, all the phases generated by the polyphase filter are accessible by switching the phase and sign selector respectively using the control signals S_0 and S_2. The differential signal is then amplified and converted into a single-ended one using a differential amplifier, while a buffer stage using an emitter follower architecture is used at the output for 50 Ω impedance matching.

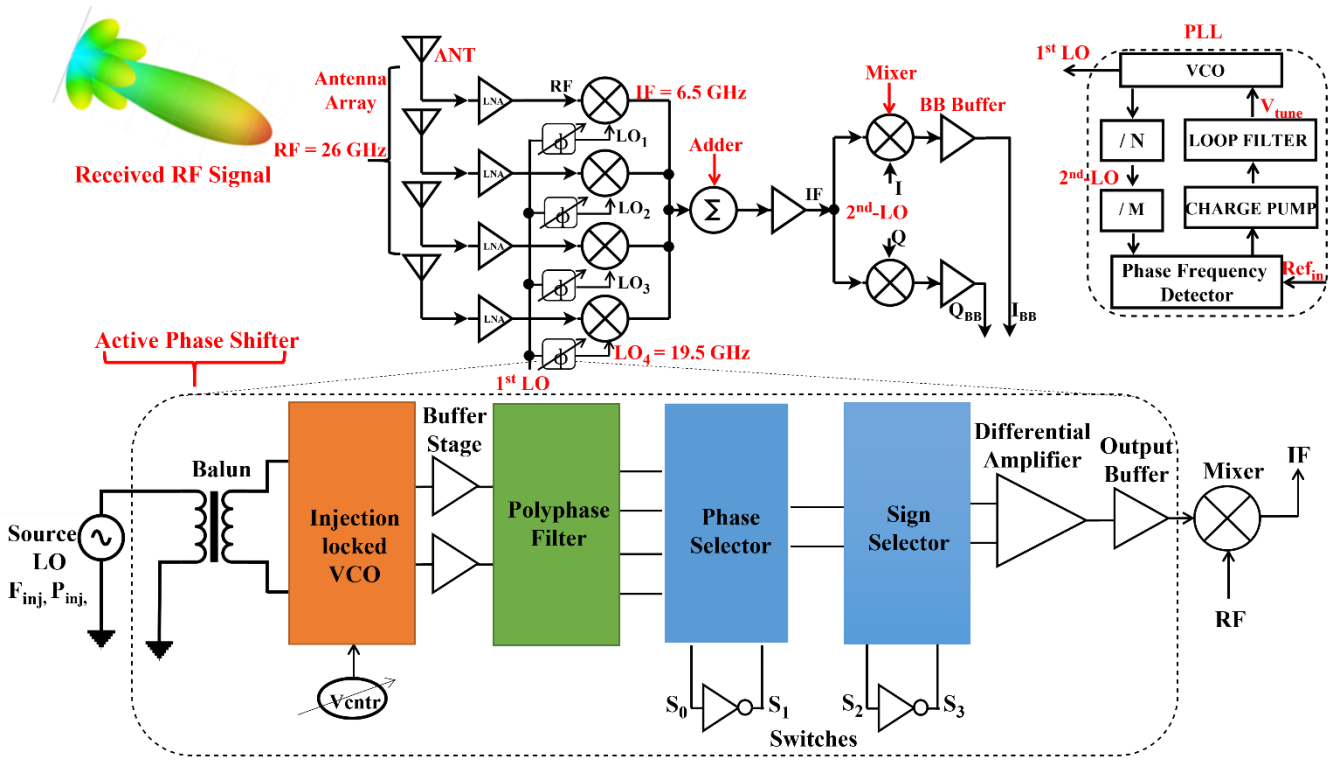

Fig. 3 Phased array receiver block diagram including the proposed building blocks of the active phase shifter

3.1. Input balun and matching network

As shown in Fig. 4, the lattice balun topology is a common lumped-element circuit used for designing small-size narrow-band baluns [15]. It is a combination of a high-pass and a low-pass filters that allows the single-ended input signal to be converted into a differential output signal. The circuit topology is also well suited for impedance matching.

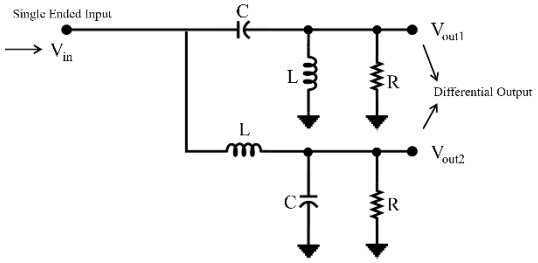

Fig. 4 Schematic of the loaded lattice balun

Let us write the transfer function in respect of output 1 which is given as follows:

$$\underline{H_1} = \frac{\underline{V_{out1}}}{\underline{V_{in}}} = \frac{1}{1 + j\omega L\left(\frac{1}{R} + j\omega C\right)} = \frac{1}{1 + 2j\xi\frac{\omega}{\omega_0} - \frac{\omega^2}{\omega_0^2}} \tag{7}$$

Where ω_0 is the natural pulsation, while ξ is the damping factor.

Which is the transfer function of a second order low pass filter (LPF) with $\omega_0^2 = \frac{1}{LC}$ and $\xi = \frac{L\omega_0}{2R}$

Hence, at a pulsation $\omega = \omega_0$:

$$\underline{H_1} = \frac{1}{2j\xi} = \frac{-jR}{L\omega_0} \tag{8}$$

As a consequence:

$$Arg\left(\underline{H_1}\right) = \emptyset_{Vout1} - \emptyset_{Vin} = \frac{-\pi}{2} rad \tag{9}$$

Also, the transfer function in respect of output 2 is given as follows:

$$\underline{H_2} = \frac{\underline{V_{out2}}}{\underline{V_{in}}}\frac{-LC\omega^2}{1 + j\frac{L\omega}{R} - LC\omega^2} = \frac{-\left(\frac{\omega^2}{\omega_0^2}\right)}{1 + 2j\xi\frac{\omega}{\omega_0} - \frac{\omega^2}{\omega_0^2}} \tag{10}$$

Which is the transfer function of a second order high pass filter (HPF)

At $\omega = \omega_0$:

$$\underline{H_2} = \frac{j}{2\xi} = \frac{jR}{L\omega_0} \tag{11}$$

And

$$Arg\left(\underline{H_2}\right) = \emptyset_{Vout2} - \emptyset_{Vin} = \frac{+\pi}{2} rad \tag{12}$$

And the difference between the phases is given as:

$$Arg\left(\underline{H_2}\right) - Arg\left(\underline{H_1}\right) = \emptyset_{Vout2} - \emptyset_{Vin} - (\emptyset_{Vout1} - \emptyset_{Vin}) \tag{13}$$

$$= \emptyset_{Vout2} - \emptyset_{Vout1} = \frac{+\pi}{2} - \left(\frac{-\pi}{2}\right) = \pi\ rad\ or\ 180^0 \tag{14}$$

Hence, this circuit can be used as a narrowband balun at $\omega = \omega_0$.

This circuit can also play the role of an impedance matching network as we explain below and from Fig. 5 where we split the lattice balun into two separated LPF and HPF filters.

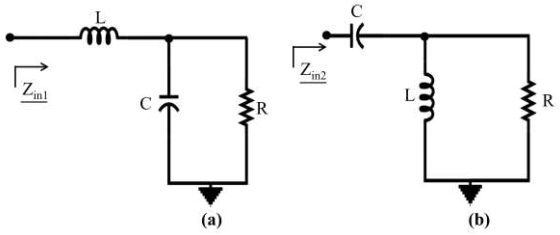

Fig. 5 Two separated LPF (a) and HPF (b) filters allowing the input impedance calculation

From Fig. 5 (a), we can write:

$$\underline{Z_{in1}} = \frac{R.\underline{Z_C}}{R + \underline{Z_C}} + \underline{Z_L} \tag{15}$$

Let us now write $L\omega_0 = \frac{1}{C\omega_0} = X$, the reactive part at ω_0

Then at $\omega = \omega_0$, we have:

$$\underline{Z_C} = -jX\ and\ \underline{Z_L} = jX \tag{16}$$

That is:

$$\underline{Z_{in1}} = \frac{-RjX}{R - jX} + jX = \frac{X^2}{R - jX} \tag{17}$$

In the same way, from Fig. 5 (b), we can write:

$$\underline{Z_{in2}} = \frac{R.\underline{Z_L}}{R + \underline{Z_L}} + \underline{Z_C} = \frac{RjX}{R + jX} - \text{JX} \tag{18}$$

Hence, we have:

$$\underline{Z_{in2}} = \frac{X^2}{R + jX} \tag{19}$$

Let us now combine Fig. 5 (a) and (b) to form the impedance matching network as presented in Fig. 6.

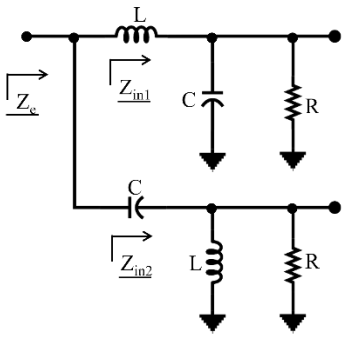

Fig. 6 Lattice balun as an impedance matching network

Then we can write the input impedance as:

$$\underline{Z_e} = \underline{Z_{in1}} \Big\| \underline{Z_{in2}} = \frac{\underline{Z_{in1}}.\underline{Z_{in2}}}{\underline{Z_{in1}} + \underline{Z_{in2}}} \tag{20}$$

Hence:

$$\underline{Z_e} = \frac{\frac{X^2}{R - jX}.\frac{X^2}{R + jX}}{\frac{X^2}{R - jX} + \frac{X^2}{R + jX}} \tag{21}$$

That is

$$\underline{Z_e} = \frac{X^4}{X^2(R + jX + R - jX)} = \frac{X^2}{2R} \tag{22}$$

Leading to:

$$X = \sqrt{2R.\underline{Z_e}} \tag{23}$$

Hence, for a given resistive load R, L and C can be calculated for the desired input impedance $\underline{Z_e}$ using the following equations:

$$L = \frac{X}{2\pi f_0} \; and \; C = \frac{1}{2\pi f_0 X} \tag{24}$$

Unfortunately, most of the time, the impedance presented by active components is complex and can be written as $\underline{Z} = R - jY$. Then:

$$\underline{Z_e} = \frac{X^2}{2(R - jY)} = \frac{X^2(2R + 2jY)}{4R^2 + 4Y^2} \tag{25}$$

Hence:

$$R_e(\underline{Z_e}) = \frac{X^2 R}{2(R^2 + Y^2)} \tag{26}$$

And:

$$I_m(\underline{Z_e}) = \frac{X^2 Y}{2(R^2 + Y^2)} \tag{27}$$

From (26), we can express X as follows for $R_e(\underline{Z_e}) = 50\ \Omega$:

$$X = \sqrt{\frac{100(R^2 + Y^2)}{R}} \tag{28}$$

Hence the values of L and C can be again calculated by using (24).

Furthermore, since $I_m(\underline{Z_e}) > 0$, the imaginary part of $\underline{Z_e}$ in Fig. 6 can be cancelled by using a simple capacitor in series to the circuit as shown in Fig. 7.

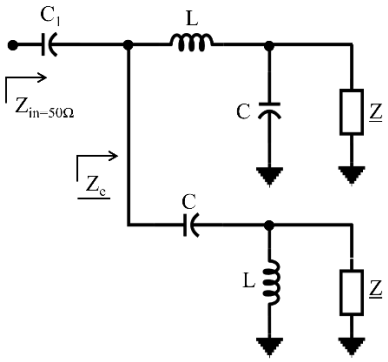

Fig. 7 Schematic of the complete impedance matching network

As a consequence:

$$\underline{Z_{in}} = \underline{Z_e} - \frac{j}{C_1 \omega_0} \tag{29}$$

Then, if the desired input impedance is 50 Ω, we have:

$$\underline{Z_{in}} = 50 + j\frac{X^2 Y}{2(R^2 + Y^2)} - \frac{j}{C_1 \omega_0} \tag{30}$$

Thus

$$C_1 = \frac{2(R^2 + Y^2)}{X^2 Y . \omega_0} \tag{31}$$

Hence, Fig. 8 shows the design of the proposed input balun with a matching network that converts the unbalanced single-ended input to a balanced differential output. The values of the components involved are calculated from the load impedance

presented at the input of the ILVCO which is equal to the value presented in equation (32) at 21.76 GHz and with the previous equations. The values of the inductor (L_B), and capacitors (C_B, C_1) are calculated from the equations (24) and (31) which are found to be 961 pH, 55.6 fF and 186 fF respectively. However, due to the non-idealistic behaviour of these components, an optimization has been performed and leads to new values i.e. 720 pH, 92 fF and 165 fF with a quality factor of 23.95, 77.62 and 42.38 respectively. In this case, the balun is optimised in order to operate at a frequency of 21.76 GHz. These values are chosen with a sufficient margin so that when the parasitic components from the layout are extracted, the balun will be expected to have optimum performances at the desired frequency of 19.5 GHz.

$$\underline{Z} = 106.84 - j * 83.95 \tag{32}$$

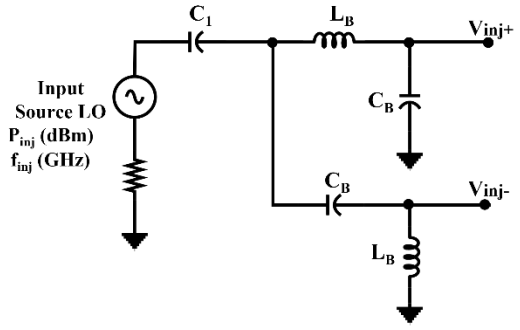

Fig. 8 Schematic of the input balun and matching network

3.2. Injection-locked VCO

The principle of injection is based on the situation whereby an oscillator is disturbed by an external signal of frequency f_{inj} close to its free-running oscillation frequency f_0 . Then, under certain conditions, it can lock on f_{inj}. Therefore, a phase shift $\Delta\phi$ is created between the injection signal and the output signal of the injection-locked oscillator. This phase shift may be varied by controlling the oscillators' free-running frequency f_0 via the control voltage V_{cntr} as shown in Fig. 9 below.

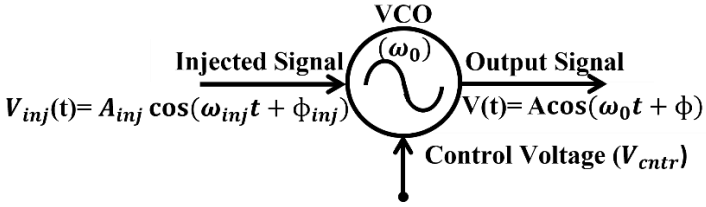

Fig. 9 Injection-locked Oscillator (ILO)

The oscillator under injection has a behaviour that has been extensively studied using various procedures in the literature. The first theory has been developed by Adler [16] for weak injection levels and then it was taken up by Paciorek [17], Kurokawa [18] and Razavi [19] for high levels of injection.

A new theoretical model of the injection phenomenon based on the theory developed in [20] and [21] is presented in [5]. For this purpose, let us consider a Van der Pol oscillator, used to model an LC oscillator, under a current injection I_{inj}, as shown in Fig. 10. In these conditions, the active part is modeled by the negative conductance -G_d (A) in parallel with an LC resonant circuit. G_L is the conductance representing the resistive part of the resonator.

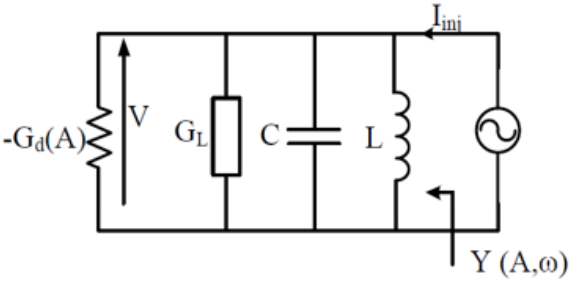

Fig. 10 Van der Pol oscillator under injection

Hence, it is shown in [5] that the behaviour of this system is governed by the following equation:

$$\omega_{inj} = \omega_0 + \frac{\omega_a . I_{inj}}{A G_L} sin\ (\phi_{inj} - \phi) \tag{33}$$

With ϕ and ϕ_{inj} respectively the phase of the oscillator output signal and the phase of the injected signal, while A and ω_a represent the amplitude of the output voltage of the oscillator and the bandwidth of the resonator, respectively.
Furthermore, (33) can be rewritten as follows:

$$\omega_{inj} = \omega_0 + \frac{\omega_0}{2Q} \frac{R_L . I_{inj}}{A} sin\ (\phi_{inj} - \phi) \tag{34}$$

Where $Q = \frac{\omega_0}{2\omega_a}$ is the resonator quality factor and $R_L = \frac{1}{G_L}$

For each oscillator, a locking range $\pm \Delta\omega_L = \omega_{inj} \pm \omega_{0,max}$ is defined which represents the maximum frequency difference between the injection frequency and the free-running oscillation frequency. In other words, when the free-running oscillation frequency is within the locking range, the oscillator locks to the frequency of the injected signal otherwise it is not able to lock. Thus, from equation (34), we deduce the one-sided locking range $\Delta\omega_L$, in the case of low injection levels ($R_L . I_{inj} \ll A$):

$$\Delta\omega_L = \frac{\omega_0}{2Q} \frac{R_L . I_{inj}}{A} \tag{35}$$

Equation (35) shows that this locking range is directly proportional to the injection strength ($R_L . \frac{I_{inj}}{A}$) and inversely proportional to the resonator quality factor. Thus, when the free-running oscillation frequency f_0 is within the locking range, the oscillator locks to f_{inj} and a phase shift $\Delta\phi = \phi_{inj} - \phi$ is obtained. This phase shift, given by the equation below, is controlled by changing the free-running frequency f_0 through V_{cntr} (see Fig. 9).

$$\Delta\phi = \phi_{inj} - \phi = sin^{-1}\left(\frac{\omega_{inj} - \omega_0}{\Delta\omega_L}\right) \tag{36}$$

As shown in equation (36), the phase shift $\Delta\phi$ varies in the ±90° range when the free-running frequency varies in the $\pm \Delta\omega L$ locking range.
Equation (34) was generalized in [22] regardless of the level of the injection strength. Thus, we obtain:

$$\omega_{inj} - \omega_0 = \frac{\omega_0}{2Q} \frac{I_{inj}}{I_{osc}} \frac{\sin\ (\phi_{inj} - \phi)}{1 + \frac{I_{inj}}{I_{osc}} \cos\ (\phi_{inj} - \phi)} \tag{37}$$

With I_{inj}, the amplitude of the injection current and I_{osc} the amplitude of the oscillator current when there is no injection, as explained in [19] and [22].

The locking range in this case is determined by looking for the maximum of the function (37) with respect to the variable $\Delta\phi = \phi_{inj} - \phi$. Thus, the locking range is given by the following relationship [17], [22]:

$$\Delta\omega_L = \frac{\omega_0}{2Q} \frac{I_{inj}}{I_{osc}} \frac{1}{\sqrt{1 - \left(\frac{I_{inj}}{I_{osc}}\right)^2}} \tag{38}$$

Therefore, a larger locking range is obtained when the injection strength is high compared to the case corresponding to a weak injection. In this case, the $\Delta\phi_{max}$ depends only on the value of the injection strength $k = I_{inj}/I_{osc}$ and thus it can exceed ± 90° and reach (180°- $cos^{-1}(k)$) [13], [11].

As stated in [11], increasing the injection strength allows for the achievement of a larger locking range and better phase linearity and resolution between ± 90°. However, the variation of the locking range as a function of the injection strength becomes nonlinear for high values of the injected signal compared to low injection levels, as shown in equations (35) and (38). Furthermore, the larger the locking range the faster the oscillator locks [23], [24]. Thus, all of these findings must be taken into account when designing an injection-locked oscillator.

The theoretical phase shift Δϕ is plotted as a function of ω_0 in Fig. 11 using equation (37). From this figure, one can notice the linearity of the phase shift in the range [- 45°, + 45°] and its strong nonlinearity at the ends of the locking range. Therefore, as it stands, the design of an automatically adjustable phase shifter for phase shift values between ± 90° is complicated. Furthermore, limiting the range of linear variation (±45°) will reduce the efficiency of the beamforming system. In this respect, an architecture based on an ILO associated with an injection-locked frequency tripler is proposed in [25]. This technique allows to obtain a continuous and linear phase shift in the whole phase plane but at the expense of the complexity of implementation of the frequency tripler for which a limiter stage is necessary. Another method, based on a triple push ILVCO, was developed by [26] to control the elements of the antenna array linearly throughout the 360° phase plane but the system suffers from complexity and high-power consumption limitations which leads to further research. As a consequence, we propose here an active phase shifter in the millimeter wave band to address the challenges encountered by the previously presented active phase shifters.

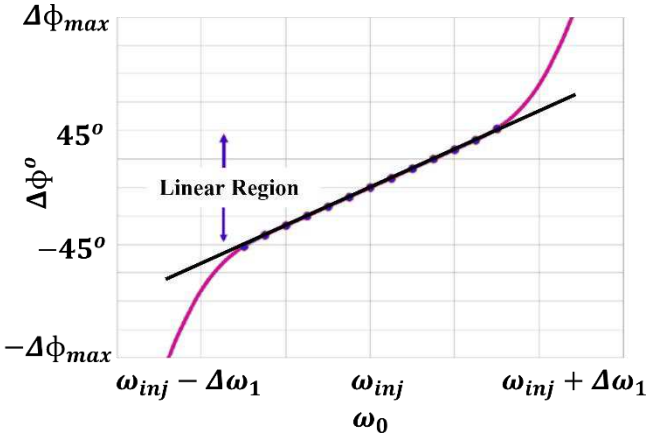

Fig. 11 Phase shift characteristic curve

The architecture of the injection-locked LC oscillator is shown in Fig. 12. It is one of the essential elements of the proposed active phase shifter. In the context of our design, the topology chosen for this elementary circuit is based on a differential LC-VCO structure. The LC resonator used consists of a symmetric center tapped inductor in parallel with two single-ended varactor diodes biased by a control voltage V_{cntr}. The value of the differential inductance is chosen equal to 351 pH and the quality factor has been evaluated in simulation using equation (39) below and found to be 30.15 at 19.5 GHz.

$$Q_{diff} = \frac{im(Z_{11}+Z_{22}-Z_{12}-Z_{21})}{Re(Z_{11}+Z_{22}-Z_{12}-Z_{21})} \tag{39}$$

Two NMOS transistors M_1 and M_2, which are identical, constitute the active part of the differential LC VCO. These two NMOS transistors present a negative conductance of $\frac{-gm}{2}$. In order to meet the oscillation start-up requirements, the size of the NMOS transistors (M_1, M_2) is defined for a provided bias current.

The expression for a given simple cross-coupled pair architecture is provided in equation (40) below as:

$$|g_{neg}| > \frac{1}{R_p} \tag{40}$$

With:

$$g_{neg} = -\frac{g_m}{2} \tag{41}$$

R_P is the loss resistance of the resonator and g_m is the transconductance of the transistor.

The size of the transistors is chosen so that gm is at least two times greater than $2/R_P$ in order to meet the start-up condition of the VCO. Thus, for a bias current equal to 3 mA, the width of the two NMOS transistors of the cross-coupled differential pair is fixed at 15 µm. The length of the NMOS transistors is fixed to the minimum offered by the Bicmos9mw process (L= 0.13 µm).

The injection current is provided by the differential pair $M_{3,4}$. A high injection strength has been selected to be ($I_{inj}/I_{osc} = 0.5$) to ensure a large locking range and eventually a better linearity and phase symmetry in the range of ± 45° [5], [22]. As a result, the NMOS transistors M_3 and M_4 in the injection circuit are designed with a size of 7.5 µm/ 0.13 µm, and a bias current $I_{inj} = 0.75\ mA$. At the frequency of 19.5 GHz, the injected signal power at the phase shifter's input is equal to -8.5 dBm. Thus, synchronisation occurs and a phase shift between V_{inj+}/V_{inj-} and V_{out1}/V_{out2} is created when the free-running frequency is in the locking range.

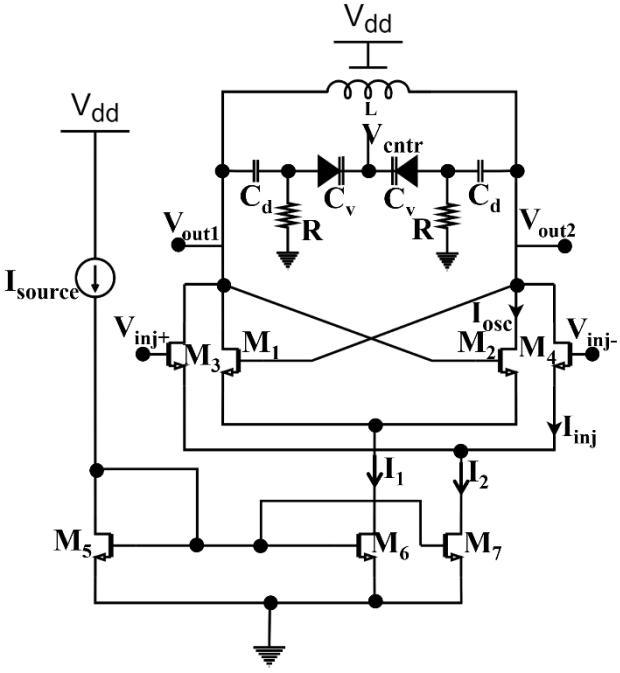

Fig. 12 Schematic of the injection-locked VCO

3.3. The polyphase filter

The RC-CR polyphase filter is made of a low-pass filter and a high-pass filter with differential inputs (Fig. 13). It provides four signals in phase and quadrature at its outputs. Thus, a phase difference of 90° is obtained between the four outputs (V_{I+}, V_{Q+}, V_{I-}, V_{Q-}) over a wide frequency band while the amplitude of the outputs is equal at the pulsation ω=1/RC [27]. In this case, the values of C and R were selected to be 30 fF and 252 Ω respectively. Nevertheless, due to process changes, any difference in the values of C and R can modify the frequency at which the amplitudes are equal. An additional issue is that the input signal's harmonic components are also shifted by ±90°, causing gain and phase imbalance. To be able to decrease the phase error, the harmonic's effect of the input signal should as well be decreased. The transfer function between V_I and V_{in} is:

$$H_I(\omega) = \frac{V_I}{V_{in}} = \frac{1}{1 + j\omega RC} \tag{42}$$

Similarly, the transfer function between V_Q and V_{in} is equal to:

$$H_Q(\omega) = \frac{V_Q}{V_{in}} = \frac{j\omega RC}{1 + j\omega RC} \tag{43}$$

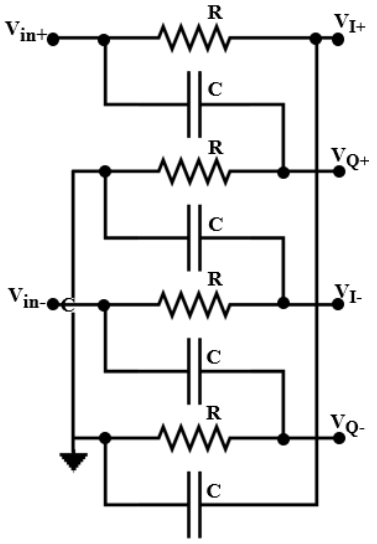

Fig. 13 Schematic of the polyphase filter

3.4. The phase and sign selector

The phase selection circuit is derived from a MOS cascode differential amplifier configuration as depicted in Fig. 14, which is one of the popular building blocks of IC. The choice of this selection circuit is justified by the fact that the voltage gain is much higher than a classical differential pair and it has a better frequency response [28].

As illustrated in Fig. 14, two cascode differential pairs are used to accommodate the four path quadrature signals (V_{I+}, V_{I-}, V_{Q+} and V_{Q-}) from the outputs of the polyphase filter and to select two of them with respect to digital command signals (S_0 and S_1). The phase selector is formed by two pairs of NMOS cascode differential pairs (M_8 - M_{15}) to select the two phases from the outputs of the polyphase filter. The sizes of transistors $M_{8\text{-}15}$ are chosen to be (W/L) = 20 µm/0.13 µm and the tail current source, which is a simple NMOS current mirror (M_{18}, M_{19} and M_{20}), draws 3 mA from I_{ps}. The lower NMOS transistors (M_{16}, M_{17}) act as a control switch according to the command signals S_0 and S_1, which leads to the selection of one part of the phase selector ON while keeping the other part OFF. A CMOS inverter is employed to command the switching transistors and thus the two differential pairs in opposite polarity (right part of Fig. 14 and Fig. 15). A shared load inductor of 1.06 nH is used for the phase and sign selectors to ensure a sufficient voltage headroom.

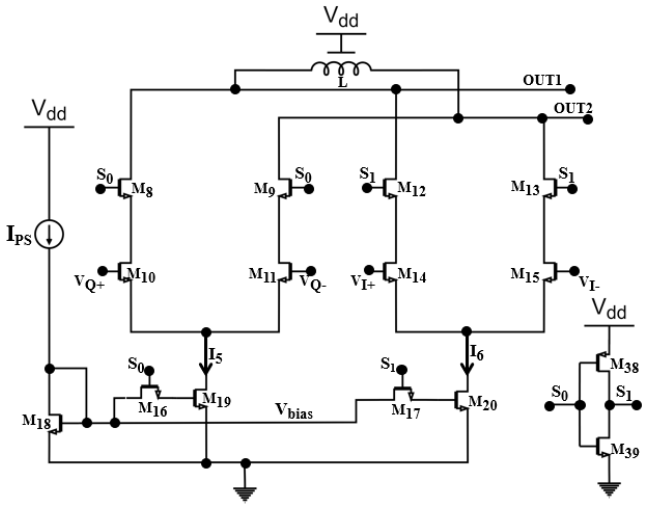

Fig. 14 Schematic of the phase selector

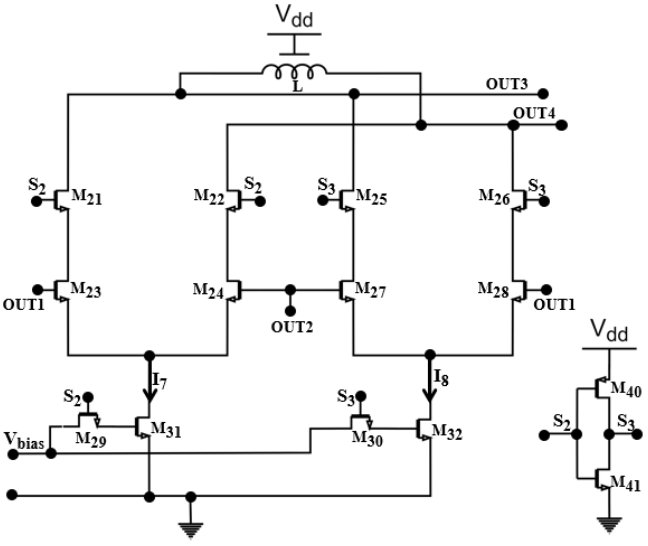

Fig. 15 Schematic of the sign selector

3.5. Differential amplifier and output buffer

The output stage is a combination of a differential to single-ended amplifier and a buffer as shown in Fig. 16. The differential amplifier converts the differential signal to a single-ended one, while the buffer enables 50 Ω output matching. The differential amplifier is made up of a pair of bipolar transistors (B_4 and B_5) that have dimensions of 1 μm emitter length and a load resistor (R) of 500 Ω, while the degeneration resistor (R_{deg}) value is 220 Ω. The current source provides the bias current I_{Ampl} which is equivalent to 850 μA to bias the differential amplifier and the buffer. The differential amplifier's single-ended output signal stimulates the buffer in a common collector architecture (right part side of Fig. 16). The input impedance of the buffer is high, and the output impedance is low which makes the buffer to ensure impedance matching on 50 Ω load. The choice of BJT transistors is justified considering the frequency response and the sufficient power needed at the output of the active phase shifter. The buffer is designed with a bipolar transistor (B_6) with an emitter length of 3 μm and it is connected at the output of the differential amplifier.

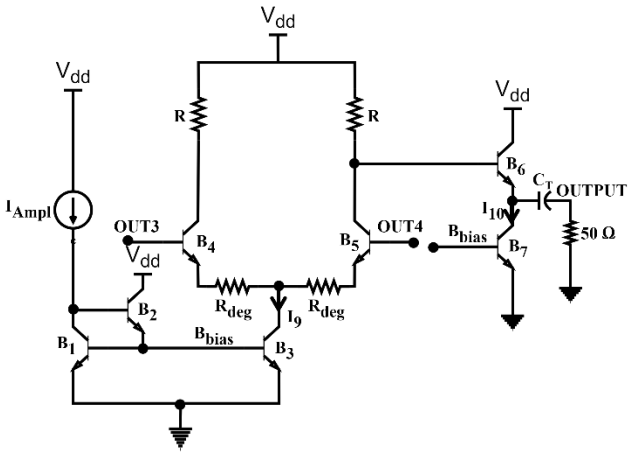

Fig. 16 Schematic of the differential amplifier and output buffer

4. PHASE SHIFTER IMPLEMENTATION AND POST LAYOUT SIMULATION RESULTS

The proposed active phase shifter is designed to operate at a frequency of 19.5 GHz and implemented in the BiCMOS SiGe:C 0.13 µm process of ST Microelectronics. The layout of the circuit is shown in Fig. 17 and has an area of 1.310*1.150 mm^2 including all the pads. To avoid IQ imbalance, the metallization level and the polyphase filter layout design symmetry were carefully considered. Furthermore, additional design strategies were applied to limit sensitivity from process gradient and therefore eliminate mismatch of the components. The procedure for extraction is performed with PVS tool and it is used to estimate and take into account layout parasitic components. The phase and gain consistency of the V_I and V_Q signals guaranteed a high level of quadrature accuracy at the output of the coarse tuning part.

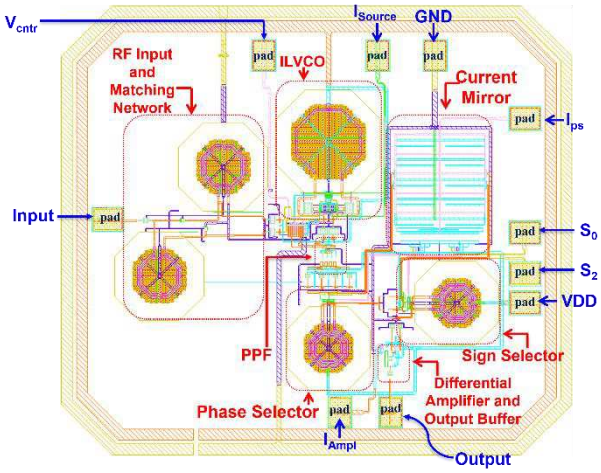

Fig. 17 Active phase shifter layout

The post-layout Simulation results obtained with Cadence Spectre RF shows that the free-running oscillation frequency f_0 of the VCO varies from [17.87 GHz - 20.16 GHz] for a $\boldsymbol{V_{cntr}}$ range of 0 to 2.5 V, as shown in Fig. 18.

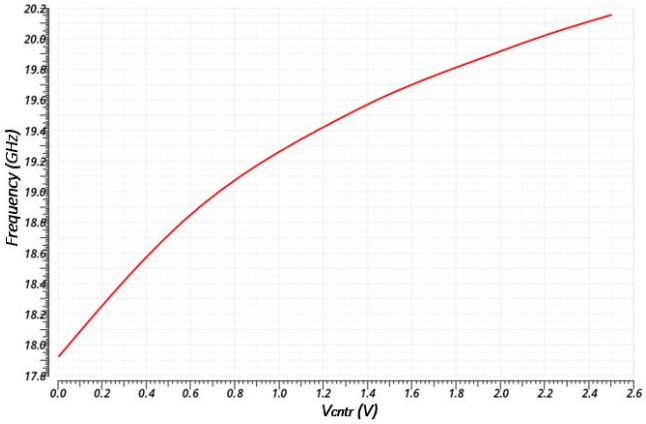

Fig. 18 Variations of the free-running oscillation frequency f_0 as a function of the control voltage $\boldsymbol{V_{cntr}}$

Thus, by applying an injected signal at the input with a power P_{inj} = -8.5 dBm and a frequency f_{inj} = 19.5 GHz, a phase shift Δϕ is obtained by changing the oscillation frequency f_0 of the injection-locked VCO via the control voltage V_{cntr}. A variation of ± 500 MHz around f_{inj} thus allows to obtain a phase shift varying linearly from -45° to +45° for each combination of S_0 and S_2. Fig. 19 illustrates the variation of the phase shift obtained for "S_0S_2 = 00". The linearity error of the phase shift around ± 45° is less than 3°, while around ± 55° it is less than 7°.

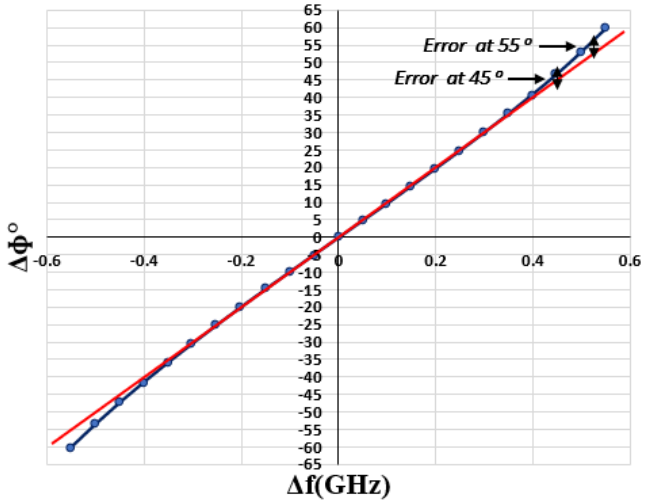

Fig. 19 Phase shift variation as a function of $\boldsymbol{\Delta f} = (\boldsymbol{f_0} - \boldsymbol{f_{inj}})$ for "S_0S_2 = 00"

By switching the control signals (S_0, S_2) between 0 V and 1.3 V, a continuous control of the phase shift over 360° is obtained, as shown in Fig. 20 and Table 1 below. Indeed, for (S_0S_2=00) combination, the Δϕ can be continually controlled between about [-53° to +53°]. An overlap between two adjacent quadrants ensures a continuity of the Δϕ between the four switching combinations.

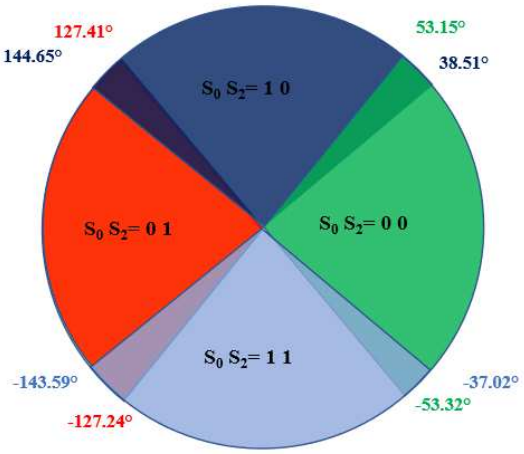

Fig. 20 Proposed active phase shifter phase diagram

Table 1 Variation of the phase shift for different combinations of S_0S_2

V_{cntr} (V)	1,0	1,5	2,0
S_0 S_2 = 0 0 (Δϕ°)	-53.32	0	53.15
S_0 S_2 = 0 1 (Δϕ°)	127.41	-180.61	-127.24
S_0 S_2 = 1 0 (Δϕ°)	38.51	90.70	144.65
S_0 S_2 = 1 1 (Δϕ°)	-143.59	-89.75	-37.02

Fig. 21 shows the waveforms of the output signal for two adjacent combinations (S_0, S_2) and for the same control voltage $V_{cntr} = 1.5\ V$. The phase difference obtained between these two cases is around 90°.

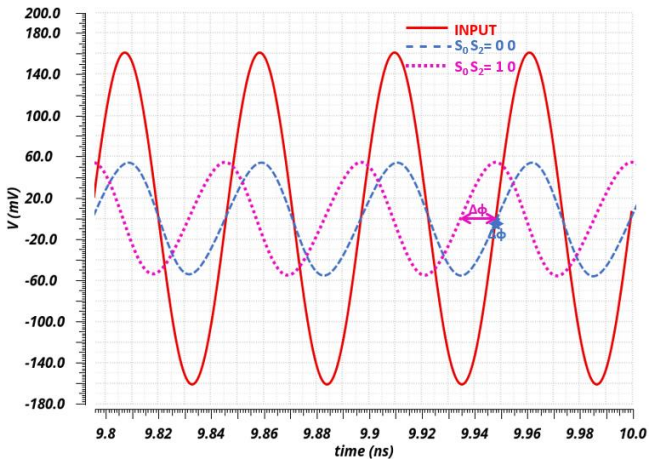

Fig. 21 Input and output waveforms obtained for two combinations (" S_0S_2 = 00 and 10") with V_{cntr} = 1,5 V

At the phase shifter's input, a 50 Ω input matching network (IMN) is used to ensure maximum power transfer from the injection source to the circuit. The reflection coefficient S_{11} displayed in Fig. 22 is less than -10 dB in the frequency range [18.20 GHz – 20.19 GHz] and reaches about -21.06 dB at 19.5 GHz, showing that the circuit is properly matched in this frequency band. In these conditions, with this circuit if we consider S_{11} = -15 dB, we can reach a bandwidth of about 2.2 GHz (i.e 11.3 % between 18.10 and 20.30 GHz). This ensures that the circuit is properly matched for the intended application.

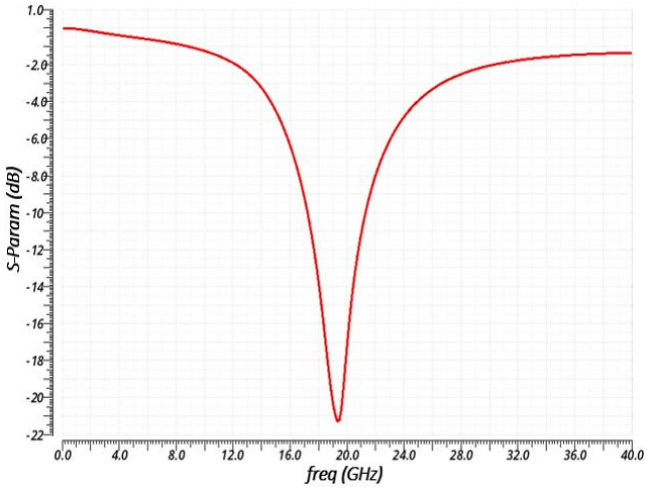

Fig. 22 Reflection coefficient (S11) as a function of frequency

The overall results and performances are summarized in Table 2. In addition, Table 3 demonstrates and compares the performances between the proposed active phase shifter and other recently published phase shifters. It can be noted that the proposed circuit consumes less power and occupies a reasonable area as compared to the existing state of the art.

Table 2 Summary of the phase shifter performances

Parameter	**Value**
Supply voltage	1.3 V
Tuning Range	17.87 – 20.16 GHz
f_{inj}	19.5 GHz
P_{inj}	-8.5 dBm
Phase shift range	360^0
Total Power consumption	26.61 mW
Power consumed by output buffer	4.31 mW
Average P_{out} on 50 Ω load	-15.58 dBm
Process	0.13 µm BiCMOS SiGe:C
Die size	1.310 * 1.150 mm^2

Table 3 Summary of the phase shifter performances

Parameter	[26]	[5]	[11]	[29]	This Work
Process	0.25 µm BiCMOS	0.25 µm BiCMOS	40 nm CMOS	0.13 µm BiCMOS	**0.13 µm BiCMOS**
Phase Control	Analog	Analog + Digital (2-bit)	Digital (8-bit)	Digital (6-bit)	**Analog +Digital (2-bit)**
Frequency (GHz)	24	5.8	28	6 -18	**19.5**
Phase Shift Range (°)	±90*/ continuous	360	360	360	**360**
Power Consumption (mW)	158	92.5	28.6	93.06	**26.61**
Chip Area (mm^2)	2.174	1.43	0.18	2.44	**1.51**
Supply Voltage (V)	3	2.5	1.1	3.3	**1.3**

* ±180 by adding a phase sign selector

5. CONCLUSION

Using a 0.13µm SiGe:C BiCMOS process, a fully integrated active phase shifter at 19.5 GHz for beamforming of phased antenna array has been designed and implemented. By changing the two commands (S_0 and S_2) of the phase selector and its sign, the desired phase is synthesised for coarse tuning and by tuning the control voltage V_{cntr} of the ILVCO for fine tuning. Hence, a phase shift of 360° is obtained with a total power consumption of 26.61 mW (including the buffer) from a supply voltage of 1.3 V. The post layout results obtained have shown the potential of this proposed active phase shifter architecture for beamforming in 5G applications.

Acknowledgment

The authors would like to respectably thank PTDF, Nigeria for sponsoring the research work.

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NURADDEEN ADO MUHAMMAD
was born in the city of kano, Nigeria, in 1987. He barged a bachelor degree of Computer Engineering from Bayero University Kano in 2012, and received master's degree in Electronics and Communication Engineering from Jodhpur National University, India in 2016. He was a Computer Engineer II and academic staff in the Department of Computer Science and Mathematics at Nigeria Police Academy, Wudil, Kano from 2015 to 2019. His research interest is design of RF integrated circuits. He is currently working towards obtaining a Ph.D. in the XLIM Laboratory of University of Poitiers.

DAVID COREAU received the M.S. degree in electronics from the Ecole Nationale Supe´rieure d'Inge´nieurs de Limoges, France in 2000 and the Ph.D. degree from the University of Poitiers, France, in 2004. His doctoral dissertation concerned the behavioral study and design of integrated polyphases VCOs using Si and SiGe technologies for radio communications. From 2003 to 2005, he was with ACCO where he was in charge of the design of silicon RF integrated circuits. He joined the University of Poitiers, France, in 2005 as an assistant Professor and became an Associate Professor in 2006. His present research interests include RF and Microwave integrated circuits with an emphasis on VCOs, arrays of coupled oscillators and Injection-Locked Oscillators. He has published several papers in international journals (IEEE JSSC, AEU¨ IJEC, IET Microw.Antenn.Prop, J. Circ. Sys. Comp., Int. J. Microw. RF CAE, Microelectronics Journal) and conferences (RFIC, IMS, ECWT, CSICS, ISCAS, NEWCAS, ICECS, ECCTD, SMACD…). He has also three invited papers (ECAI'11, ECAI'13, EFTF/IFCS'17) and one French patent.

JEAN-MARIE PAILLOT (M'95) received the Ph.D. degree in electronics from the University of Limoges, France, in 1990. His thesis on the design of nonlinear analogic circuits and the study of the noise spectra of integrated oscillators was prepared at the Institute of Research for Optical Communications and Microwaves, Limoges. After graduation, he joined the Electronics Laboratory of PHILIPS Microwave, at Limeil, as an R&D engineer in charge of the design of analogical and numerical microwave monolithic integrated circuits. Since October 1992, he is with the University Institute of Technology, Angoulême as a Professor of Electronics Engineering and currently the institution's director. He is as well in charge of several contracts with industry, and author of a many papers published in scientific journals. Presently he is interested in phase noise reduction techniques for microwave oscillators, as well as in the research and development of switched capacitor filters in RF domain.