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LUT-based design of a cryogenic cascode LNA with simultaneous noise and power matching

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Abstract—In recent years, cryogenic silicon electronics have gained increased interest for applications in fields such as quantum computers and space exploration. Unfortunately, commercial technologies lack cryogenic compact models for circuit design. In this paper, we target the sizing of the critical input stage of a power efficient low-noise amplifier working at 7 GHz and 4 K with simultaneous noise and power matching for meeting the stringent specifications of a gate-dispersive readout circuit for spin quantum bits. In the absence of a compact model for the transistors in 28 nm FD-SOI technology, we propose a design methodology using a look-up table that has been built with 4 K DC measurements of technology transistors and their associated capacitors to demonstrate the feasibility of the circuit.

Index Terms—Cryo-CMOS, LNA, Qubit, Look-Up Table, Fano factor.

I. INTRODUCTION

Cryogenic electronics have seen a recent interest due to its application in fields such as quantum computers, physics research, satellite communication and many others [1]. A great opportunity hence exists for the semiconductor industry to leverage the expertise of silicon manufacturing processes to cryogenic environments. However, mature compact models in CMOS technologies addressing such applications are not yet available or limited in scope, breaking the design process and optimization of electronic systems. To address this shortcoming, we propose a Look-Up Table (LUT) design environment created in MATLAB which exploits a set of transistor cryogenic measurements.

This paper presents the design methodology for sizing the critical input stage of a cascode Low-Noise Amplifier (LNA) with simultaneously input and noise matching for spin quantum bit readout using the developed cryogenic design environment. Section II presents the LUT-based design environment and the data that can be extracted for describing the circuit components. Using a cascode amplifier as case-study, Section III illustrates how the circuit analysis is carried out by integrating its components in the design environment. Section IV presents the circuit equations that are incorporated in the environment for achieving Simultaneous Noise and Power Matching (SNPM) of a cascode amplifier. Section V presents experimental results for sizing the critical input stage of a cryogenic LNA with SNPM. Finally, Section VI gives some conclusions and directions for future work.

II. CRYOGENIC LUT-BASED DESIGN ENVIRONMENT

LUT-based design was initially developed to counteract the complexities brought by short-channel transistors in advanced technology nodes [2]. In this work, the LUT-based approach is helpful for the design of cryo-CMOS amplifiers which is today limited by the lack of compact models, requiring iterative design procedures that often involves optimizations after fabrication.

In this paper, we enhance the LUT-based design approach by: (1) making use of two-port network theory for handling subcircuits and their interconnections [3], (2) modeling transistor white noise at any temperature by employing the Fano noise suppression factor and the equivalent gate resistance, and (3) exploiting the fact that the normalized transconductance efficiency is relatively independent of temperature and related to the Fano factor [4].

A. Basic two-port blocs

The LUT-based design environment is built upon the premise that the circuit can be regarded as a decomposition of simpler two-port networks. For example, a cascode amplifier can be viewed as an interconnection of basic two-port blocks such as active common source, common gate or common drain stages, or passive elements such as resistors, inductors or capacitors. For AC and noise analysis, the basic blocks are represented in terms of small-signal matrix models, such as ABCD or y-parameter matrices. The relationships between the basic blocks in a circuit determine the type of matrices to be used for each basic block, requiring in certain instances to transform the matrices from one type to another. This simplifies the matrix operations for constructing a single two-port representation of the amplifier.

Depending on the level of accuracy needed, the small-signal model can vary on complexity and on the number of elements composing it. However, in order to satisfy the simulation requirements, this model should be valid for a wide range of frequencies and have an equal behavior as the complete model regardless of the terminal used as input signal. For a common source transistor used later for example, its y-parameter matrix representation is given by

$$[Y_{cs}] = \begin{bmatrix} \frac{s(C_{gs}+C_{gd})}{1+s(C_{gs}+C_{gd})R_g} & \frac{-sC_{gd}}{1+s(C_{gs}+C_{gd})R_g} \\ \frac{g_m-sC_{gd}}{1+s(C_{gd}+C_{gs})R_g} & g_{ds} + sC_{db} + \frac{sC_{gd}(g_m+\frac{1}{R_g}+sC_{gs})}{s(C_{gs}+C_{gd})+\frac{1}{R_g}} \end{bmatrix}. \quad (1)$$

B. Noise correlation matrix

For high-frequency noise modeling, we follow a similar approach of two-port decomposition [6]. From network theory, noise sources associated with each port are enough for completely characterizing the noise behavior of a circuit. In the case of radio-frequency amplifiers, a popular convention is to use the input-referred noise sources. These noise sources are used to build a matrix representation of the noise of a circuit known as noise correlation matrix. Noise correlation matrices of individual blocks are used for simulating complex amplifiers [7]. For a single two-port common source transistor, the noise sources considered are the voltage noise due to the gate resistance, and the current noise due to the channel. The complete noise representation is given by its ABCD noise correlation matrix as follows

$$[C_{Acs}] = \begin{bmatrix} \overline{v_{ng}^2} + \frac{i_{nd}^2}{g_m^2} (1 + \omega^2 R_g^2 C_{gg}^2) & \frac{i_{nd}^2}{g_m^2} (\omega^2 C_{gg}^2 R_g - j\omega C_{gg}) \\ \frac{i_{nd}^2}{g_m^2} (\omega^2 C_{gg}^2 R_g + j\omega C_{gg}) & \frac{i_{nd}^2}{g_m^2} \omega^2 C_{gg}^2 \end{bmatrix}. \quad (2)$$

The transistor gate noise voltage is represented by the thermal model $\overline{v_{ng}^2} = 4kT\Delta f R_g$ which depends on the temperature profile of the gate resistance R_g . Experimental measurements for CMOS technology have shown a linear decrease of resistance with temperature down to around 50 K, where carrier freeze-out results in saturation or slight resistance increase at lower temperatures [5].

The transistor channel noise on the other hand is modeled by using the Fano noise suppression factor F_a as $i_{nd}^2 = 2qI_d\Delta f F_a$. Recent studies suggest that the Fano factor is a relatively temperature independent parameter [4] that can predict the channel white noise value, contrary to the conventional thermal model that overestimates the noise improvement seen at cryogenic temperatures [5]. The Fano factor serves as an indication of the degree of shot noise suppression with respect to the full shot noise level $2qI_D\Delta f$. For weak inversion, the shot noise is dominant corresponding to a diffusion current and F_a tends to 1. For strong inversion, F_a tends to 0 and shot noise is suppressed corresponding to a drift current where thermal noise is dominant [11].

C. Normalized transconductance efficiency and equivalent slope factor

The transistor normalized transconductance efficiency $g_m/I_d|_{norm}$ is given by

$$\frac{g_m}{I_d}|_{norm} = n_{eq}U_T \cdot \frac{g_m}{I_d} \quad (3)$$

where $U_T = kT/q$ is the thermal voltage and n_{eq} is the equivalent slope factor that captures the temperature dependence of the slope factor at low temperatures. This factor can be extracted at temperature T using [13]

$$n_{eq}(T) = \frac{SS(T)}{\ln 10 U_T} \quad (4)$$

where $SS(T)$ is the Subthreshold Swing extracted from the $\log(I_{ds})$ - V_{gs} DC characteristic at temperature T.

As shown in Fig. 1 by simulations in the standard temperature range for a 28 nm FD-SOI technology, the Fano factor follows a rather linear relationship with the normalized transconductance efficiency given by

$$F_a = \frac{2\gamma_n}{n_{eq}} \cdot \frac{g_m}{I_d}|_{norm} \quad (5)$$

where γ_n represents the excess noise factor, which divided by n_{eq} is almost temperature independent. $g_m/I_d|_{norm}$ turns out to be a rather temperature independent parameter [13] that represents the level of inversion of the transistor. The use of normalized equations and the denormalization at cryogenic temperature facilitate the design.

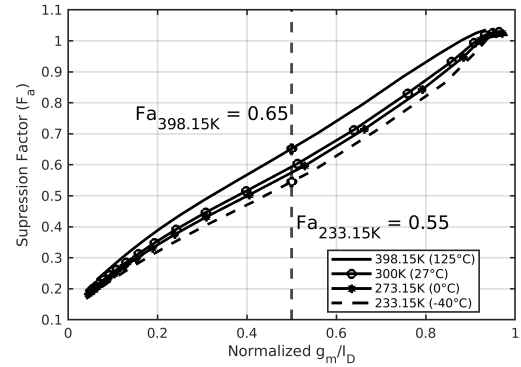


Fig. 1. Fano factor versus $g_m/I_d|_{norm}$ in 28 nm FD-SOI in the standard temperature range.

D. LUT-based design environment

The parameters that are required in the circuit matrices and the design equations are calculated from the measurements that are present in the LUT, at a given temperature T. The LUT is constructed by doing a 4-dimensional sweep of the voltage terminals of a transistor and its length (L , V_{GS} , V_{DS} and V_{SB}), and storing in a database the values of I_d and transistor capacitors obtained at room and cryogenic temperatures, as shown in Fig. 2 [2]. The Matlab environment is used for representing the circuit matrices and the design equations, and doing searches in the LUT.

In the case that there are some measurement limitations or incomplete data, it is also possible to complete missing data using simplified transistor models such as sEKV [8] [9] or ACM [10] at cryogenic temperatures, or simulations of the design kit in the standard temperature range.

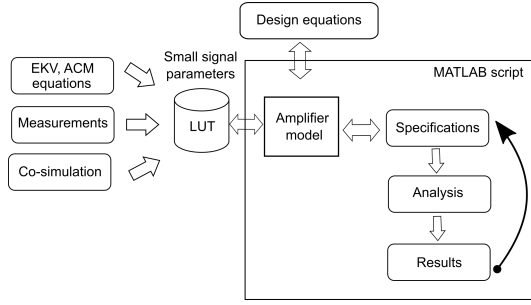


Fig. 2. LUT-based design environment.

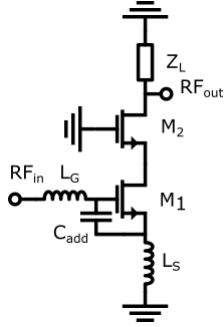


Fig. 3. Schematic of cascode LNA (bias not shown and AC output obtained via a transformer in the Z_L tank).

III. CASCODE LNA DECOMPOSITION

A cascode LNA as shown in Fig. 3 can be analyzed as a network consisting of a basic amplifying stage with a feedback section. The basic amplifying stage is composed by the cascaded interconnection of a common source, common gate and a parallel load tank formed by a capacitance, inductor and resistor. On the other hand, the feedback section is composed of the input (L_G) and degeneration (L_S) inductances and the feedback capacitor (C_{add}) [17].

The cascode amplifier seen as a feedback network in Fig.4 facilitates the analysis as an interconnection of basic two-ports subcircuits. The basic amplifying network can be seen as individual ABCD matrices cascaded, while the series-series feedback section can be viewed as a single two-port network of inductances L_G and L_S and capacitor C_{add} . For a series-series connection, and under the assumption that both the main amplifying stage and feedback are in a z-parameter representation, the equivalent two-port representation is equal to the addition of each of the impedance matrices. The cascode amplifier is then reduced to a single equivalent two-port transmission matrix. For noise analysis considering noise correlation ABCD matrices, the equivalent two-port noise correlation matrix of two cascaded blocs is given by

$$C_A = A_1 C_{A_2} A_1^* + C_{A_1} \quad (6)$$

and this matrix is converted to an equivalent z-parameter matrix that is added with the z-parameter matrix of the feedback block to obtain the equivalent noise matrix of the overall amplifier.

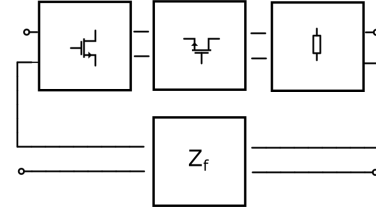


Fig. 4. Cascode LNA as an interconnection of two-port subcircuits for MATLAB analysis.

IV. CRYOGENIC LNA FOR SPIN QUBIT READOUT

The LNA for a spin quantum bit readout must have a very low noise figure while also aiming at a very low power consumption with sufficient gain. To this end, we show here the LUT-based design of the input stage which is the major contributor to the noise figure of the overall LNA. The design starts with the sizing and biasing of the input transistor M1 in Fig. 3 for values that result in a trade-off between the minimum noise figure F_{min} and the current efficiency g_m/I_D . F_{min} is related to the Fano factor by [6]

$$F_{min} = 1 + \frac{I_d F_a}{U_{T_o}} \left(\frac{f}{f_t} \right)^2 R_g + \frac{f}{f_t} \sqrt{\left(\frac{I_d F_a}{U_{T_o}} \right)^2 \left(\frac{f}{f_t} \right)^2 R_g^2 + 2R_g \frac{I_d F_a}{U_{T_o}} \frac{T}{T_o}} \quad (7)$$

where the dependency with the transit frequency $f_t = g_m/(2\pi C_{gg})$ helps determine the appropriate transistor length. However, the lowest F_{min} is obtained for the shortest length.

By combining Eqs. 5 and 7, we can derive the dependency of F_{min} with the normalized g_m/I_D as shown in Fig. 5. As suggested in [9], the moderate inversion is a good compromise between power consumption, noise figure and transistor speed.

The design procedure starts by choosing a compromise between F_{min} and the normalized g_m/I_D in the moderate inversion region. After choosing the normalized g_m/I_D , from the LUT at 4 K, we can extract n_{eq} using Eq.4.

Transistor M1 will be composed of N_f fingers that will give a transistor width of

$$W = N_f \cdot W_f. \quad (8)$$

For the 28 nm FD-SOI technology, an optimum gate finger width around $1 \mu m$ is reported [14] to optimize the gate resistance and minimize F_{min} . For achieving a noise figure equal to the lowest possible value of the technology F_{min} , we need to present to the input of the transistor an impedance equal to the optimum impedance Z_{sopt} . The optimum impedance for a single finger is obtained as [6]

$$Z_{sopt} = \sqrt{R_g^2 + 2R_g \left(\frac{f_t}{f} \right)^2 \frac{U_T}{I_d F_a}} + \frac{j}{\omega C_{gg}} \quad (9)$$

and the number of fingers N_f will be chosen so that Z_{sopt} can be brought to $Z_s = 50 \Omega$. This may need the help of an added capacitor C_{add} at the gate input of transistor M1 as shown in

Fig. 3, so that simultaneous input and noise matching can be obtained with inductance values that can be integrated. The new transit frequency is given by [15]

$$f_t' = \frac{g_m}{2\pi(C_{gg} + C_{add})} \quad (10)$$

from which we can calculate the required C_{add} although it will penalize the amplifier gain.

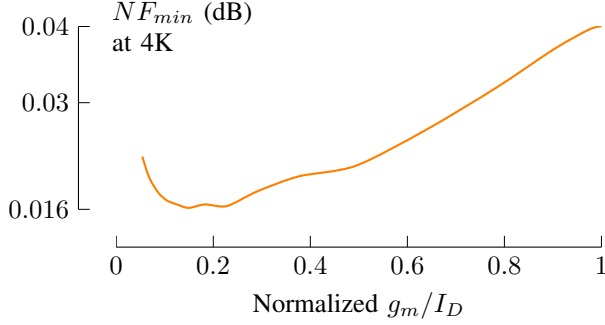


Fig. 5. The LUT-generated NF_{min} reaches its lowest value at strong inversion $g_m/I_D|_{norm} \approx 0.2$. This minimum inversion region is maintained regardless of temperature variations.

The gain of the cascode LNA, assuming that both transistors have the same sizing and polarity, can be approximated as

$$A_v = \frac{-(g_m r_{ds} + 1) g_m r_{ds}}{1 + s \left[(R_g + R_o)(C_{gg} + C_{add}) + L_s g_m + \frac{C_{gg}}{g_m} \right]} \quad (11)$$

The input impedance for a degenerated common source transistor with an added gate inductance is given by [12]

$$Z_{in} = s(L_S + L_G) + \frac{1}{s(C_{gg} + C_{add})} + 2\pi f_t' L_s \quad (12)$$

where the last term fixes the real part of the input impedance. Thus $L_S = \frac{Z_s}{2\pi f_t'}$ while $L_G = \frac{1}{2\pi f_0(C_{gg} + C_{add})} - L_S$ is used to tune the imaginary part.

The overall procedure is implemented in Matlab, so that after choosing the trade-off point between F_{min} and normalized g_m/I_D , the LUT search directly finds the different component values. Finally, it must be noticed that in the case of MOSFETs, it is possible to achieve simultaneous noise and input matching due to the fact that the imaginary parts of Z_{in} and Z_{sopt} have typically a difference around 20% [15].

V. EXPERIMENTAL RESULTS

We target the design of a 28 nm FD-SOI LNA for quantum readout applications working at $T_s = 4$ K, with a sensitivity $K_B(T_s + T_e)$ of -120 dBm (equivalent input noise temperature $T_e \approx 4$ K) for reading an input signal of power -100 dBm in a band of 2 GHz centered at the operation frequency of 7 GHz. Power consumption should be around 1 mW per quantum bit measured. Since the NF is mostly set by the input stage, we illustrate here the sizing of the input transistor M1 in Fig. 3 and the values of other components for operation at 4 K and 7 GHz.

We consider for the cascode LNA the same sizing and biasing for transistors M1 and M2, with $V_{ds} = 0.5$ V. We have estimated the gate resistance considering a simulation of the 28 nm FD-SOI transistor in the standard temperature range, giving the relationship $R_{g_{sq}} = 0.0341 * T(K) + 21.241$. We extrapolate the value of $R_{g_{sq}}$ down to 50 K and we assume this value at 4 K, giving $R_{g_{sq}}(4K) = 22.9 \Omega$. The values of the transistor capacitors are extracted from the LUT at 4 K.

We choose a value of $g_m/I_D|_{norm} = 0.5$ in moderate inversion that results in a $NF_{min} = 21.9$ mdB. Using Eq.4 we obtain a slope factor $n_{eq} = 29.7$ which leads to $g_m/I_D = 48.8 S/A$, $I_{ds} = 873.7 \mu A$ (thus a power consumption of $873.7 \mu W$ for a power supply of 1 V) and $g_m = 38.9 mS$, with an operation point of $V_{gs} = 0.444$ V and $V_{ds} = 0.5$ V. Simultaneous input and noise matching is obtained with $N_f = 99$ fingers, with $C_{gg} = 57.6$ fF and $R_g = 7.7 \Omega$. We obtain this way a $Z_{sopt} = 50 \Omega$ but the resulting value of the gate inductance is too large to be integrated. We consider then an additional feedback capacitor $C_{add} = 122$ fF which results in $L_s = 266.6 pH$ and $L_g = 2.6 nH$. The gain obtained is $A_v = 42.3 dB$ around the central frequency of 7 GHz. By using these values in Eqs. 5 and 7 and combining them, we obtain a value of the Fano factor at 4 K of $F_a = 0.59$ and a $NF = 136.2$ mdB. The estimated bandwidth, measured on the pass-band gain, is about 7.2 GHz.

The design values we show here are in the order of those obtained in state-of-the-art cryogenic LNAs working in this range of frequencies and with the same LNA input stage topology [17]. Furthermore, the LUT-based design environment will allow us in the future to investigate further compromises between noise figure, power consumption and gain. Since the LNA can be used to read simultaneously a large number of quantum bits, it is possible to seek lower values of noise figure required by gate-dispersive spin quantum bit readout circuits, with higher values of power consumption but meeting the requirements per quantum bit read.

VI. CONCLUSION

This paper shows the use of a LUT-based cryogenic design environment for sizing a LNA that is aimed at quantum bit readout circuits. The inversion level of the minimum length input transistor allows a good trade-off between the minimum noise figure and the gain and power consumption. Although simultaneous noise and input matching is possible, the values of the inductances are too large for integration. The use of an additional feedback capacitor degrades the noise figure but results in inductance values that are smaller for integration. These results show the feasibility of using the 28 nm FD-SOI technology to meet the stringent quantum readout applications targeted, before proceeding in the future with a full LNA design.

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